MOTOROLA

MC74F112

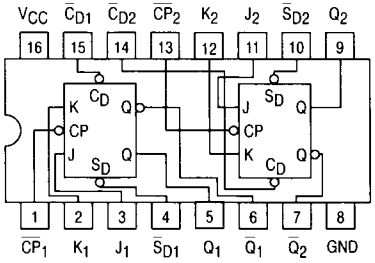
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

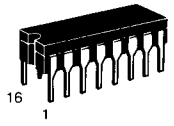
The MC74F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

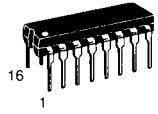
FAST™ SCHOTTKY TTL

CONNECTION DIAGRAM

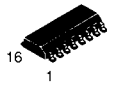




J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

FUNCTION TABLE (Each Half)

Inputs		Output
@ t_n		@ $t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:

LOW Input to S_D sets Q to HIGH level

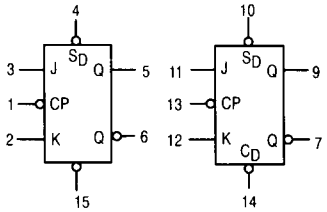
LOW Input to C_D sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on C_D and S_D makes both Q and Q HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
$t_n + 1$ = Bit time after clock pulse

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

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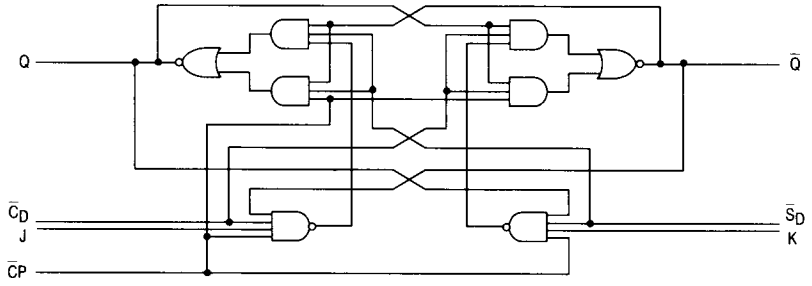
LOGIC DIAGRAM (one half shown)



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−1.0	mA
I_{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	74	2.5	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					100	µA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current (J and K Inputs)				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
	($\overline{CP}$ Inputs)				−2.4	mA		
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				−3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			12	19	mA	V_{CC} = MAX, V_{CP} = 0 V	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		74F T_A = 0°C to +70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		Unit
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	110				MHz
t_{PLH}	Propagation Delay	2.0	6.5	2.0	7.5	ns
t_{PHL}	$\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0	6.5	2.0	7.5	
t_{PLH}	Propagation Delay	2.0	6.5	2.0	7.5	ns
t_{PHL}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0	6.5	2.0	7.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0 V			74F T_A = 0°C to +70°C V_{CC} = 5.0 V ± 10%		Unit
		Min	Typ	Max	Min	Max	
t_s (H)	Setup Time, HIGH or LOW	4.0			4.0		ns
t_s (L)	J_n or K_n to $\overline{CP}_n$	3.0			3.0		
t_h (H)	Hold Time, HIGH or LOW	0			0		
t_h (L)	J_n or K_n to $\overline{CP}_n$	0			0		
t_w (H)	$\overline{CP}_n$ Pulse Width, HIGH	4.5			4.5		ns
t_w (L)	or LOW	4.5			4.5		
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.5			4.5		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	4.0			5.0		ns

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