National Semiconductor

MICROCIRCUIT DATA SHEET

CN54F175-X REV 0A0

Original Creation Date: 01/12/98
Last Update Date: 02/02/98
Last Major Revision Date: 01/12/98

QUAD D FLIP-FLOP

General Description

The F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

Industry Part Number

54F175

NS Part Numbers

54F175DC

Prime Die

M175

Processing

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Quality Conformance Inspection

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Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+70
3	Static tests at	0
4	Dynamic tests at	+25
5	Dynamic tests at	+70
6	Dynamic tests at	0
7	Functional tests at	+25
8A	Functional tests at	+70
8B	Functional tests at	0
9	Switching tests at	+25
10	Switching tests at	+70
11	Switching tests at	0

Features

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge- Triggered Clock
- Asynchronous Common Reset
- True and Complement Output

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0 C to +70 C
Supply Voltage	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=5.5V	1, 2	INPUTS		5.0	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=7.0V, VINH=5.5V	1, 2	INPUTS		7.0	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.5V	1, 2	INPUTS		-0.6	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIL=0.8V, IOL=20mA, VINH=5.5V, VINL=0.0V, VIH=2.0V	1, 2	OUTPUTS		0.5	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, VIH=2.0V, IOH=-1.0mA, VIL=0.8V, VINL=0.0V	1, 2	OUTPUTS	2.5		V	1, 2, 3
		VCC=4.75V, VIH=2.0V, IOH=-1.0mA, VIL=0.8V, VINL=0.0V	1, 2	OUTPUTS	2.7		V	1, 2, 3
IOS	Short Circuit Current	VCC=5.5V, VINH=5.5V, VM=0.0V, VINL=0.0V	1, 2	OUTPUTS	-60	-150	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=5.5V	1, 2	INPUTS		-1.2	V	1, 2, 3
ICC	Supply Current	VCC=5.5V, VINH=5.5V	1, 2	VCC		34	mA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VINH=5.5V, VINL=0.0V, VM=5.5V	1, 2	OUTPUTS		100	uA	1, 2, 3
VID	Input Leakage Test	VCC=0V, IID=1.9uA	1, 2	INPUTS	4.75		V	1, 2, 3
IOD	Output Leakage Circuit Current	VCC=0V, VIOD=0.15V	1, 2	OUTPUTS		4.75	uA	1, 2, 3
VIL	Input Low Voltage	Recognized as a LOW signal	3	INPUTS		0.8	V	1, 2, 3
VIH	Input High Voltage	Recognized as a HIGH signal	3	INPUTS	2.0		V	1, 2, 3

Electrical Characteristics

AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(1)	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @0C/+70C	1, 2	CP to Qn or $\overline{Qn}$	4.0	6.5	ns	9
			1, 2	CP to Qn or $\overline{Qn}$	3.5	7.5	ns	10, 11
tpHL(1)	Propagation Delay	VCC= 5.0V @25C, VCC=4.5V & 5.5V @0C/+70C	1, 2	CP to Qn or $\overline{Qn}$	4.0	8.5	ns	9
			1, 2	CP to Qn or $\overline{Qn}$	4.0	9.5	ns	10, 11
tpLH(2)	Propagation Delay	VCC= 5.0V @25C, VCC=4.5V & 5.5V @0C/+70C	1, 2	$\overline{MR}$ to $\overline{Qn}$	4.0	8.0	ns	9
			1, 2	$\overline{MR}$ to $\overline{Qn}$	4.0	9.0	ns	10, 11
tpHL(2)	Propagation Delay	VCC= 5.0V @25C, VCC=4.5V & 5.5V @0C/+70C	1, 2	$\overline{MR}$ to Qn	4.5	11.5	ns	9
			1, 2	$\overline{MR}$ to Qn	4.5	13.0	ns	10, 11
ts(H/L)	Setup Time	VCC= 5.0V @25C, VCC=4.5V & 5.5V @0C/+70C	4	Dn to CP	3.0		ns	9, 10, 11
th(H/L)	Hold Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @0C/+70C	4	Dn to CP	1.0		ns	9, 10, 11
tw(H)	Pulse Width	VCC=5.0V @25C, VCC=4.5V & 5.5V @0C/+70C TR/TF=1.0ns	4	CP	4.0		ns	9, 10, 11
tw(L)	Pulse Width	VCC=5.0V @25C, VCC=4.5V & 5.5V @0C/+70C TR/TF=1.0ns	4	CP	5.0		ns	9, 10, 11
tw (L)	Pulse Width	VCC=5.0V @25C, VCC=4.5V & 5.5V @0C/+70C TR/TF=1.0ns	4	$\overline{MR}$	5.0		ns	9, 10, 11
tREC	Recovery Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @0C/+70C	4	$\overline{MR}$ to CP	5.0		ns	9, 10, 11
fMAX	Maximum Count Frequency	VCC=5.0V @25C, VCC=4.5V & 5.5V @0C/+70C TR/TF=1.0ns	4	CP	100		MHZ	9, 10, 11

Note 1: Screen tested 100% on each device at +75C temperature, subgroups 2, 8A & 10.
Note 2: Sample tested (Method 5005, Table 1) on each MFG. lot at +75C temperature, subgroups 2, 8A & 10.
Note 3: Guaranteed by applying specific input condition and testing VOL & VOH.
Note 4: GUARANTEED BUT NOT TESTED. (Design Characterization Data)

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002747	02/02/98	Donald B. Miller	Initial MDS Release