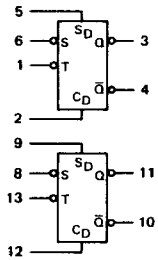
MC978 • MC878

Available in TO-86 Flat Package, Add F Suffix.

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S_D and C_D inputs may be used for asynchronous operation.



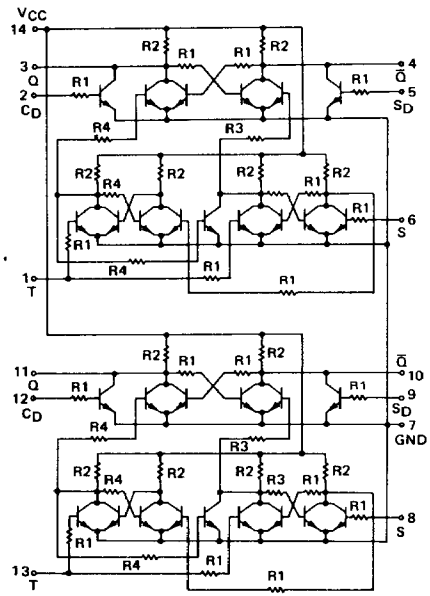
DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	③
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ④

t_n	t_{n+1}	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_C = C_C = 0$. The output state cannot be predetermined in the case when the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 180
R4 = 480

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

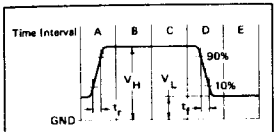
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC978	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC878	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC978 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC878 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	$1.8\,I_{in}$	1	-	225	-	234	-	198	μAdc	-	270	-	252	-	252	μAdc	1	-	6	-	14	-	2, 5, 7
	$1.8\,I_{in}$	1	-	225	-	234	-	198		-	270	-	252	-	252		1	-	-	-		-	2, 5, 6, 7
	I_{in}	2#	-	125	-	130	-	110		-	150	-	140	-	140		2	-	-	-		-	5, 6, 7
		5#	-		-		-			-		-		-			5	-	6	-		-	2, 7
		6#	-		-		-			-		-		-			6	-	-	-		-	2, 5, 7
Output Current	I_{A3}	3	350	-	364		308	-	μAdc	420	-	430	-	395	-	μAdc	3	1	5	2	14	-	6, 7
		3#		-				-			-		-		-		3	6	5	2		-	7
		4		-				-			-		-		-		4	1	2, 6	5		-	
		4#		-				-			-		-		-		4	-	2	5, 6		-	
Output Voltage	V_{out}	3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	1, 5	-	14	-	6, 7
		3	-		-		-			-		-		-			-	4	1	-		-	2, 5, 6, 7
		4	-		-		-			-		-		-			-	5	1, 2	-		-	6, 7
		4	-		-		-			-		-		-			-	3	1	-		-	2, 5, 6, 7
Saturation Voltage	$V_{CE(sat)}$	3	-	220	-	220	-	220	mVdc	-	450	-	400	-	350	mVdc	2	-	1, 5	-	14	-	6, 7
																	4	-	1	-		-	2, 5, 6, 7
		3	-		-		-			-		-		-			-	-	1	5		-	6, 7
		3*	-		-		-			-		-		-			-	-	-	6		-	2, 7
		3§†	-		-		-			-		-		-			-		5	-		-	2, 7
		3#‡	-		-		-			-		-		-			5	-	1, 2	-		-	6, 7
		4	-		-		-			-		-		-			3	-	1	-		-	2, 5, 6, 7
		4	-		-		-			-		-		-			-	-	1	2		-	6, 7
		4‡	-		-		-			-		-		-			-	6	-	-		-	5, 7
		4§*	-		-		-			-		-		-			-	-	2	-		-	5, 7
		4#**	-		-		-			-		-		-									
Current Leakage	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	1, 2, 5, 6, 7

* = Pin 1 Clock Pulse a
§ = Pin 1 Clock Pulse b
\# = Pin 2 Data Pulse a
** = Pin 6 Data Pulse a
† = Pin 5 Data Pulse a
‡ = Pin 6 Data Pulse b
See Figure 4

Ground inputs of flip-flop not under test. Other pins not listed are left open.

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

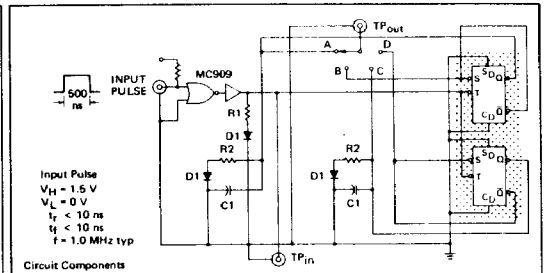
MC878

T_A	V_L	V_H
$+25^0$C	+460 ± 2.0 mVdc	+0.850 ± 2.0 mVdc
0^0C	+500 ± 2.0 mVdc	+0.900 ± 2.0 mVdc
$+75^0$C	+400 ± 2.0 mVdc	+0.760 ± 2.0 mVdc

MC978

T_A	V_L	V_H
$+25^0$C	+450 ± 2.0 mVdc	+0.800 ± 2.0 mVdc
-55^0C	+660 ± 2.0 mVdc	+0.985 ± 2.0 mVdc
$+125^0$C	+260 ± 2.0 mVdc	+0.605 ± 2.0 mVdc

FIGURE 2 - SWITCHING TIMES TEST AND WAVEFORMS



Input Pulse
V_H = 1.5 V
V_L = 0 V
t_r < 10 ns
t_f < 10 ns
f = 1.0 MHz typ

Circuit Components
C1 = 8.0 pF including jig and probe
R1 = 220 ohms ± 1.0%
R2 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or equivalent

SWITCHING TIMES

TEST	SWITCH	MAXIMUM (ns @ 25°C)
t_{T-Q+}	A	120
t_{T-Q-}	A	80
$t_{T-\bar{Q}+}$	B	120
$t_{T-\bar{Q}-}$	B	80
$t_{T-\bar{Q}+}$	D	120
$t_{T-\bar{Q}-}$	D	80
t_{T-Q+}	C	120
t_{T-Q-}	C	80

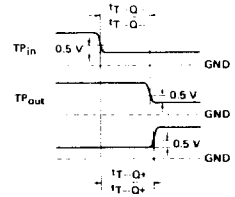


FIGURE 3A - SET UP AND RELEASE TIMES TEST CIRCUIT

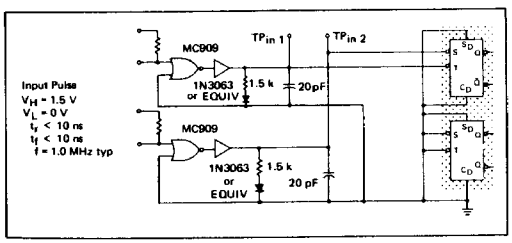


FIGURE 3B - INPUT PULSE WIDTHS FOR SET UP AND RELEASE TIMES

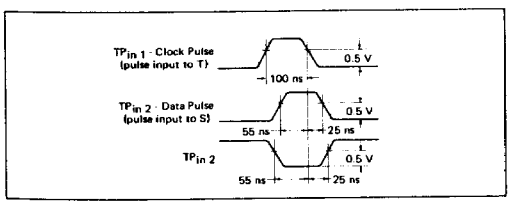
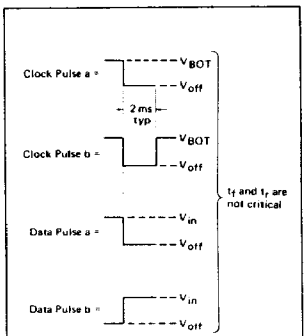


FIGURE 4 - CORRELATION OF CLOCK PULSE a & b AND DATA PULSE a & b



When applicable, the negative transition of Clock Pulse a must precede the transition of Data Pulse a and Data Pulse b. The negative and positive transitions of Clock Pulse b must follow the negative transition of Data Pulse a.

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns