

# TYPE SN54L99 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

DECEMBER 1972—REVISED DECEMBER 1983

- N-Bit Serial-to-Parallel Converter
- N-Bit Parallel-to-Serial Converter
- N-Bit Storage Register
- J-K̄ Serial Input

### description

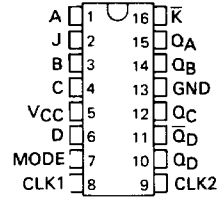
These 4-bit registers feature parallel inputs, parallel outputs, J-K̄ serial inputs, mode control, and two clock inputs. The registers have three modes of operation:

- Parallel (broadside) load
- Shift right (the direction Q<sub>A</sub> toward Q<sub>D</sub>)
- Shift left (the direction Q<sub>D</sub> toward Q<sub>A</sub>)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flop and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on a high-to-low transition of clock 1 when the mode control is low. Serial data for the right-shift mode is entered at the J-K̄ inputs. These inputs permit the first stage to perform as a J-K̄, a D-type, or T-type flip-flop as shown in the function table. Shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q<sub>D</sub> to input C, etc.). Serial data for this mode is entered at the D input. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

SN54L99 ... J PACKAGE  
(TOP VIEW)



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FUNCTION TABLE

MODE CONTROL	INPUTS								OUTPUTS				
	CLOCKS		SERIAL		PARALLEL				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q̄ <sub>D</sub>
	2 (L)	1 (R)	J	K̄	A	B	C	D					
H	H	X	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q̄ <sub>D0</sub>
H	↓	X	X	X	a	b	c	d	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	d	ā
H	↓	X	X	X	Q <sub>B</sub> †	Q <sub>C</sub> †	Q <sub>D</sub> †	d	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	d	ā
L	L	H	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q̄ <sub>D0</sub>
L	X	↓	L	H	X	X	X	X	Q <sub>A0</sub>	Q <sub>A0</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q̄ <sub>Cn</sub>
L	X	↓	L	L	X	X	X	X	Q <sub>A0</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q̄ <sub>Cn</sub>
L	X	↓	H	H	X	X	X	X	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q̄ <sub>Cn</sub>
L	X	↓	H	L	X	X	X	X	Q̄ <sub>An</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q̄ <sub>Cn</sub>
↑	L	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q̄ <sub>D0</sub>
↑	L	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q̄ <sub>D0</sub>
↑	L	H	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q̄ <sub>D0</sub>
↑	H	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q̄ <sub>D0</sub>
↑	H	H	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q̄ <sub>D0</sub>

† Shifting left requires external connection of Q<sub>B</sub> to A, Q<sub>C</sub> to B, and Q<sub>D</sub> to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level.

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>C0</sub>, Q<sub>D0</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the indicated steady state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>, Q<sub>Dn</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the most-recent ↓ transition of the clock.

### PRODUCTION DATA

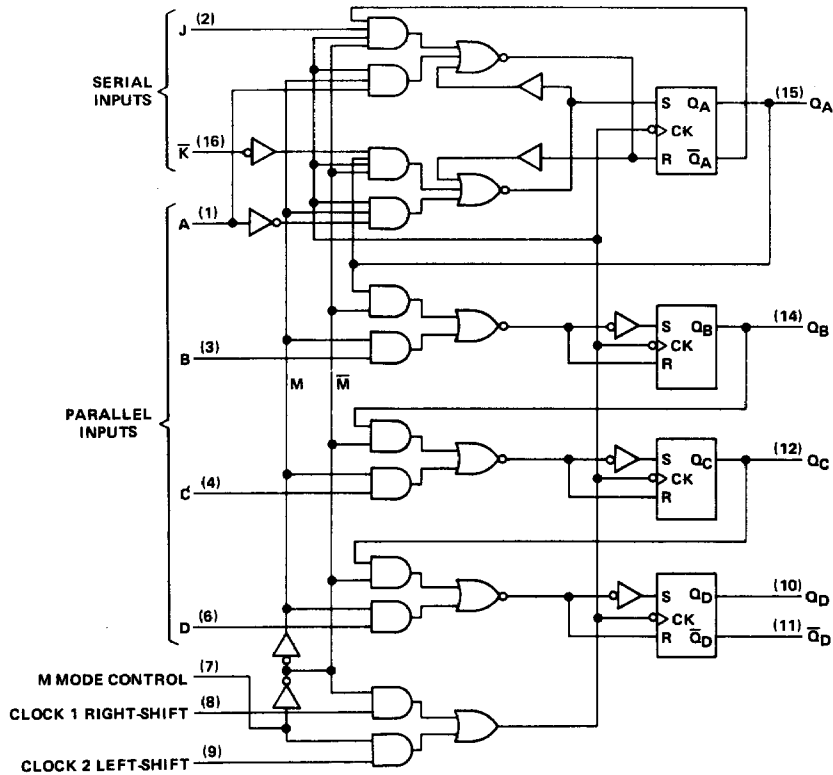
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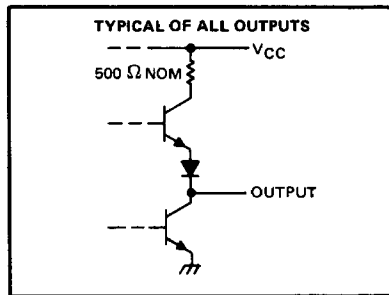
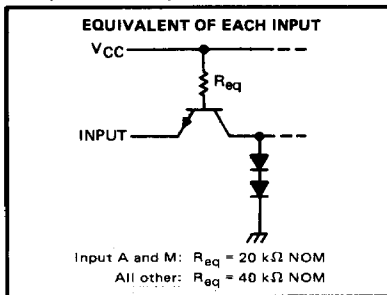
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TYPE SN54L99  
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

logic diagram



schematics of inputs and outputs



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# TYPE SN54L99 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	8 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range	-55°C to 125°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.  
2. Input voltages must be zero or positive with respect to network ground terminal.

## recommended operating conditions

	SN54L99	UNIT		
			MIN	NOM
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.7	V
$I_{OH}$ High-level output current			-0.1	mA
$I_{OL}$ Low-level output current			2	mA
$t_w(\text{clock})$ Width of clock pulse	200			ns
$t_{su}(H)$ Setup time for high-level data at J, $\bar{K}$ , A, B, C, or D inputs	100			ns
$t_{su}(L)$ Setup time for low-level data at J, $\bar{K}$ , A, B, C, or D inputs	120			ns
$t_h$ Hold time at J, $\bar{K}$ , A, B, C, or D inputs	0			ns
$t_{enable 1}$ Time to enable clock 1 (See Figure 1)	225			ns
$t_{enable 2}$ Time to enable clock 2 (See Figure 1)	200			ns
$t_{inhibit 1}$ Time to inhibit clock 1 (See Figure 1)	100			ns
$t_{inhibit 2}$ Time to inhibit clock 2 (See Figure 1)	0			ns
$T_A$ Operating free-air temperature	-55		125	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54L99		UNIT
		MIN	TYP ‡	
$V_{OH}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OH} = -0.1 \text{ mA}$	2.4	3.3	V
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OL} = 2 \text{ mA}$	0.15	0.3	V
$I_I$	J, $\bar{K}$ , B, C, or D			mA
	M or A		0.1	
$I_{IH}$	J, $\bar{K}$ , B, C, or D		0.2	$\mu\text{A}$
	M or A	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	10	
$I_{IL}$	J, $\bar{K}$ , B, C, or D		20	mA
	M or A	$V_{CC} = \text{MAX}, V_I = 0.3 \text{ V}$	-0.18	
$I_{OS} §$	$V_{CC} = \text{MAX}$		-0.36	
$I_{CC}$	$V_{CC} = \text{MAX},$ See Note 3	-3	-15	mA
		3.8	9	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.  
‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 3: With all outputs and J and  $\bar{K}$  inputs open, mode control at 4.5 V, inputs A through D grounded,  $I_{CC}$  is measured after a momentary 3 V, then ground is applied to both clock inputs.

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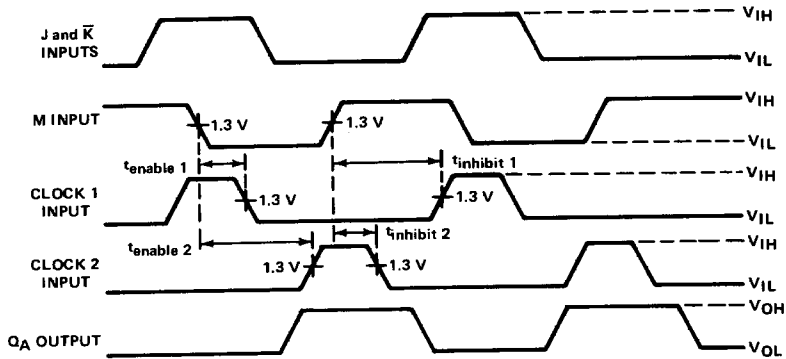
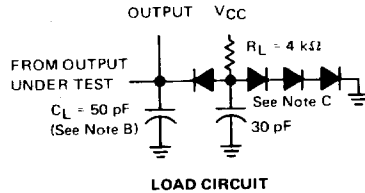
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# TYPE SN54L99 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{max}}$	Any	Any	$R_L = 4\text{ k}\Omega$ , $C_L = 50\text{ pF}$ See Figures 1 and 2	3	5		MHz
$t_{\text{PLH}}$				115	200	ns	
$t_{\text{PHL}}$				125	200	ns	

## PARAMETER MEASUREMENT INFORMATION



NOTE: A input is at the low level.

**VOLTAGE WAVEFORMS  
FIGURE 1—CLOCK ENABLE/INHIBIT TIMES**

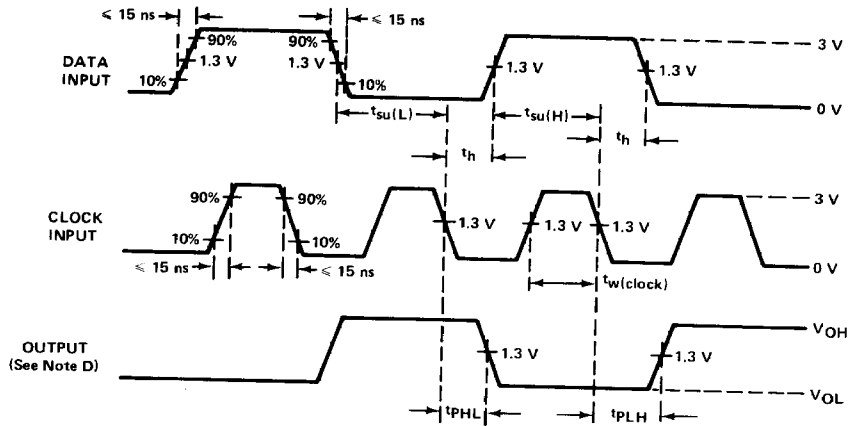
- NOTES: A. The input waveforms are supplied by pulse generators having the following characteristics:  $Z_{\text{out}} \approx 50\ \Omega$ . For data pulse generator:  $t_w \geq 150\text{ ns}$ ,  $\text{PRR} \leq 500\text{ kHz}$ ,  $t_{\text{setup(L)}} = 120\text{ ns}$ , and  $t_{\text{setup(H)}} = 100\text{ ns}$ . For clock pulse generator:  $t_w \geq 200\text{ ns}$  and  $\text{PRR} \leq 1\text{ MHz}$ . When testing  $f_{\text{max}}$ , vary PRR.
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. When data input is applied to J and K inputs, the output waveform applies only to output  $Q_A$ .

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**TYPE SN54L99**  
**4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS**

**PARAMETER MEASUREMENT INFORMATION**



**VOLTAGE WAVEFORMS**  
**FIGURE 2—SWITCHING TIMES**

- NOTES: A. The input waveforms are supplied by pulse generators having the following characteristics:  $Z_{out} \approx 50 \Omega$ . For data pulse generator:  $t_w \geq 150$  ns,  $PRR \leq 500$  kHz,  $t_{setup(L)} = 120$  ns, and  $t_{setup(H)} = 100$  ns. For clock pulse generator:  $t_w \geq 200$  ns and  $PRR \leq 1$  MHz. When testing  $f_{max}$ , vary PRR.
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. When data input is applied to J and K inputs, the output waveform applies only to output  $Q_A$ .

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