### SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS SDLS067A - OCTOBER 1976 - REVISED JUNE 1999

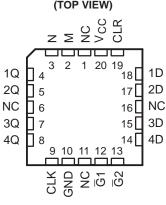
- 3-State Outputs Interface Directly With System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:
  - Parallel Load
  - Do Nothing (Hold)
- For Application as Bus Buffer Registers
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

TYPE	TYPICAL PROPAGATION DELAY TIME	MAXIMUM CLOCK FREQUENCY
'173	23 ns	35 MHz
'LS173A	18 ns	50 MHz

### description

The '173 and 'LS173A 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and

SN7417 SN74LS173	73 N	PA( or N	PACKAGE
	, U		<b>n</b>
M	1	16	J VCC
N	2	15	] CLR
1Q [	3	14	] 1D
2Q [	4	13	] 2D
3Q [	5	12	] 3D
4Q [	6	11	] 4D
CLK [	7	10	] G2
GND [	8	9	] <b>G</b> 1
SN54LS17	3A (TOP V		



NC - No internal connection

driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs can be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable ( $\overline{G1}$ ,  $\overline{G2}$ ) inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output-control (M, N) inputs also are provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54173 and SN54LS173A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74173 and SN74LS173A are characterized for operation from 0°C to 70°C.



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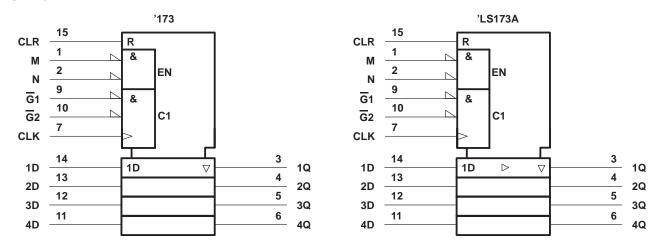
Copyright © 1999, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SDLS067A - OCTOBER 1976 - REVISED JUNE 1999

		FUNC1	TION TAB	LE	
		INPUTS			
CLR	CLK	DATA E	NABLE	DATA	OUTPUT
ULK	CLK	G1	G2	D	<u> </u>
Н	Х	Х	Х	Х	L
L	L	Х	Х	Х	Q <sub>0</sub>
L	$\uparrow$	Н	Х	Х	Q <sub>0</sub> Q <sub>0</sub> Q <sub>0</sub>
L	$\uparrow$	Х	Н	Х	Q <sub>0</sub>
L	$\uparrow$	L	L	L	L
L	$\uparrow$	L	L	Н	Н

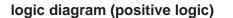
When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

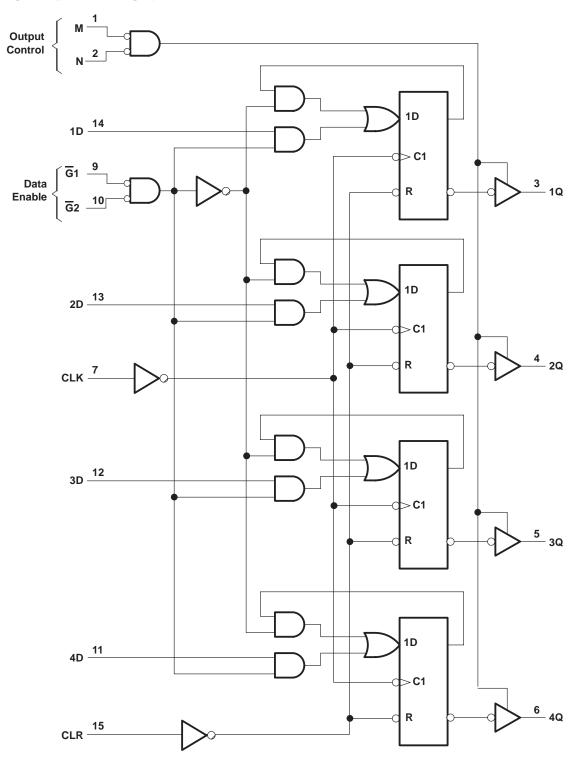
### logic symbol<sup>†</sup>



 $^\dagger$  This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.





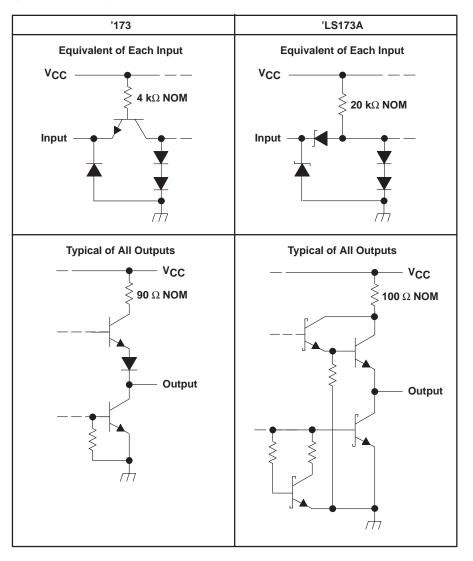


Pin numbers shown are for D, J, N, and W packages.



SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

### schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>CC</sub> (see Note 1)	
Input voltage: '173	–0.5 V to 5.5 V
'LS173A	–0.5 V to 7 V
Off-state output voltage	–0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	113°C/W
N package	
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



SDLS067A - OCTOBER 1976 - REVISED JUNE 1999

### recommended operating conditions (see Note 3)

		5	SN54173		5	SN74173		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
ЮН	High-level output current			-2			-5.2	mA
IOL	Low-level output current			16			16	mA
Т <sub>А</sub>	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	7507.00	TEST CONDITIONS		SN54173			SN74173		UNIT
	PARAMETER	TEST CO	NDITIONS	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	V
VIK	Input clamp voltage	$V_{CC} = MIN,$	l <sub>l</sub> = –12 mA			-1.5			-1.5	V
VOH	High-level output voltage	$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = MAX	2.4			2.4			V
VOL	Low-level output voltage	$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA			0.4			0.4	V
1	Off-state (high-impedance state)	V <sub>CC</sub> = MAX,	V <sub>O</sub> = 2.4 V			150			40	
IO(off)	output current	V <sub>IH</sub> = 2 V	V <sub>O</sub> = 0.4 V			-150			-40	μA
lj	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V			1			1	mA
IIН	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.4 V			40			40	μΑ
۱ <sub>IL</sub>	Low-level input current	$V_{CC} = MAX,$	V <sub>I</sub> = 0.4 V			-1.6			-1.6	mA
IOS	Short-circuit output current§	$V_{CC} = MAX$		-30		-70	-30		-70	mA
ICC	Supply current	V <sub>CC</sub> = MAX,	See Note 4		50	72		50	72	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

§ Not more than one output should be shorted at a time.

NOTE 4: I<sub>CC</sub> is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, G1, G2, and all data inputs grounded; and CLK and M at 4.5 V.

### timing requirements over recommended operating conditions (unless otherwise noted)

			SN54	173	SN74	UNIT	
			MIN	MAX	MIN	MAX	UNIT
fclock	Input clock frequency			25		25	MHz
tw	Pulse duration	CLK or CLR	20		20		ns
		Data enable (G1, G2)	17		17		
t <sub>su</sub>	Setup time	Data	10		10		ns
		CLR (inactive state)	10		10		
+.	Hold time	Data enable (G1, G2)	2		2		
th	Hold time Data		10		10		ns



# SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

# switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, R<sub>L</sub> = 400 $\Omega$ (see Figure 1)

	PARAMETER	TEST CONDITIONS	SN54173			S	N74173		UNIT
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency		25	35		25	35		MHz
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clear input	С <sub>L</sub> = 50 рF		18	27		18	27	ns
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output from clock input			28	43		28	43	
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clock input			19	31		19	31	ns
<sup>t</sup> PZH	Output enable time to high level		7	16	30	7	16	30	
<sup>t</sup> PZL	Output enable time to low level	1	7	21	30	7	21	30	ns
<sup>t</sup> PHZ	Output disable time from high level		3	5	14	3	5	14	ns
<sup>t</sup> PLZ	Output disable time from low level	C <sub>L</sub> = 5 pF	3	11	20	3	11	20	115



### recommended operating conditions

		SN	54LS173	BA	SN	SN74LS173A		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
ЮН	High-level output current			-1			-2.6	mA
IOL	Low-level output current			12			24	mA
Т <sub>А</sub>	Operating free-air temperature	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	7507.00		SN	154LS17	3A	SN	74LS17	3A	UNIT
	PARAMETER	TEST COL	NDITIONS <sup>†</sup>	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.7			0.8	V
VIK	Input clamp voltage	$V_{CC} = MIN,$	lı = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max,	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = MAX	2.4	3.4		2.4	3.1		V
M		$V_{CC} = MIN,$	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V
VOL	Low-level output voltage	V <sub>IL</sub> = 0.8 V,	I <sub>OL</sub> = 24 mA					0.35	0.5	V
1.0.0	Off-state (high-impedance state)	V <sub>CC</sub> = MAX,	V <sub>O</sub> = 2.7 V			20			20	V
IO(off)	output current	V <sub>IH</sub> = 2 V	V <sub>O</sub> = 0.4 V			-20			-20	v
lj	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V			0.1			0.1	mA
Iн	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V			20			20	μΑ
Ι <sub>Ι</sub>	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
IOS	Short-circuit output current§	$V_{CC} = MAX$		-30		-130	-30		-130	mA
ICC	Supply current	V <sub>CC</sub> = MAX,	See Note 4		19	30		19	24	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 4: I<sub>CC</sub> is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, G1, G2, and all data inputs grounded; and CLK and M at 4.5 V.

### timing requirements over recommended operating conditions (unless otherwise noted)

			SN54L	S173A	SN74L	UNIT	
			MIN	MAX	MIN	MAX	UNIT
fclock	clock Input clock frequency					25	MHz
tw	Pulse duration	CLK or CLR	25		25		ns
		Data enable (G1, G2)	35		35		
t <sub>su</sub>	Setup time	Data	17		17		ns
		CLR (inactive state)	10		10		
+.	Hold time	Data enable (G1, G2)	0		0		
th		Data	3		3		ns



# SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

# switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, R<sub>L</sub> = 667 $\Omega$ (see Figure 2)

	PARAMETER	TEST CONDITIONS	SN	54LS17	BA	SN	74LS173	BA	UNIT
	FARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f <sub>max</sub>	Maximum clock frequency		30	50		30	50		MHz
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clear input	C <sub>L</sub> = 45 pF		26	35		26	35	ns
tPLH	Propagation delay time, low-to-high-level output from clock input			17	25		17	25	
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clock input			22	30		22	30	ns
<sup>t</sup> PZH	Output enable time to high level			15	23		15	23	
<sup>t</sup> PZL	Output enable time to low level			18	27		18	27	ns
<sup>t</sup> PHZ	Output disable time from high level			11	20		11	20	ns
<sup>t</sup> PLZ	Output disable time from low level	C <sub>L</sub> = 5 pF		11	17		11	17	115



### SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS SDLS067A - OCTOBER 1976 - REVISED JUNE 1999

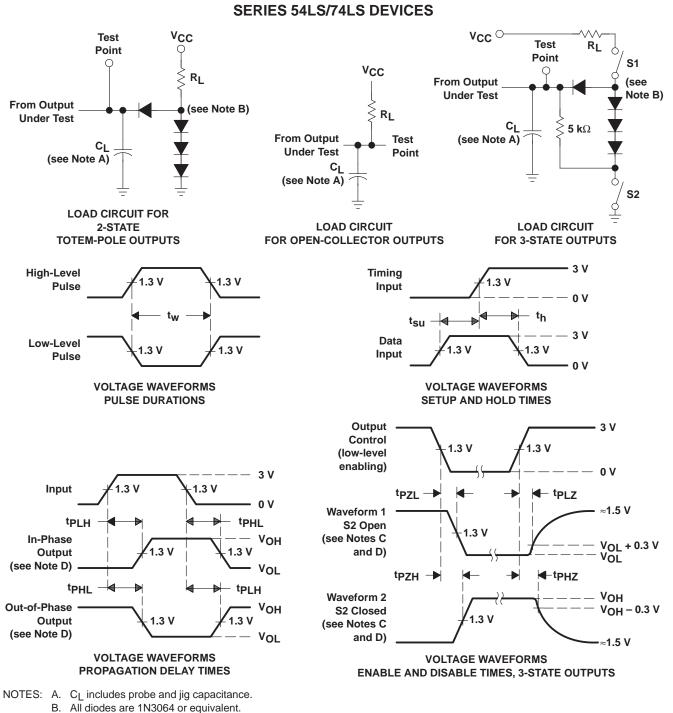
PARAMETER MEASUREMENT INFORMATION SERIES 54/74 AND 54S/74S DEVICES Vcc O  $(\Lambda \Lambda)$  $R_L$ Test Vcc Point Test **S**1 Point ۷сс From Output  $\bigcirc$ (see ξ  $R_L$ **Under Test** Note B) RL CL **From Output 1 k**Ω (see Note B) (see Note A) Under Test From Output Test **Under Test** Point Cı (see Note A) Cı (see Note A) S2 LOAD CIRCUIT LOAD CIRCUIT LOAD CIRCUIT FOR 2-STATE TOTEM-POLE OUTPUTS FOR OPEN-COLLECTOR OUTPUTS FOR 3-STATE OUTPUTS 3 V **High-Level** Timing 1.5 V 1.5 V 1.5 V Pulse Input 0 V t<sub>su</sub> 3 V Data Low-Level 1.5 V 1.5 V 1.5 V Input Pulse 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PULSE DURATIONS SETUP AND HOLD TIMES Output 3 V Control 1.5 V .5 V (low-level enabling) 0 V 3 V 5 1.5 V ۱. Input tPZL -<sup>t</sup>PLZ 0 V ≈1.5 V - tPHL **t**PLH Waveform 1 .5 V In-Phase (see Notes C Vон OL + 0.5 V and D) Output 1.5 V 1.5 V VOL (see Note D) Vol tPZH -<sup>t</sup>PHZ <sup>t</sup>PHL - tPLH VOH **Out-of-Phase** VOH Waveform 2 V<sub>OH</sub> – 0.5 V Output 1.5 V 1.5 V (see Notes C 1.5 V (see Note D) and D) VOL ≈1.5 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS** 

- NOTES: A.  $\ensuremath{\mathsf{C}}\xspace_L$  includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tPZL.
  - E. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub>  $\approx$  50  $\Omega$ , t<sub>f</sub> and t<sub>f</sub>  $\leq$  7 ns for Series 54/74 devices and t<sub>f</sub> and t<sub>f</sub>  $\leq$  2.5 ns for Series 54S/74S devices.
  - F. The outputs are measured one at a time with one input transition per measurement.

#### Figure 1. Load Circuits and Voltage Waveforms



SDLS067A – OCTOBER 1976 – REVISED JUNE 1999



PARAMETER MEASUREMENT INFORMATION

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tPZL. E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
- F. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub>  $\approx$  50  $\Omega$ , t<sub>f</sub>  $\leq$  15 ns, t<sub>f</sub>  $\leq$  6 ns. G. The outputs are measured one at a time with one input transition per measurement.

### Figure 2. Load Circuits and Voltage Waveforms





### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/36101BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36101BEA	Samples
JM38510/36101BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36101BFA	Samples
M38510/36101BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36101BEA	Samples
M38510/36101BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36101BFA	Samples
SN54173J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54173J	Samples
SN54LS173AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS173AJ	Samples
SN74LS173AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS173A	Samples
SN74LS173AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS173AN	Samples
SNJ54173J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54173J	Samples
SNJ54LS173AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 173AFK	Samples
SNJ54LS173AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS173AJ	Samples

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.



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## PACKAGE OPTION ADDENDUM

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF SN54LS173A, SN74LS173A :

Catalog : SN74LS173A

Military : SN54LS173A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

### TEXAS INSTRUMENTS

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### TUBE



### - B - Alignment groove width

### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
JM38510/36101BFA	W	CFP	16	1	506.98	26.16	6220	NA
M38510/36101BFA	W	CFP	16	1	506.98	26.16	6220	NA
SN74LS173AD	D	SOIC	16	40	507	8	3940	4.32
SN74LS173AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS173AN	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS173AFK	FK	LCCC	20	1	506.98	12.06	2030	NA

LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N\*\*) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/E 08/12

# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) –16x0,55 -14x1,27 -14x1,27 16x1,50 5,40 5.40 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 .55 Example 1. Solder Mask Opening (See Note E) -0,07 All Around

NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16



J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



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