MOTOROLA

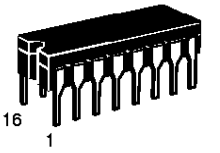
MC54/74F109

DUAL $\overline{JK}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

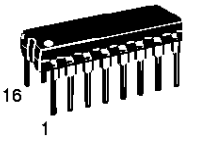
The MC54/74F109 consists of two high-speed, completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop (refer to F74 data sheet) by connecting the J and $\overline{K}$ inputs together.

DUAL $J\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

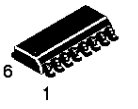
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

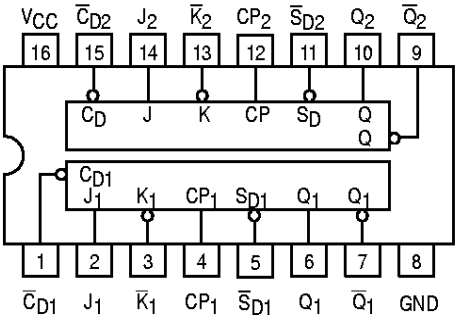


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Input		Output	
@ t_n		@ t_n + 1	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

Asynchronous Inputs:

LOW Input to $\overline{S}_D$ sets Q to HIGH level

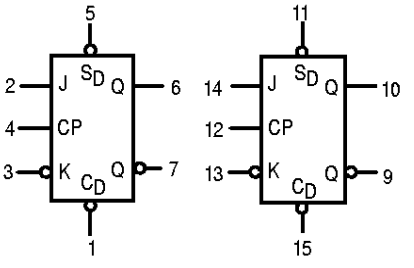
LOW Input to $\overline{C}_D$ sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

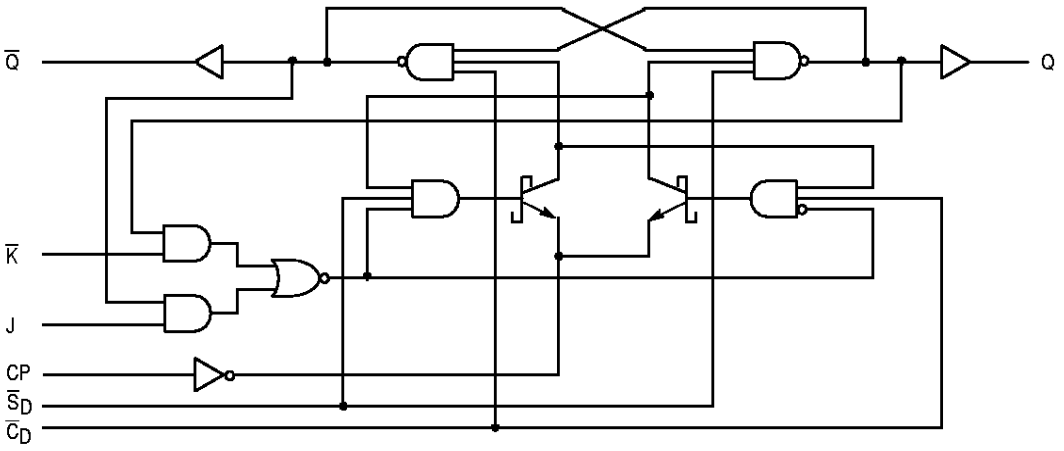
H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
t_n + 1 = Bit time after clock pulse

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM (one half shown)



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	–55	25	125	°C
		54	0	25	70	
I_{OH}	Output Current — High	54, 74			–1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				–1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = –1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	µA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current (J, $\overline{K}$ and CP Inputs)				–0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				–1.8	mA		
I_{OS}	Output Short Circuit Current (Note 2)		–60		–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			11.7	17	mA	V_{CP} = 0 V	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			54F T_A = –55°C to +125°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF		74F T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 10%, C_L = 50 pF		Unit
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	125		70		90		MHz
t_{PLH}	Propagation Delay	3.8	5.3	7.0	3.8	9.0	3.8	8.0	ns
t_{PHL}	CP_n to Q_n or $\overline{Q}_n$	4.4	6.2	8.0	4.4	10.5	4.4	9.2	
t_{PLH}	Propagation Delay	2.5	5.2	7.0	2.5	9.0	2.5	8.0	ns
t_{PHL}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.5	7.0	9.0	3.5	11.5	3.5	10.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A = –55°C to +125°C, V_{CC} = 5.0 V ± 10%		74F T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 10%		Unit
		Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	3.0			3.0		3.0		ns
$t_s(L)$	J_n or $\overline{K}_n$ to CP_n	3.0			3.0		3.0		
$t_h(H)$	Hold Time, HIGH or LOW	1.0			1.0		1.0		
$t_h(L)$	J_n or $\overline{K}_n$ to CP_n	1.0			1.0		1.0		
$t_w(H)$	CP_n Pulse Width, HIGH	4.0			4.0		4.0		ns
$t_w(L)$	or LOW	5.0			5.0		5.0		
$t_w(L)$	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.0			4.0		4.0		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			2.0		2.0		ns