

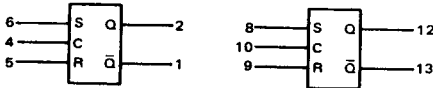
DUAL R-S FLIP-FLOP
WITH NEGATIVE CLOCK

MECL II MC1000/1200 series

MC1015
MC1215

Two dc Set-Reset flip-flops with a negative clock input provided for each flip-flop. This unit is useful as a dual storage element and may be teamed with the MC1014/MC1214 for shift register functions with a minimum number of packages.

POSITIVE LOGIC



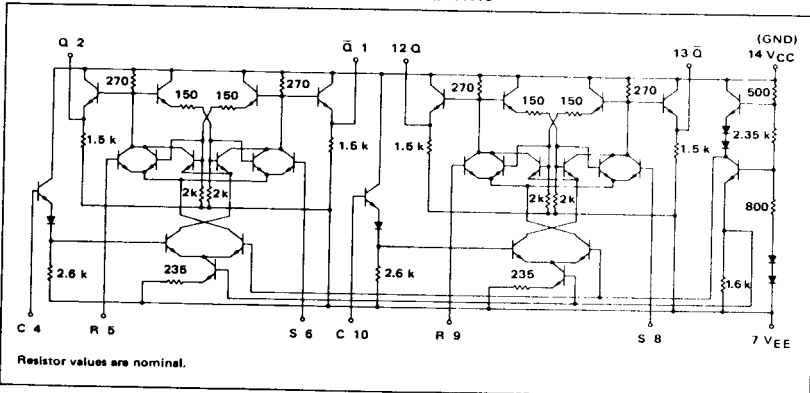
DC Input Loading Factor : C = 1; S, R = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

TRUTH TABLE

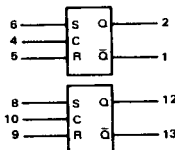
R	S	C	Q ⁿ⁺¹
0	1	0	1
1	0	0	0
0	0	0	Q ⁿ
1	1	0	N.D.
*	*	1	Q ⁿ

* Either State
N.D. = Not Defined

CIRCUIT SCHEMATIC



MC1015, MC1215 (continued)



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1215 Test Limits						MC1015 Test Limits						Unit		
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C				
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	-	-	-	36	-	-	-	mA	
Input Current	I_{in}	4	-	-	-	100	-	-	-	-	-	-	100	-	-	-	μ A
		5	-	-	-	150	-	-	-	-	-	-	150	-	-	-	μ A
		6	-	-	-	150	-	-	-	-	-	-	150	-	-	-	μ A
Input Leakage Current	Inputs*	4, 5, 6	-	-	-	0.2	-	1.0	-	-	-	0.2	-	1.0	-	μ A	
'Q' Logical '1' Output Voltage	V_{OH}^1	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
'Q' Logical '0' Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
'Q-bar' Logical '1' Output Voltage	V_{OH}^1	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
'Q-bar' Logical '0' Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max		
Clock Inputs Propagation Delay	t_{4-1}	1	6.0	10.0	6.0	10.0	8.0	12.0	ns	6.0	10.0	6.0	10.0	7.0	11.0	ns	
		1	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5		
		2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5		
		2	6.0	10.0	6.0	10.0	8.0	12.0		6.0	10.0	6.0	10.0	7.0	11.0		
Rise Time	t_{1+}	1															
		2															
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11.0		5.0	8.5	5.0	8.5	6.0	9.5		
		2	5.0	8.5	5.0	8.5	7.0	11.0		5.0	8.5	5.0	8.5	6.0	9.5		
Set-Reset Inputs Propagation Delay	t_{6+1}	1	5.0	8.0	5.0	8.0	7.0	11.0	ns	5.0	8.0	5.0	8.0	6.0	9.0	ns	
		1															
		2															
Rise Time	t_{5+2}	1	6.0	9.0	6.0	9.0				6.0	9.0	6.0	9.0	7.0	10.0		
		1															
		2	6.0	9.0		9.0					9.0		9.0				
Fall Time	t_{1-}	1	5.0	8.0		8.5	8.0	11.5			8.5		8.5				
		2	5.0	8.0		8.5	8.0	11.5			8.5		8.5				

* Individually test each input using the pin connections shown.

¹ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

APPLICATIONS INFORMATION

The MC1015/MC1215 is a dual R-S flip-flop with a negative clock input for each flip-flop. An extra level of gating is accomplished with only 2.0 ns increase in propagation delay. This device may be used with the MC1014/MC1214 positive-clock R-S flip-flop in a single-phase clocked master-slave type of shift register as shown in Figure 1.

		TEST VOLTAGE/CURRENT VALUES						
		$V_{dc} \pm 1.0\%$					± 50 mV	mAdc
@ Test Temperature		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	V_{BB}	I_L	
MC1215	-55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5	
MC1015	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-1.115	-2.5	

		TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:							
Characteristic	Symbol	Pin Under Test	$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	V_{BB}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 6, 7, 8, 9	-	-	14
Input Current	I_{in}	5 6	-	-	4 5 6	5, 6, 7, 8, 9, 10 4, 6, 7, 8, 9, 10 4, 5, 7, 8, 9, 10	-	-	14
Input Leakage Current	Inputs*	4, 5, 6	-	-	-	4, 5, 6, 7, 8, 9, 10	-	-	14
"Q" Logical "1" Output Voltage	V_{OH1}	2	4	6	-	5, 7, 8, 9, 10	5	2	14
"Q" Logical "0" Output Voltage	V_{OL}	2	4	5	-	4, 7, 8, 9, 10	6	-	14
"Q" Logical "1" Output Voltage	V_{OH1}	1	4	5	-	4, 7, 8, 9, 10	6	1	14
"Q" Logical "0" Output Voltage	V_{OL}	1	4	6	-	5, 7, 8, 9, 10	5	-	14
Switching Times (Fan-Out = 3)			$V_{IL\ max} + 1.2$ Vdc	Pulse In	Pulse Out	$V_{EE} = -4.0$ Vdc			+1.2V
Clock Inputs									
Propagation Delay	t_{4-1-}	1	-	4	1	5, 6, 7, 8, 9, 10	-	-	14
	t_{4-1+}	1	-	-	1	-	-	-	-
	t_{4-2+}	2	-	-	2	-	-	-	-
	t_{4-2-}	2	-	-	2	-	-	-	-
Rise Time	t_{1+}	1	-	-	1	-	-	-	-
	t_{2+}	2	-	-	2	-	-	-	-
Fall Time	t_{1-}	1	-	-	1	-	-	-	-
	t_{2-}	2	-	-	2	-	-	-	-
Set-Reset Inputs									
Propagation Delay	t_{6+1-}	1	4	6	1	7, 8, 9, 10	-	-	14
	t_{5+1+}	1	-	5	1	-	-	-	-
	t_{6+2+}	2	-	6	2	-	-	-	-
	t_{5+2-}	2	-	5	2	-	-	-	-
Rise Time	t_{1+}	1	-	6	1	-	-	-	-
	t_{2+}	2	-	-	2	-	-	-	-
Fall Time	t_{1-}	1	-	-	1	-	-	-	-
	t_{2-}	2	-	-	2	-	-	-	-

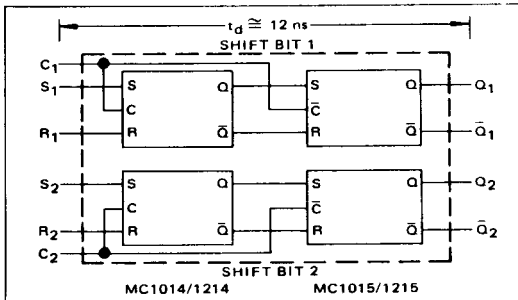
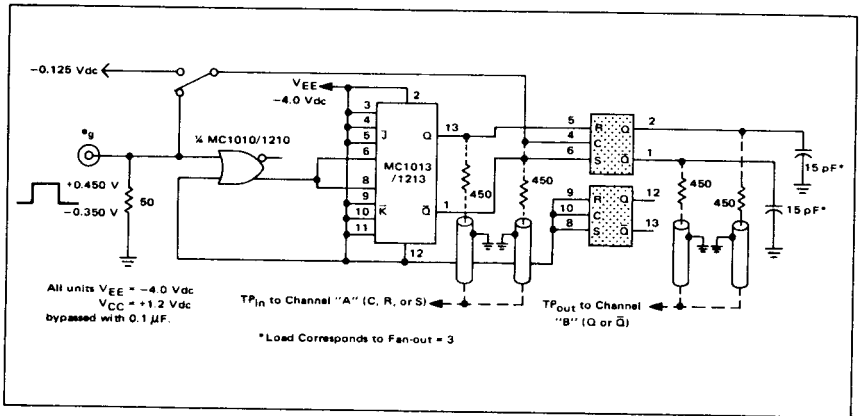


FIGURE 1 - MC1014/MC1214 AND MC1015/MC1215 CONNECTED TO MAKE TWO MASTER-SLAVE SHIFT REGISTER ELEMENTS

MC1015, MC1215 (continued)

SWITCHING TIME TEST CIRCUIT T_A = 25°C



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

