FAIRCHILD
A Schlumberger Company

11C06
750 MHz D-Type Flip-Flop

11C ECL Product

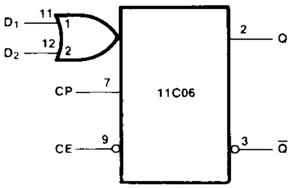
Description

The F11C06 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 750 MHz. Designed primarily for high-speed prescaling, it can also be used in any application which does not require preset inputs. The circuit is voltage-compensated, which makes input thresholds and output levels insensitive to V_{EE} variations. Complementary Q and $\overline{Q}$ outputs are provided, as are two Data inputs, Clock and Clock Enable inputs. The 11C06 is pin-compatible with the Motorola MC1690L but is a higher-frequency replacement.

Pin Names

D_n	Data Input
CP	Clock Input
$\overline{CE}$	Clock Enable (Active LOW)
$Q, \overline{Q}$	Outputs

Logic Symbol



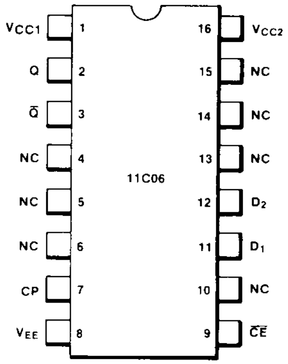
V_{CC1} = Pin 1 (1)
V_{CC2} = Pin 16 (16)
V_{EE} = Pin 8 (8)
( ) = Flatpak

Ordering Information

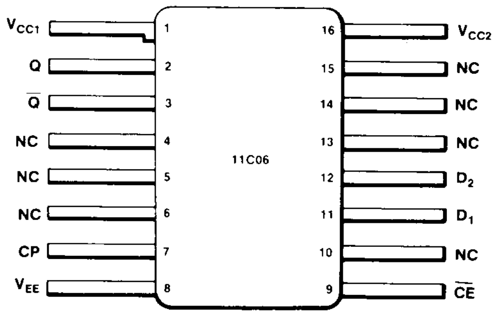
Package	Outline	Order Code
Ceramic DIP	4J	DC
Flatpak	3L	FC

Connection Diagram

16-Pin DIP (Top View)



16-Pin Flatpak (Top View)



Truth Table

$\overline{CE}$	CP	D	Q_n
L	L	X	Q_{n-1}
L	H	X	Q_{n-1}
L	$\uparrow$	L	L
L	$\uparrow$	H	H
H	X	X	Q_{n-1}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
$\uparrow$ = LOW to HIGH Transition
Q_{n-1} = Previous State

Absolute Maximum Ratings Above which the useful life may be impaired

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	-7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	-50 mA
Operating Range	-5.7V to -4.7V
Lead Temperature (Soldering 10 sec.)	300°C

Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Ambient Temperature (T_A)
Min	Typ	Max	
−5.7V	−5.2V	−4.7V	0°C to +75°C

DC Characteristic: V_{EE} = -5.2V, V_{CC} = GND

Symbol	Characteristic	Min	Typ	Max	Unit	T_A	Condition
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C +25°C +75°C	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ per Truth Table Loading 50Ω to -2V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1635 -1620 -1595	mV	0°C +25°C +75°C	
V_{OHC}	Output Voltage High	-1020 -980 -920			mV	0°C +25°C +75°C	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$ for D_n Inputs Loading 50Ω to -2V
V_{OLC}	Output Voltage LOW			-1615 -1600 -1575	mV	0°C +25°C +75°C	
V_{IH}	Input Voltage HIGH	-1135 -1095 -1035		-840 -810 -720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1500 -1485 -1460	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs
I_{IH}	Input Current HIGH Clock Input Data Input			 250 270	μA	+25°C	$V_{IN} = V_{IH(Max)}$
I_{IL}	Input Current LOW	0.5			μA	+25°C	$V_{IN} = V_{IH(Min)}$
I_{EE}	Power Supply Current	-59	-40		mA	+25°C	All Inputs Open

AC Characteristics: V_{EE} = -5.2V, V_{CC} = GND, T_A = 25°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_{PHL}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	See Figure 1
t_{PHL}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	
t_{TLH}	Transition Time 20% to 80%	0.5	0.8	1.0	ns	
t_{THL}	Transition Time 80% to 20%	0.5	0.8	1.0	ns	
t_S	Set-up Time		0.2		ns	
t_H	Hold Time		0.2		ns	
$f_{TOG(MAX)}$	Toggle Frequency (CP)	650	750		MHz	See Figure 2, Note

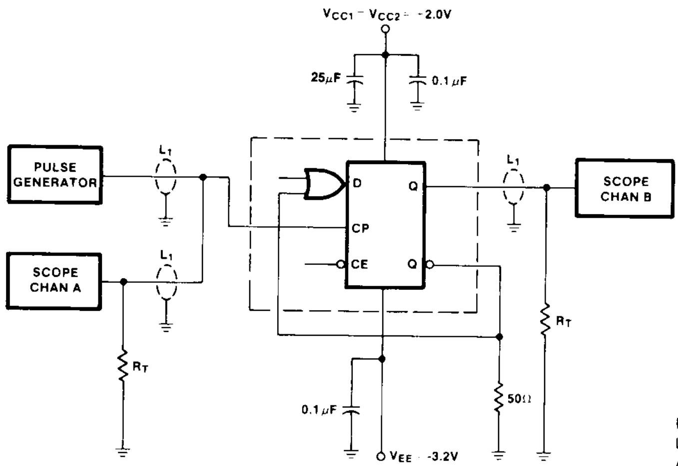
Note: The device is guaranteed for f_{TOG}(CP) ≥ 600 MHz, f_{TOG} (CE) ≥ 550 MHz over the 0°C to +75°C temperature range.

Functional Description

While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master-slave changes when the clock has slow rise or fall times.

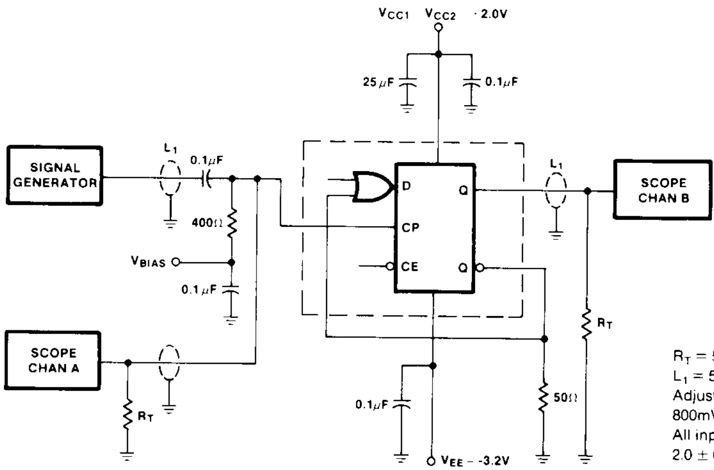
The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the Dual In-Line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should go HIGH while CP is still HIGH.

Figure 1 Propagation Delay (CP to Q)



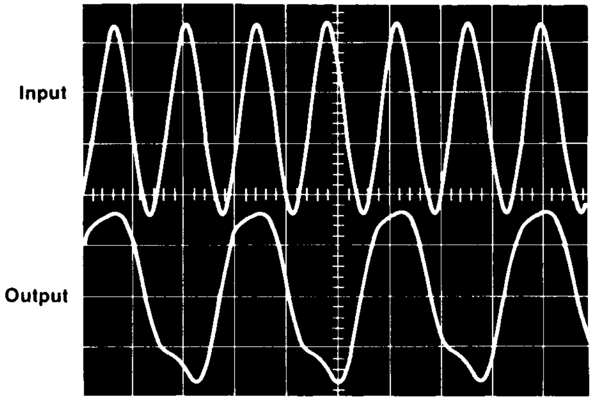
R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
All input transition times are
2.0 ± 0.2 ns

Figure 2 Toggle Frequency Test Circuit



R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
Adjust V_{BIAS} for +0.7V baseline of
800mV peak-to-peak sinewave input
All input transition times are
2.0 ± 0.2 ns

Typical Waveforms



700 MHz Operation

Horizontal Scale = 1.0 ns/div

Vertical Scale = 200 mV/div