

# SN54ALS109A, SN54AS109, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198A – APRIL 1982 – REVISED DECEMBER 1994

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

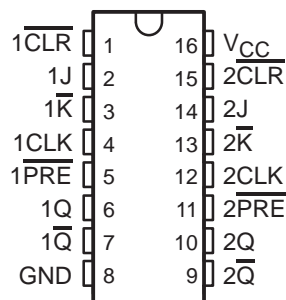
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS109A	50	6
SN54AS109, SN74AS109A	129	29

## description

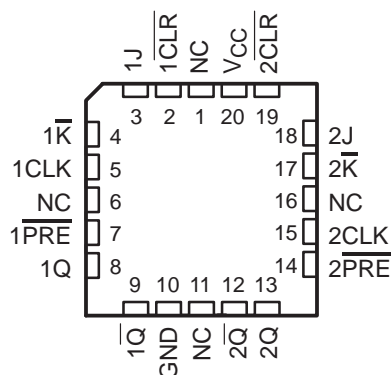
These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the J and  $\overline{\text{K}}$  inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and  $\overline{\text{K}}$  inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\overline{\text{K}}$  and tying J high. They also can perform as D-type flip-flops if J and  $\overline{\text{K}}$  are tied together.

The SN54ALS109A and SN54AS109 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS109A and SN74AS109A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS109A, SN54AS109 . . . J PACKAGE  
SN74ALS109A, SN74AS109A . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS109A, SN54AS109 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

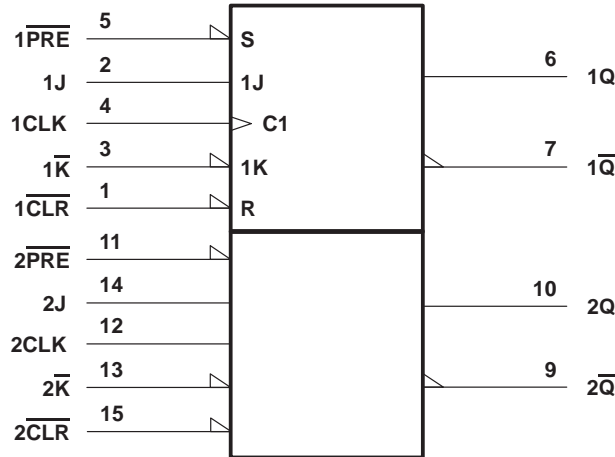
INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q0	$\overline{\text{Q}}0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{\text{Q}}0$

<sup>†</sup> The output levels in this configuration are not specified to meet the minimum levels for  $V_{\text{OH}}$  if the lows at  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are near  $V_{\text{IL}}$  maximum. Furthermore, this configuration is nonstable; that is, it does not persist when either  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS109A	-55°C to 125°C
SN74ALS109A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS109A			SN74ALS109A			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
$V_{IH}$	High-level input voltage	2			2			V		
$V_{IL}$	Low-level input voltage			0.7			0.8	V		
$I_{OH}$	High-level output current			-0.4			-0.4	mA		
$I_{OL}$	Low-level output current			4			8	mA		
$f_{clock}$	Clock frequency	0		30	0		34	MHz		
$t_w$	Pulse duration	PRE or CLR low		15			15	ns		
		CLK high		16.5			14.5			
		CLK low		16.5			14.5			
$t_{su}$	Setup time before CLK↑	Data		15			15	ns		
		PRE or CLR inactive		10			10			
$t_h$	Hold time after CLK↑	Data		0			0	ns		
$T_A$	Operating free-air temperature			-55		125		0	70	°C

# SN54ALS109A, SN54AS109, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS109A		SN74ALS109A		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.5		-1.5	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$		V	
$V_{OL}$	$V_{CC} = 4.5\text{ V}$			0.25	0.4	0.25	0.4	V
						0.35	0.5	
$I_I$	CLK, J, or $\overline{K}$ $\overline{PRE}$ or $\overline{CLR}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1		0.1	mA
					0.2		0.2	
$I_{IH}$	CLK, J, or $\overline{K}$ $\overline{PRE}$ or $\overline{CLR}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20		20	$\mu\text{A}$
					40		40	
$I_{IL}$	CLK, J, or $\overline{K}$ $\overline{PRE}$ or $\overline{CLR}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-0.2		-0.2	mA
					-0.4		-0.4	
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-20		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , See Note 1		2.4	4		2.4	4	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J,  $\overline{K}$ , CLK, and  $\overline{PRE}$  grounded, then with J,  $\overline{K}$ , CLK, and  $\overline{CLR}$  grounded.

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			30		34		MHz
$t_{\text{PLH}}$	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	17	3	13	ns
$t_{\text{PHL}}$			5	17	5	15	
$t_{\text{PLH}}$	CLK	Q or $\overline{Q}$	5	21	5	16	ns
$t_{\text{PHL}}$			5	20	5	18	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS109	-55°C to 125°C
SN74AS109A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54AS109			SN74AS109A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-2			-2	mA
$I_{OL}$	Low-level output current			20			20	mA
$f_{clock}^*$	Clock frequency	0		90	0		105	MHz
$t_w^*$	Pulse duration	PRE or CLR low		4	4		ns	
		CLK high		4	4			
		CLK low		5.5	5.5			
$t_{su}^*$	Setup time before CLK↑	Data		5.5	5.5		ns	
		PRE or CLR inactive		2	2			
$t_h^*$	Hold time after CLK↑	Data		0	0		ns	
$T_A$	Operating free-air temperature	-55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS109			SN74AS109A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ , $I_I = -18 mA$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -2 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5 V$ , $I_{OL} = 20 mA$		0.25	0.5		0.25	0.5	V
$I_I$	$V_{CC} = 5.5 V$ , $V_I = 7 V$			0.1			0.1	mA
$I_{IH}$	CLK, J, or K	$V_{CC} = 5.5 V$ , $V_I = 2.7 V$		20		20	μA	
	PRE or CLR			40		40		
$I_{IL}$	CLK, J, or K	$V_{CC} = 5.5 V$ , $V_I = 0.4 V$		-0.5		-0.5	mA	
	PRE or CLR			-1.8		-1.8		
$I_{O}^{\S}$	$V_{CC} = 5.5 V$ , $V_O = 2.25 V$	-30		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5 V$ , See Note 1		11.5	17		11.5	17	mA

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.



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**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS109		SN74AS109A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			90		105		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	9	2	8	ns
t <sub>PHL</sub>			3.5	11.5	3.5	10.5	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	3.5	10	2.5	9	ns
t <sub>PHL</sub>			4.5	10.5	3.5	9	

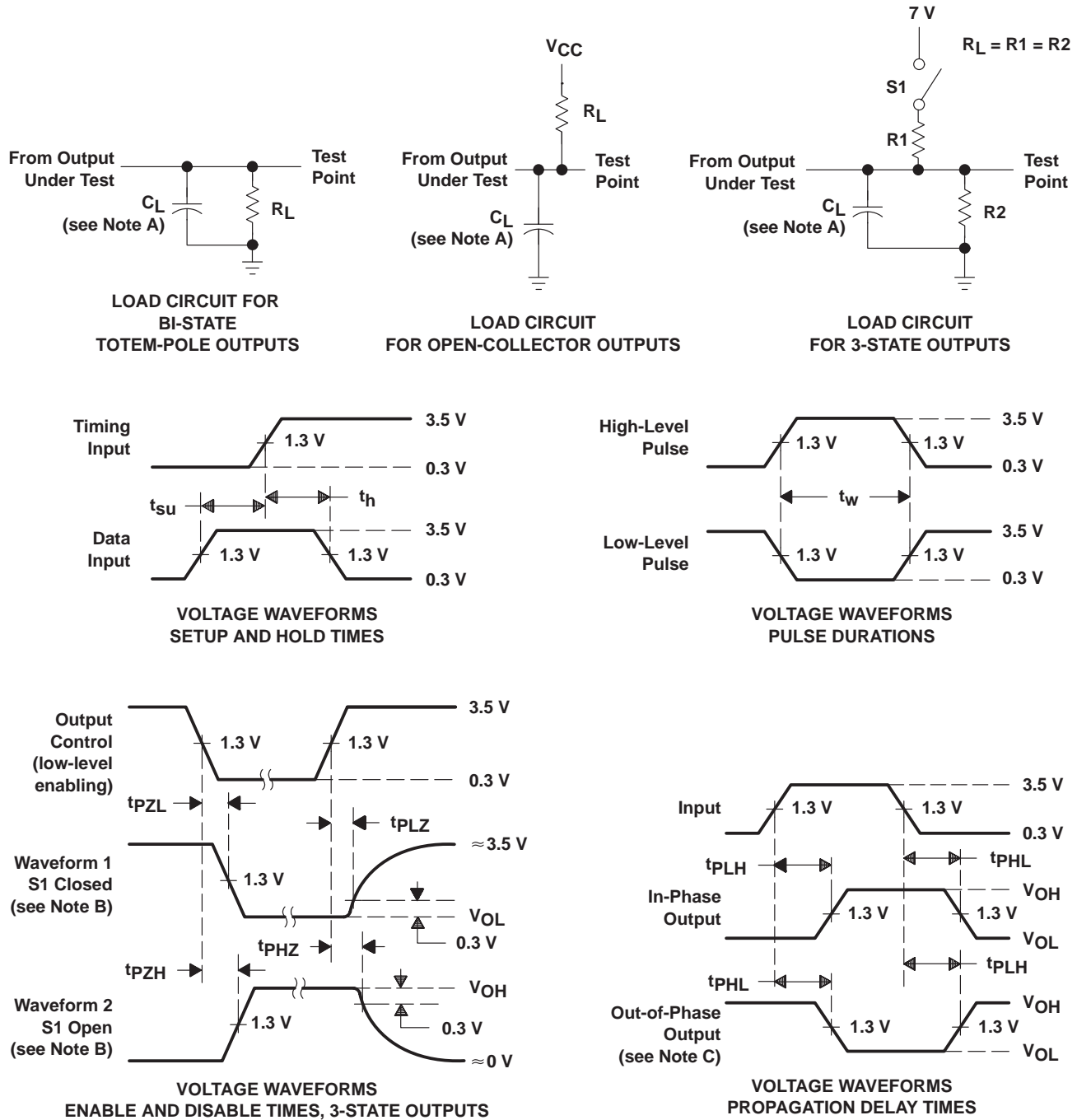
\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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