



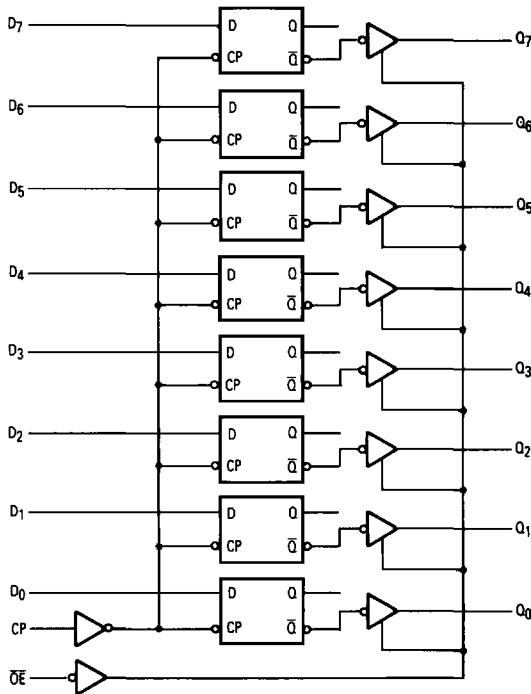
Octal D-Type Positive Edge-Triggered Flip-Flop With 3-State Inverted Outputs

**ELECTRICALLY TESTED PER:
MIL-M-38510/34106**

The 54F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus Oriented Applications

LOGIC DIAGRAM



Military 54F534



AVAILABLE AS:

- 1) JAN: JM38510/34106BXA
- 2) SMD: *
- 3) 883C: 54F534/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2
*Call Factory for latest update**

PIN ASSIGNMENTS

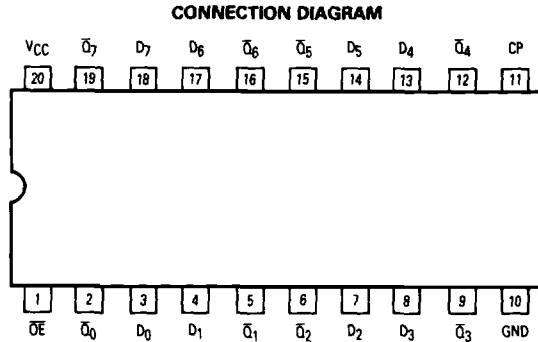
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
\overline{OE}	1	1	1	VCC
$\overline{Q_0}$	2	2	2	OPEN
D ₀	3	3	3	VCC
D ₁	4	4	4	VCC
$\overline{Q_1}$	5	5	5	OPEN
$\overline{Q_2}$	6	6	6	OPEN
D ₂	7	7	7	VCC
D ₃	8	8	8	VCC
$\overline{Q_3}$	9	9	9	OPEN
GND	10	10	10	GND
CP	11	11	11	VCC
$\overline{Q_4}$	12	12	12	OPEN
D ₄	13	13	13	VCC
D ₅	14	14	14	VCC
$\overline{Q_5}$	15	15	15	OPEN
$\overline{Q_6}$	16	16	16	OPEN
D ₆	17	17	17	VCC
D ₇	18	18	18	VCC
$\overline{Q_7}$	19	19	19	OPEN
VCC	20	20	20	VCC

**BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX**

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TRUTH TABLE			
Inputs		Outputs	
D _n	CP	OE	Q _n
H		L	H
L		L	L
X	X	H	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance

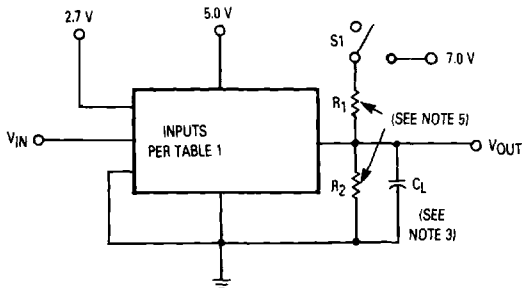


FUNCTIONAL DESCRIPTION

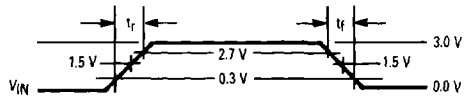
The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP)

transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

AC TEST CIRCUIT

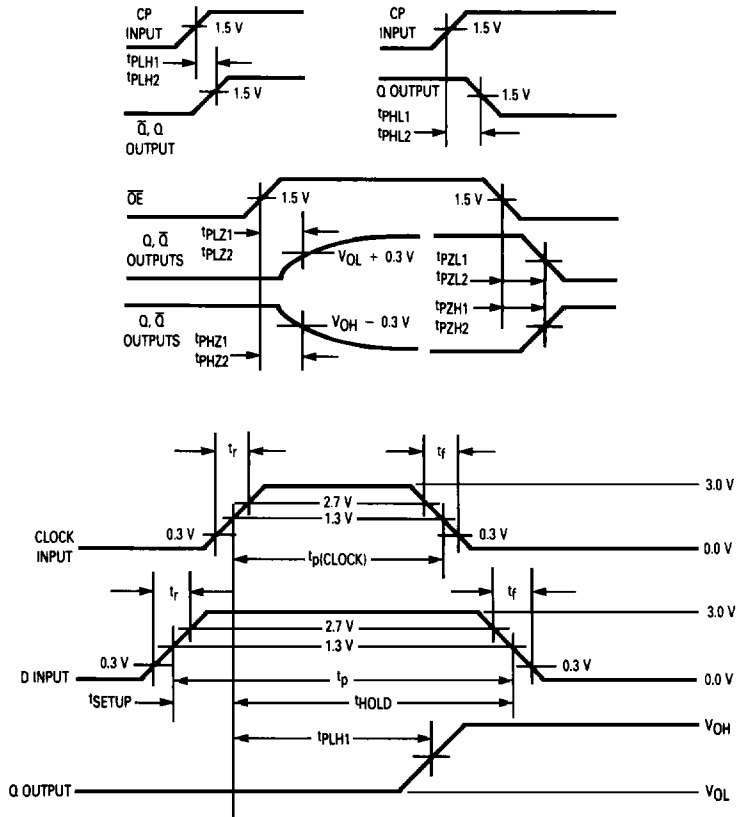


Test Type	S1
t _{PLH}	open
t _{PHL}	open
t _{PHZ}	open
t _{PZH}	open
t _{PLZ}	closed
t _{PZL}	closed



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WAVEFORMS



NOTES:

1. $t_r = t_f \approx 2.5$ ns.
2. PRR as in table 1, duty cycle $50 \pm 15\%$.
3. When testing f_{MAX} , the output frequency shall be 1/2 the input frequency.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
VOH	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, V _{IL} = 0.8 V (all inputs), CP = (See Note 6).
VOL	Logical "0" Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} = 20 mA, V _{IH} = 2.0 V (all inputs), CP = (See Note 6), OE = 0.8 V.
VIC	Input Clamping Voltage		-1.2					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V (all inputs).
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V (all inputs).
I _{OD}	Diode Current	35		35		35		mA	V _{CC} = 4.5 V, V _{IN} = 5.5 V (all inputs), OE = 0 V, CP = (See Note 6), V _{OUT} = 2.5 V.
I _{IL}	Logical "0" Input Current	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V (all inputs).
I _{OS}	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), V _{OUT} = 0 V, CP = (See Note 6).
I _{IOZH}	Output Off Current High		50		50		50	μA	V _{CC} = 5.5 V, V _{IN} = 2.7 V (all inputs), V _{OUT} = 2.7 V, OE = 2.0 V, CP = (See Note 6).
I _{IOZL}	Output Off Current Low		-50		-50		-50	μA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), V _{OUT} = 0.5 V, OE = 2.0 V, CP = (See Note 6).
I _{CCZ}	Power Supply Current Off		86		86		86	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, (Repeat at) V _{CC} = 5.5 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL2}	Propagation Delay /Data-Output CP to \overline{Q}_n	4.0	8.5	4.0	11	4.0	11	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH2}	Propagation Delay /Data-Output CP to \overline{Q}_n	4.0	8.5	4.0	10.5	4.0	10.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLZ2}	Propagation Delay /Data-Output OE to \overline{Q}_n	1.5	5.5	1.5	7.5	1.5	7.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PHZ2}	Propagation Delay /Data-Output OE to \overline{Q}_n	1.5	7.0	1.5	8.0	1.5	8.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PZL2}	Propagation Delay /Data-Output OE to \overline{Q}_n	2.0	7.5	2.0	10	2.0	10	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PZH2}	Propagation Delay /Data-Output OE to \overline{Q}_n	2.0	11.5	2.0	14	2.0	14	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
f _{MAX}	Maximum Clock Frequency	80		60		60		MHz	V _{CC} = 5.0 V, C _L = 50 pF, (See Note 7).
t _{s(H)}	Setup Time, HIGH D _n to CP	2.5		2.5		2.5		ns	V _{CC} = 5.0 V, C _L = 50 pF, (See Note 7).
t _{s(L)}	Setup Time, LOW D _n to CP	2.0		2.0		2.0		ns	V _{CC} = 5.0 V, C _L = 50 pF, (See Note 7).
t _{h(H)}	Hold Time, HIGH D _n to CP	2.0		2.0		2.0		ns	V _{CC} = 5.0 V, C _L = 50 pF, (See Note 7).
t _{h(L)}	Hold Time, LOW D _n to CP	2.5		2.5		2.5		ns	V _{CC} = 5.0 V, C _L = 50 pF, (See Note 7).

NOTES:

1. V_{IN} = Input pulse has the following characteristics: t_r = t_f ≤ 2.5 ns, PRR ≤ 1.0 MHz.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. R₁ = R₂ = 499 Ω ± 5.0%.
6. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to CP, then make measurement.
7. This is for information only, no test required.
8. f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be 1/2 the input frequency.