CMOS

LATCHES/FLIP-FLOPS

Item	Function	DEVICE NO.	Data Inputs	Common Clear	Enable/Clock Inputs (Level)	Required Enable/Clock Pulse Width-ns (Typ) V_{DD} = 10V	Enable/Clock to Q Delay-ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
1	Dual JK Flip-Flop	**4027B**	JK	RS	H	35	45	C21	4L,6B,9B
2	Dual D Flip-Flop	**4013B**	D	RS	H	30	38	C22	3I,6A,9A
3	Quad D Flip-Flop	**40175B**	D	X	H	10	35	C23	4L,6B,9B
4	Quad D Flip-Flop w/3-State Ouptuts	**4076B**	D	MR	L	35	35	C110	4L,6B,9B
5	Hex D Flip-Flop	**40174B**	D	X	H	10	35	C24	4L,6B,9B
6	4-Bit Latch	**4042B**	D	—	H	16	66	C25	4L,6B,9B
7	4-Bit Latch	**4043B**	RS	RS	H	14	30	C26	4L,6B,9B
8	4-Bit Latch	**4044B**	RS	RS	H	14	30	C27	4L,6B,9B
9	Dual 4-Bit Address Latch	**4723B**	D	X	L	20	50	C28	4L,6B,9B
10	8-Bit Address Latch	**4724B**	D	X	L	20	40	C29	4L,6B,9B
11	BCD-to-7-Seg Latch/Decoder/Dvr	**4511B**	D	X	L	14	90	C111	4L,6B,9B
12	BCD-to-7-Seg Latch/Decoder/Dvr for Liquid Crystal	**4543B**	D	X	H	40	200	C112	4L,6B,9B
13	BCD-to-7-Seg Latch/Decoder Dvr w/Ripple Blanking	**4734B**	D	X	L	14	90	C114	7D,9M

MULTIPLEXERS

Item	Function	DEVICE NO.	Enable Inputs	True Output	Select Delay ns (Typ) V_{DD} = 10V	Enable Delay ns (Typ) V_{DD} = 10V	Data Delay ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
14	Quad 2-Input	**4019B**	—	X	37	—	37	C30	4L,6B,9B
15	Quad 2-Input	**4519B**	—	X	50	—	50	C31	4L,6B,9B
16	Dual 4-Input	**4539B**	X	X	88	53	71	C32	4L,6B,9B
17	Single 8-Input	**4512B**	X	3-State	85	45	75	C33	4L,6B,9B

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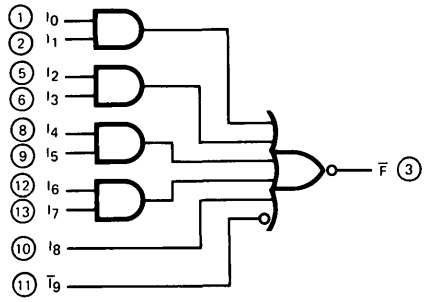
DIGITAL-CMOS

C19
4086B



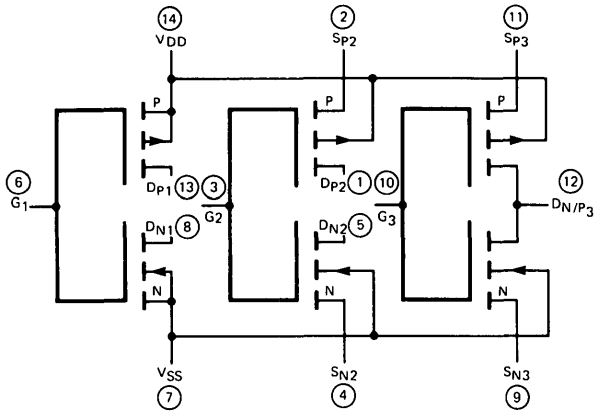
$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4 \bullet I_5 + I_6 \bullet I_7 + I_8 + I_9}$

NOTE

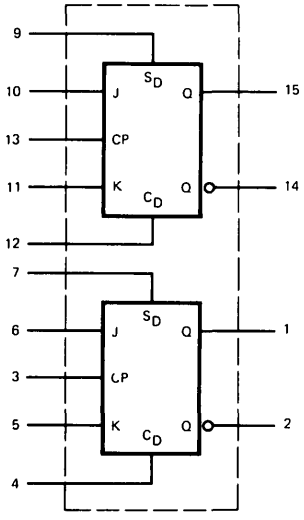
A HIGH on I_8 or a LOW on I_9 forces the output ($\overline{F}$) LOW

V_{DD} = Pin 14 V_{SS} = Pin 7 NC = Pin 4

C20
4007B

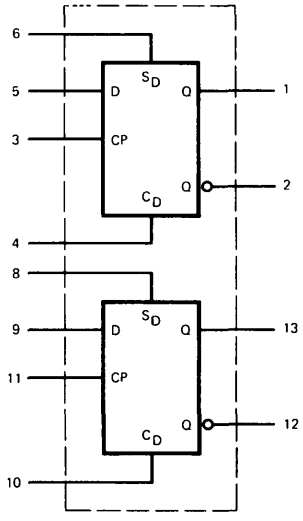


C21
4027B



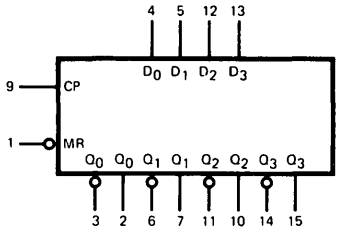
V_{DD} = Pin 16
V_{SS} = Pin 8

C22
4013B



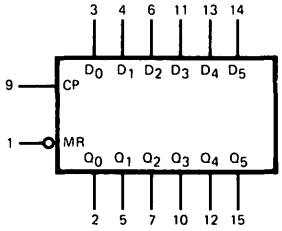
V_{DD} = Pin 14
V_{SS} = Pin 7

C23
40175B



V_{DD} = Pin 16
V_{SS} = Pin 8

C24
40174B



V_{DD} = Pin 16
V_{SS} = Pin 8

NOTE The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-Line Packages

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