54H/74H102

JK EDGE-TRIGGERED FLIP-FLOP

(With AND Inputs)

DESCRIPTION — The '102 is a high speed JK negative edge-triggered flip-flop. It features gated JK inputs and an asynchronous Clear input. The AND gate inputs are inhibited while the clock input is LOW. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

TRUTH TABLE

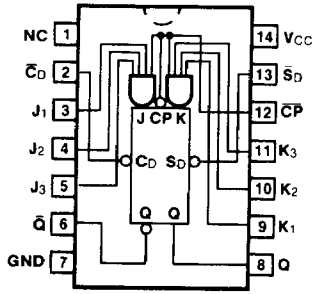
INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

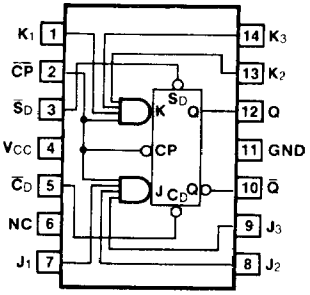
$J = (J_{1A} \bullet J_{1B}) + (J_{2A} \bullet J_{2B})$
$K = (K_{1A} \bullet K_{1B}) + (K_{2A} \bullet K_{2B})$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAMS

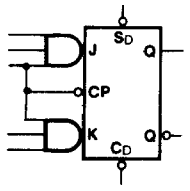
PINOUT A



PINOUT B



LOGIC SYMBOL



V_{CC} = Pin 14 (4)
GND = Pin 7 (11)

ORDERING CODE: See Section 9

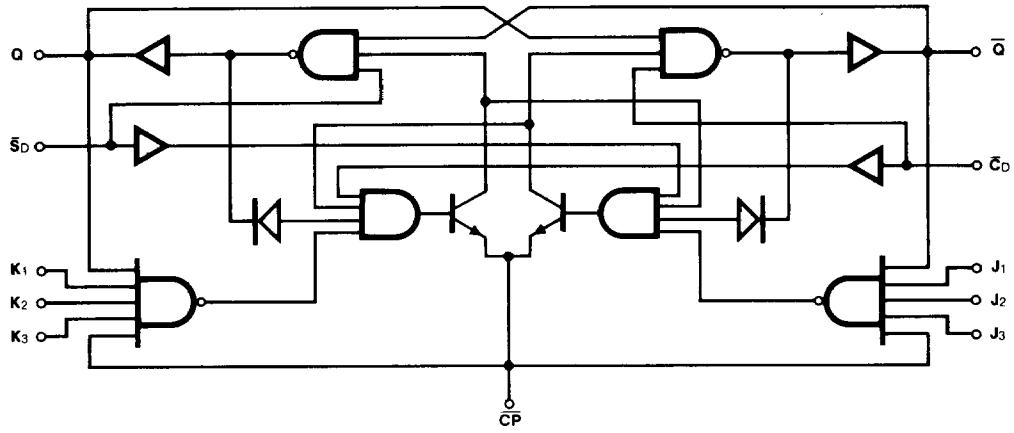
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10% T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H102PC		9A
Ceramic DIP (D)	A	74H102DC	54H102DM	6A
Flatpak (F)	B	74H102FC	54H102FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H HIGH/LOW
J_1, J_2, J_3 K_1, K_2, K_3	Data Inputs	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0*/3.0
$\overline{C}_D$	Direct Clear Input (Active LOW)	2.5/1.25
$\overline{S}_D$	Direct Set Input (Active LOW)	2.5/1.25
Q, $\overline{Q}$	Outputs	12.5/12.5

*$\overline{CP}$ Sourcing Current, see DC Characteristics Table

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current at $\overline{CP}$	0	-1.0	mA	V_{CC} = Max, V_{CP} = 2.4 V
I_{CC}	Power Supply Current		38	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF R_L = 280 Ω Min	54/74H C_L = 25 pF R_L = 280 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		15 20	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_D$ to Q or $\overline{Q}$		12 20	ns	$V_{CP} \geq$ 2.0 V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_D$ to Q or $\overline{Q}$		12 35	ns	$V_{CP} \leq$ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	10 13		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0 0		ns	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	10 15		ns	Fig. 3-9
t_w (L)	$\overline{C}_D$ or $\overline{S}_D$ Pulse Width LOW	16		ns	Fig. 3-10