

SN54298, SN54LS298, SN74298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

SDLS098 MARCH 1974 - REVISED MARCH 1988

- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

- Applications:
Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability

Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities

description

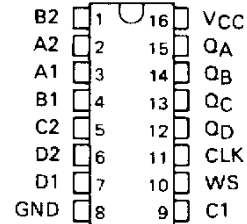
These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54157/SN74157 or SN54LS157/SN74LS157 and SN54175/SN74175 or SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

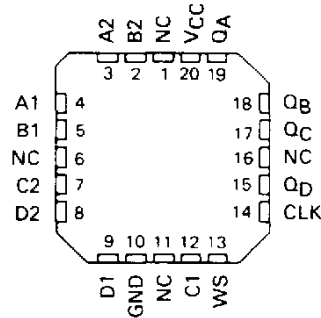
Typical power dissipation is 195 milliwatts for the '298 and 65 milliwatts for the 'LS298. SN54298 and SN54LS298 are characterized for operation over the full military temperature range of -55°C to 125°C ; SN74298 and SN74LS298 are characterized for operation from 0°C to 70°C .

SN54298, SN54LS298 . . . J OR W PACKAGE
SN74298 . . . N PACKAGE
SN74LS298 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS298 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

| INPUTS | | OUTPUTS | | | |
|-------------|-------|-----------------|-----------------|-----------------|-----------------|
| WORD SELECT | CLOCK | Q _A | Q _B | Q _C | Q _D |
| L | ↓ | a1 | b1 | c1 | d1 |
| H | ↓ | a2 | b2 | c2 | d2 |
| X | H | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} |

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

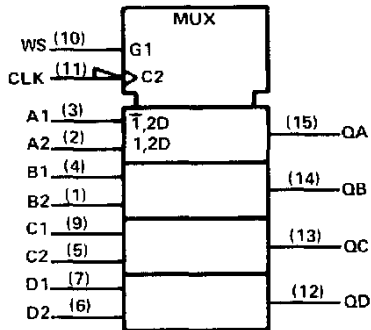
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TEXAS
INSTRUMENTS

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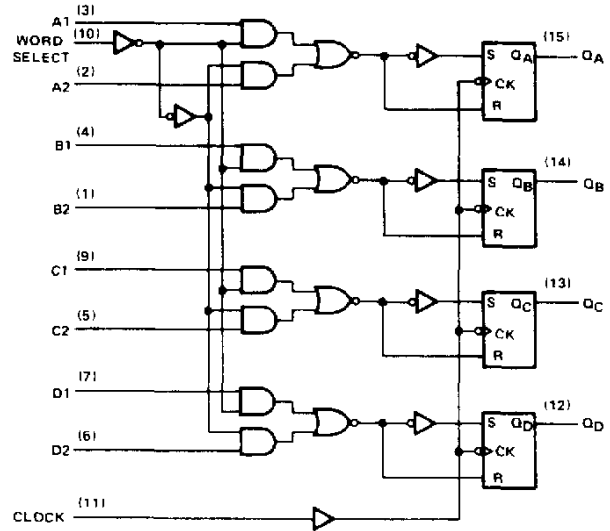
SN54298, SN54LS298, SN74298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

logic symbol†

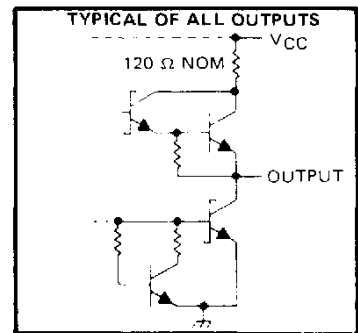
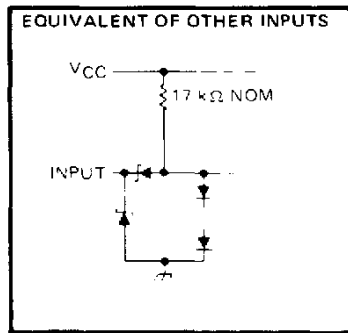
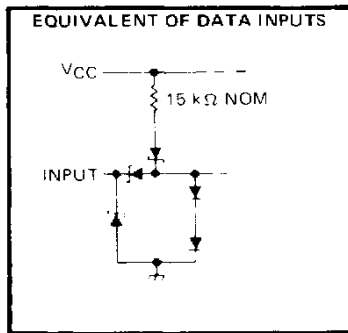
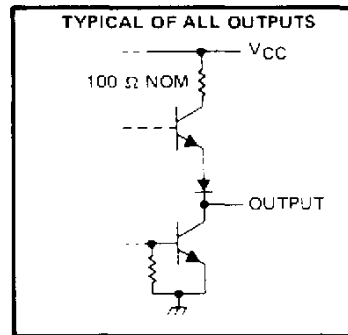
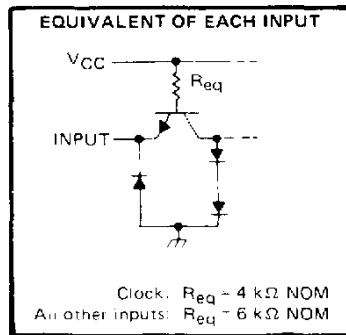


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



schematics of inputs and outputs



SN54298, SN74298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Operating free-air temperature range: SN54298 | -55°C to 125°C |
| SN74298 | 0°C to 70°C |
| Storage temperature | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | SN54298 | | | SN74298 | | | UNIT |
|--|-------------|-----|------|---------|-----|------|---------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | | | -800 | | | -800 | μ A |
| Low-level output current, I_{OL} | | | 16 | | | 16 | mA |
| Width of clock pulse, high or low level, t_W | | 20 | | | 20 | | ns |
| Setup time, t_{SU} | Data | 15 | | 15 | | | ns |
| | Word select | 25 | | 25 | | | |
| Hold time, t_H | Data | 5 | | 5 | | | ns |
| | Word select | 0 | | 0 | | | |
| Operating free-air temperature, T_A | | -55 | 125 | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|--|--|---------|------|------|---------|
| V_{IH} High-level input voltage | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.8 | V |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$ | | | -1.5 | V |
| V_{OH} High-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$ | 2.4 | 3.2 | | V |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$ | | | 0.4 | V |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | | 1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | | 40 | μ A |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | | -1.6 | mA |
| I_{OS} Short-circuit output current§ | $V_{CC} = \text{MAX}$ | SN54298 | -20 | -57 | mA |
| | | SN74298 | -18 | -57 | |
| I_{CC} Supply current | $V_{CC} = \text{MAX}$, See Note 2 | | 39 | 65 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| t_{PLH} Propagation delay time, low-to-high-level output | $C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, | | 18 | 27 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output | See Note 3 | | 21 | 32 | |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54LS298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 7 V |
| Operating free-air temperature range: SN54LS298 | -55°C to 125°C |
| SN74LS298 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | SN54LS298 | | | SN74LS298 | | | UNIT | |
|--|-------------|-----|------|-----------|-----|------|---------|----|
| | MIN | NOM | MAX | MIN | NOM | MAX | | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | |
| High-level output current, I_{OH} | | | -400 | | | -400 | μ A | |
| Low-level output current, I_{OL} | | | 4 | | | 8 | mA | |
| Width of clock pulse, high or low level, t_w | 20 | | | 20 | | | ns | |
| Setup time, t_{SU} | Data | 15 | | 15 | | | ns | |
| | Word select | 25 | | 25 | | | | |
| Hold time, t_H | Data | 5 | | 5 | | | ns | |
| | Word select | 0 | | 0 | | | | |
| Operating free-air temperature, T_A | | | -55 | 125 | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [†] | SN54LS298 | | | SN74LS298 | | | UNIT |
|--|---|-----------|------------------|------|-----------|------------------|------|---------|
| | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V_{IH} High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} High-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$ | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ | | | | | 0.35 | 0.5 | |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$ | | | 20 | | | 20 | μ A |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | | -0.4 | | | -0.4 | mA |
| I_{OS} Short-circuit output current [§] | $V_{CC} = \text{MAX}$ | -20 | | -100 | -20 | | -100 | mA |
| I_{CC} Supply current | $V_{CC} = \text{MAX}$, See Note 2 | | 13 | 21 | | 13 | 21 | mA |

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| t_{PLH} Propagation delay time, low-to-high-level output | $C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, | | 18 | 27 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output | See Note 3 | | 21 | 32 | |

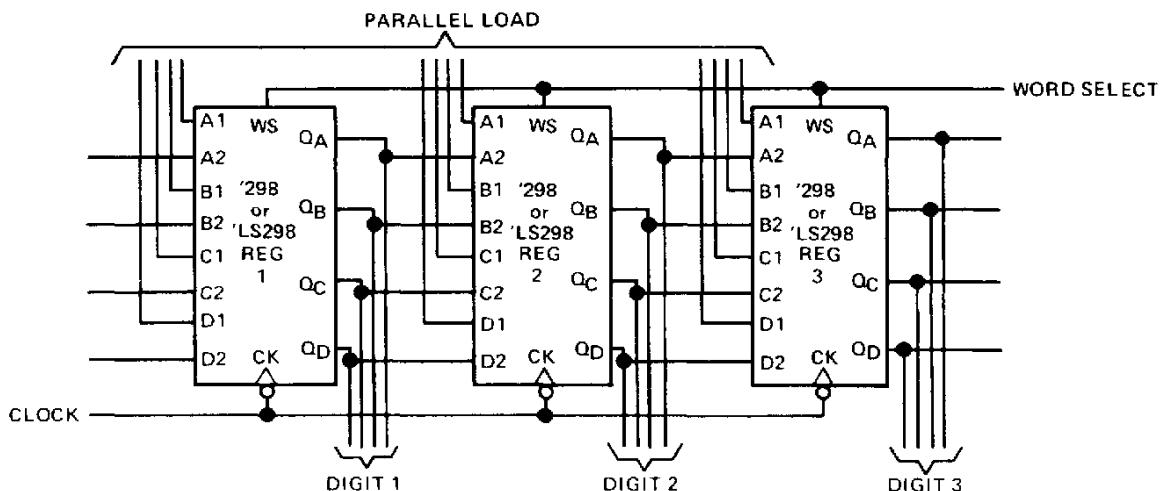
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54298, SN54LS298, SN74298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

TYPICAL APPLICATION DATA

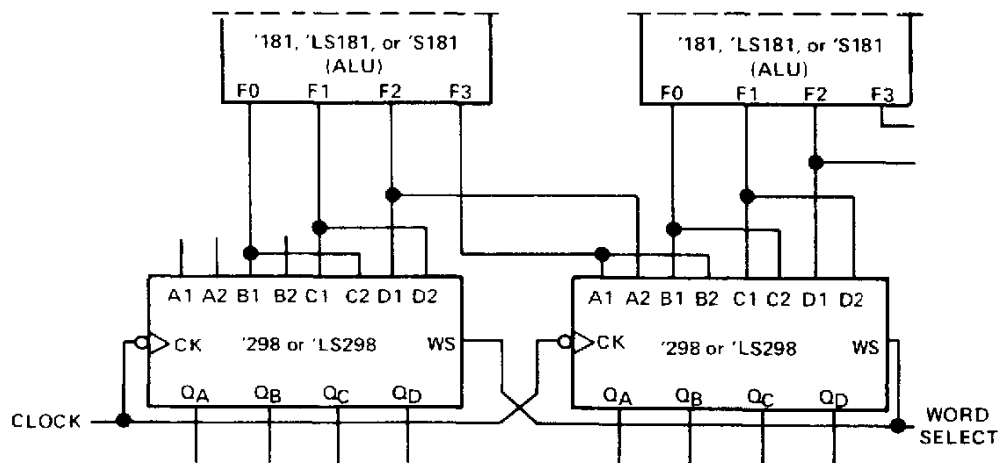
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2 and etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the '298 or 'LS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|--------------------------|-------------------------|
| 7601901EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 7601901EA SNJ54LS298J | Samples |
| SN54LS298J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS298J | Samples |
| SN54LS298J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS298J | Samples |
| SN74LS298N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS298N | Samples |
| SN74LS298N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS298N | Samples |
| SNJ54LS298J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 7601901EA SNJ54LS298J | Samples |
| SNJ54LS298J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 7601901EA SNJ54LS298J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS298, SN74LS298 :

- Catalog: [SN74LS298](#)
- Military: [SN54LS298](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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