

## 74AC1111

### *Dual J-K Negative-Edge-Triggered Flip-Flops with Clear and Preset*

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The 54AC11112 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74AC11112 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

#### **FOR REFERENCE ONLY**

# 54AC11112, 74AC11112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCAS073A – JUNE 1989 – REVISED APRIL 1993

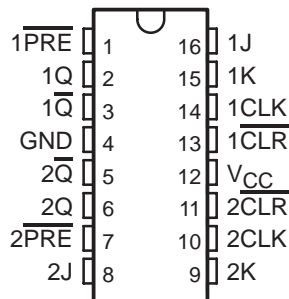
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- ESD Protection Exceeds 2000 V, MIL STD-883C Method 3015
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## description

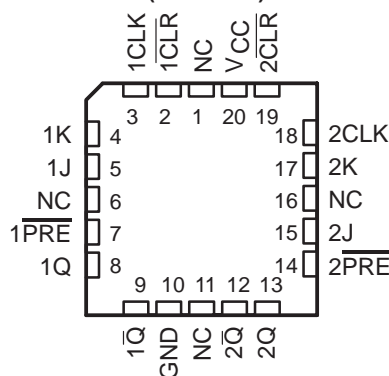
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The 54AC11112 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74AC11112 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

54AC11112 . . . J PACKAGE  
74AC11112 . . . D OR N PACKAGE  
(TOP VIEW)



54AC11112 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each gate)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↓	L	L	$Q_0$	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	$Q_0$	$\overline{Q}_0$

<sup>†</sup> This configuration is nonstable; that is, it will not persist when either  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



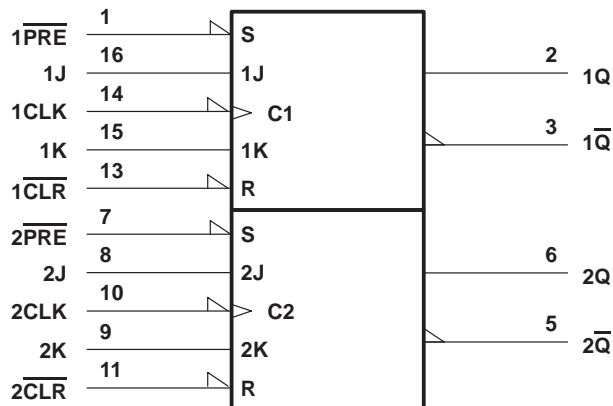
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265  
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

Copyright © 1993, Texas Instruments Incorporated

# 54AC11112, 74AC11112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

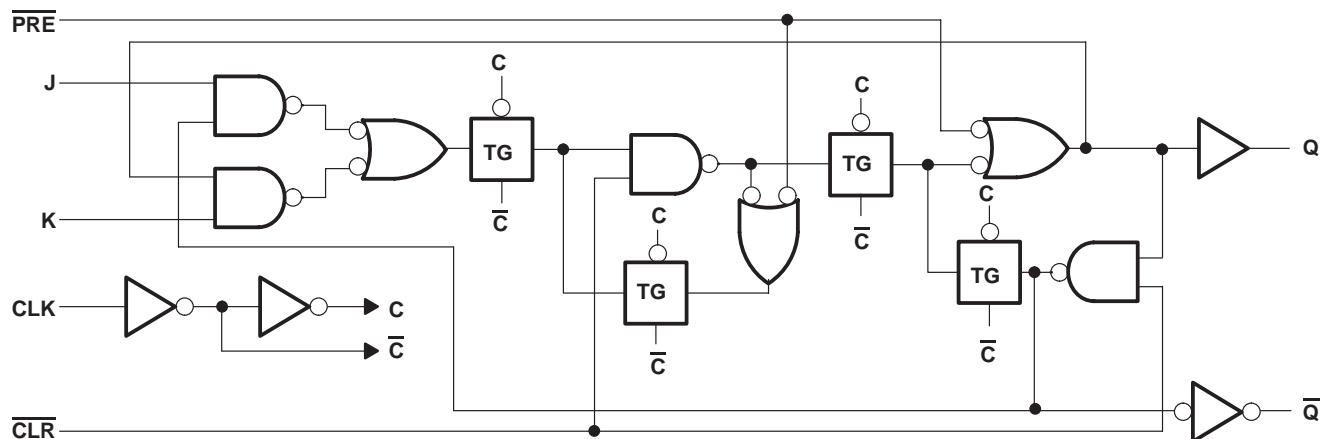
SCAS073A – JUNE 1989 – REVISED APRIL 1993

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

## logic diagram, each flip-flop (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 54AC11112, 74AC11112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCAS073A – JUNE 1989 – REVISED APRIL 1993

## recommended operating conditions

		54AC11112			74AC11112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	3	5	5.5	3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1		2.1			V
		$V_{CC} = 4.5\text{ V}$	3.15		3.15			
		$V_{CC} = 5.5\text{ V}$	3.85		3.85			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$			0.9			V
		$V_{CC} = 4.5\text{ V}$			1.35			
		$V_{CC} = 5.5\text{ V}$			1.65			
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$			-4			mA
		$V_{CC} = 4.5\text{ V}$			-24			
		$V_{CC} = 5.5\text{ V}$			-24			
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$			12			mA
		$V_{CC} = 4.5\text{ V}$			24			
		$V_{CC} = 5.5\text{ V}$			24			
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			54AC11112		74AC11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
$I_{OH} = -50\text{ mA}^\dagger$	5.5 V				3.85					
$I_{OH} = -75\text{ mA}^\dagger$	5.5 V						3.85			
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	3 V				0.1		0.1	V	
		4.5 V				0.1		0.1		
		5.5 V				0.1		0.1		
	$I_{OL} = 12\text{ mA}$	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
		5.5 V					1.65			
$I_{OL} = 50\text{ mA}^\dagger$	5.5 V						1.65			
$I_{OL} = 75\text{ mA}^\dagger$	5.5 V						1.65			
$I_I$	$V_I = V_{CC}$ or GND	5.5 V		$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4		80		40	$\mu\text{A}$	
$C_i$	$V_I = V_{CC}$ or GND	5 V		3.5					pF	

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



# 54AC11112, 74AC11112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCAS073A – JUNE 1989 – REVISED APRIL 1993

## timing requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Figure 1)

			$T_A = 25^\circ\text{C}$		54AC11112		74AC11112		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		0	100	0	70	0	70	MHz
$t_w$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5		5		5		ns
		CLK low or CLK high	5		5		5		
$t_{\text{su}}$	Setup time before CLK $\downarrow$	Data high or low	5		5		5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2.5		2.5		2.5		
$t_h$	Hold time after CLK $\downarrow$		0.5		0.5		0.5		ns

## timing requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

			$T_A = 25^\circ\text{C}$		54AC11112		74AC11112		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		0	125	0	125	0	125	MHz
$t_w$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		4		4		ns
		CLK low or CLK high	4		4		4		
$t_{\text{su}}$	Setup time before CLK $\downarrow$	Data high or low	3.5		3.5		3.5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2		2		2		
$t_h$	Hold time after CLK $\downarrow$		1		1		1		ns

## switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11112		74AC11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			100	150		100		100		MHz
$t_{\text{PLH}}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	1.5	4.9	6.7	1.5	7.6	1.5	7.3	ns
$t_{\text{PHL}}$			1.5	7	9.2	1.5	10.3	1.5	9.9	
$t_{\text{PLH}}$	CLK	Q or $\overline{Q}$	1.5	5.4	7.1	1.5	7.9	1.5	7.6	ns
$t_{\text{PHL}}$			1.5	6	7.9	1.5	9	1.5	8.5	

## switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11112		74AC11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			125	175		125		125		MHz
$t_{\text{PLH}}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	1.5	3.3	5.1	1.5	5.6	1.5	5.4	ns
$t_{\text{PHL}}$			1.5	4.6	6.7	1.5	7.7	1.5	7.3	
$t_{\text{PLH}}$	CLK	Q or $\overline{Q}$	1.5	3.4	5.1	1.5	5.8	1.5	5.6	ns
$t_{\text{PHL}}$			1.5	4.2	6.3	1.5	7.4	1.5	7	

## operating characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

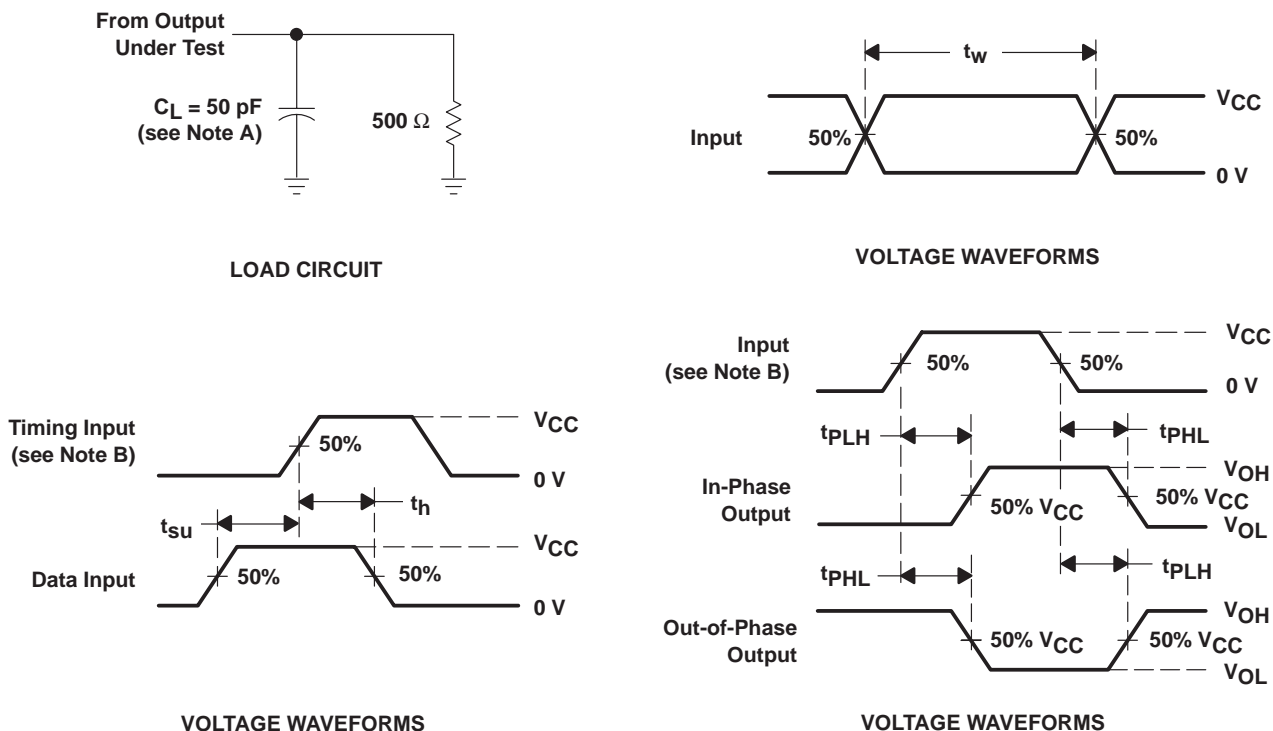
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance per gate $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	37	pF



**54AC11112, 74AC11112**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

SCAS073A - JUNE 1989 - REVISED APRIL 1993

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2009, Texas Instruments Incorporated