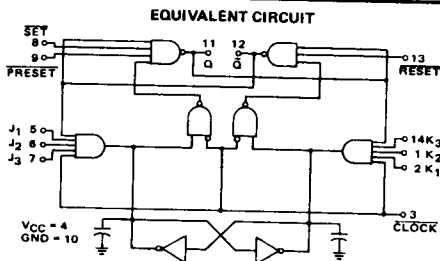
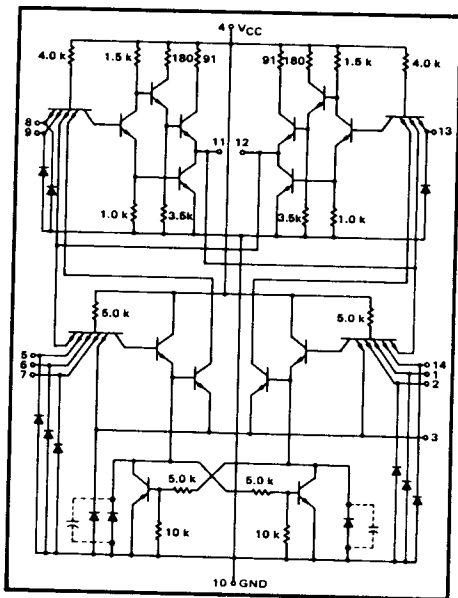


"AND" J-K FLIP-FLOP

MTTL I MC500/400 series

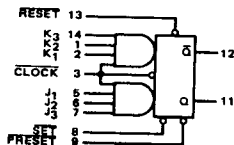
MC515 · MC565
MC415 · MC465



The MC415, MC465, MC515, and MC565 are clocked flip-flops that trigger on the negative edge and perform the J-K logic function. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct SET, PRESET, and RESET are also available.

In normal operation, information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in the high state. When the clock goes low, the information is transferred to the bistable section and the Q and Q-bar outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct SET, PRESET, or RESET inputs.

Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



J	K	Q _n	Q _{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 + J_2 + J_3$
 $K = K_1 + K_2 + K_3$

Total Power Dissipation = 40 mW typ/pkg

Switching Times:

$t_{pd} = 25$ ns typ

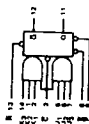
$t_{p\alpha} = 13$ ns typ

TYPE NO.	INPUT LOADING FACTOR (I _F)				OUTPUT DRIVE (I _{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC515	1.5	1	(-2.0 mA)	(-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	-55°C to +125°C
MC565						
MC415	1.5	1	(-2.5 mA)	(-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C
MC465						

MC515, MC565/MC415, MC465 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and K input, plus the SET, PRESET, and RESET inputs. To complete testing, measure through remaining J and K inputs in the same manner.



Input Characteristic	Pin Under Test	MC515, MC565 Test Limits						MC415, MC465 Test Limits						TEST CONDITIONS												
		-55°C		+25°C		+125°C		0°C		+25°C		+75°C		mA				Volts								
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I _F Forward Current	1	-1.33	-1.33	-1.33	-1.33	-1.33	-1.33	-1.86	-1.86	-1.86	-1.86	-1.86	I _{ON}	Pr	Std	I _{in}	2 I _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	
	5												10	1.5	0.7	1.0	2.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	V _{cc}	
	8												20	1.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	V _{cc}
	9												20	1.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	V _{cc}
	13												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	V _{cc}
Leakage Current	1												I _{ON}	Pr	Std	I _{in}	2 I _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{cc}	
	5												10	1.0	-1.5	-0.7	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	8												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	V _{cc}
	9												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	13												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
I _{IL} Inverter Base Current	1	100	100	100	100	100	100	100	100	100	100	100	I _{ON}	Pr	Std	I _{in}	2 I _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{cc}	
	5												10	1.0	-1.5	-0.7	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	8												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	V _{cc}
	9												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	13												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
Breakdown Voltage	1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	V _{in}	Pr	Std	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{cc}	
	5												10	1.0	-1.5	-0.7	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	8												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	V _{cc}
	9												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	13												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
V _{in} Input	1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	V _{in}	Pr	Std	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{in}	V _{cc}	
	5												10	1.0	-1.5	-0.7	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	8												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	V _{cc}
	9												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}
	13												20	1.0	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	V _{cc}

(continued)

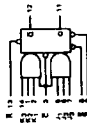
* Pr = Pulse-Out

520

MC515, MC565/MC415, MC465 (continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one device. For the other devices, one of J and K input, plus the SET, PRIORITY, and RESET inputs. To compare the test procedure through out remaining J and K inputs in the same manner.



Characteristic	Symbol	TEST CONDITIONS										V _{OH}	V _{OL}	V _{IL}	V _{IH}	V _{IO}	V _{IOZ}	V _{OC}				
		Pin Under Test		-55°C		+25°C		+125°C		+75°C									MC415, MC465		MC515, MC565	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max								Min	Max	Min	Max
Clock Input	I _T	3	-2.0	-2.0	-2.0	-2.0	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5			
Forward Current	I _F	3	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150			
Leakage Current	I _G	3	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150			
Inverse Beta Current	I _L	3	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150	150			
Breakdown Voltage	BV _{in (0)}	3	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5			
	BV _{in (1)}	3	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5			
Output	V _{out (0)}	12	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45			
Output Voltage	V _{out (1)}	11	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5			
Leakage Current	I _{OLK}	12	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25			
Short-Circuit Current	I _{SC}	12	-45	-90	-45	-90	-45	-90	-45	-90	-45	-90	-45	-90	-45	-90	-45	-90	-45			
Output Voltage	V _{OL}	12	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40			
Power Requirements (Total Device)	I _{DD}	4	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12			
Power Supply Drain	I _{DD}	4	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12			

• Prime Fan-On.

MC515, MC565/MC415, MC465 (continued)

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20 ns.

Provides direct SET, PRESET, and RESET inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

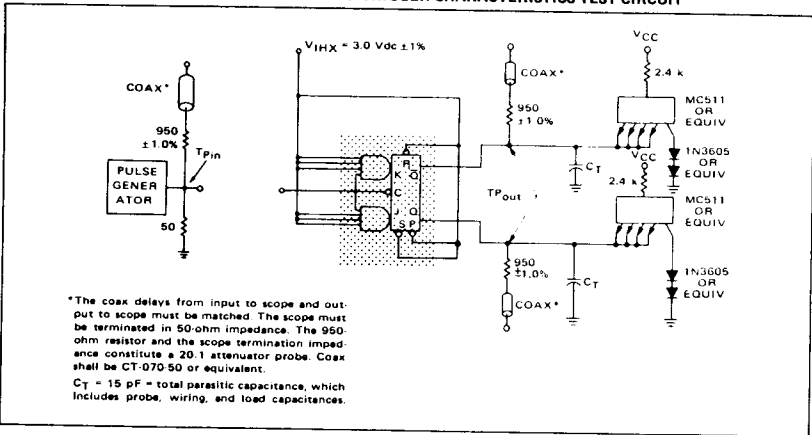
Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1"

state to "0" state information change on the J and K terminals. The flip-flop will require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering - When the clock goes from the high state to the low state, the information in the temporary storage section is transferred, and the Q and \bar{Q} outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. PRESET and SET are tied to \bar{Q} ; RESET is tied to Q.

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



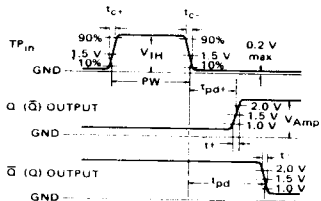
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{pd+}	V		20	ns
Delay Time On	t_{pd-}	V		40	ns
Rise Time	t_r	V		8.0	ns
Fall Time	t_f	V		5.0	ns
Amplitude	V_{amp}	V	3.2		Volt

WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	20 MHz max	W
Pulse Width	PW	20 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_c-	150 ns max	Z

WAVEFORM DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	20	5.0	5.0	1.0		MHz
PW	20	100	20	100	200	ns
t_c+	-	10	-	10	-	ns
t_c-	-	10	-	10	-	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 - JK TERMINAL CHARACTERISTICS TEST CIRCUIT

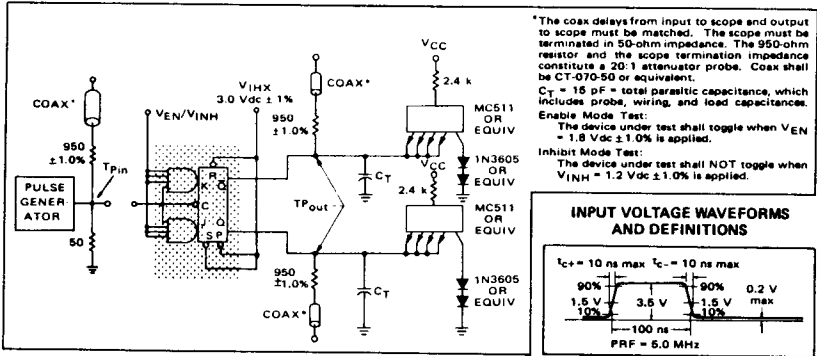


FIGURE 3 - SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT

