4-Bit Bi-Directional Parallel-Access Shift Register

LS95B

DESCRIPTION

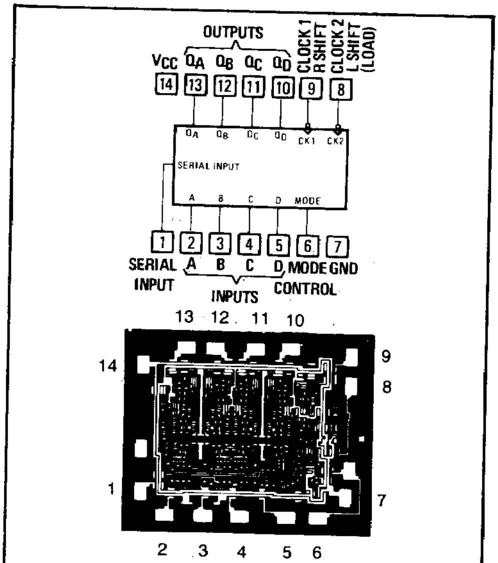
This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three modes of operation:

- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

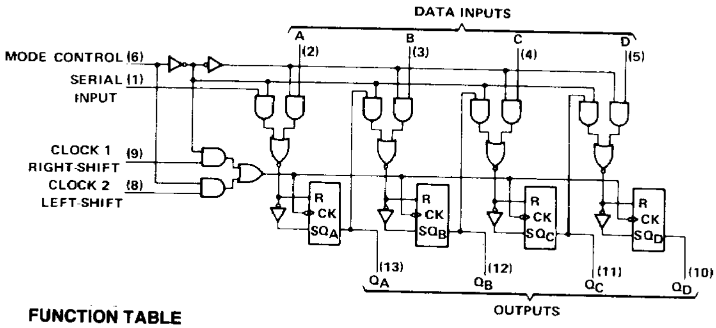
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

PIN-OUT DIAGRAM



Die Size .067 x .082

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at input, A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 2 page 2-57)	25			25			ns
Setup time, high-level or low-level data, t_{setup} (see Figure 1 page 2-57)	0			0			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1 page 2-57)	20			20			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2 page 2-57)	20			20			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2 page 2-57)	20			20			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2 page 2-57)	10			10			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 1 page 2-57)	10			10			ns
Operating free-air temperature T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	Mode inputs	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
	Other inputs					0.1			0.1	
I_{IH}	Mode inputs	V_{CC}=MAX, V_I=2.7V				40			40	μA
	Other inputs					20			20	
I_{IL}	Mode inputs	V_{CC}=MAX, V_I=0.4V				−0.8			−0.8	mA
	Other inputs					−0.4			−0.4	
I_{OS}†		V_{CC}=MAX,		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX, See Note 1			13	21		13	21	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CC} is measured with all outputs and serial inputs open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V then ground, applied to both clock inputs.

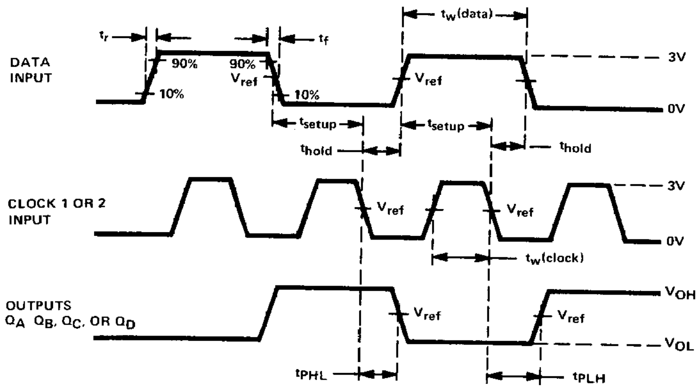
Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174 and Fig. 1 and 2, page 2-57)										
f_{max}				20	30					MHz
t_{PLH}		28	37		27	35		28	37	ns
t_{PHL}		32	45		30	40		32	45	ns
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174 and Fig. 1 and 2, page 2-57)										
t_{PLH}		32	42		31	40		32	42	ns
t_{PHL}		36	50		34	45		36	50	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

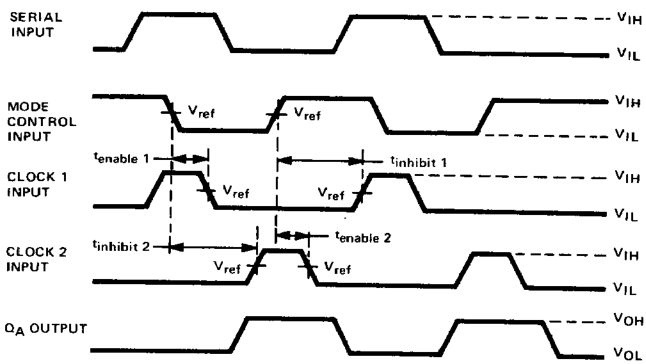


VOLTAGE WAVEFORMS
FIGURE 1 – SWITCHING TIMES

NOTES:

A. Input pulses are supplied by a generator having the following characteristics: $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns, and $Z_{out} \cong 50\Omega$. For the data pulse generator, PRR = 500kHz; for the clock pulse generator, PRR = 1MHz. When testing f_{max}, vary PRR. $t_{w(data)} \geqslant 20$ ns, $t_{w(clock)} \geqslant 15$ ns.

B. $V_{ref} = 1.3V$.



VOLTAGE WAVEFORMS
FIGURE 2 – CLOCK ENABLE/INHIBIT TIMES

NOTES:

A. Input A is at a low level.

B. $V_{ref} = 1.3V$.