# HSP43220/883

January 1994

## Decimating Digital Filter



### Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Single Chip Narrow Band Filter with up to 96dB Attenuation**
- **DC to 25.6MHz Clock Rate**
- **16-Bit 2's Complement Input**
- **20-Bit Coefficients in FIR**
- **24-Bit Extended Precision Output**
- **Programmable Decimation up to a Maximum of 16,384**
- **Standard 16-Bit Microprocessor Interface**
- **Filter Design Software Available DECI•MATE™**

### Applications

- **Very Narrow Band Filters**
- **Zoom Spectral Analysis**
- **Channelized Receivers**

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| HSP43220GM-15/883 | -55°C to +125°C | 84 Lead PGA |
| HSP43220GM-25/883 | -55°C to +125°C | 84 Lead PGA |

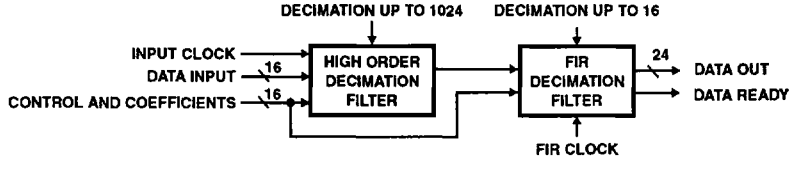
### Description

The HSP43220/883 Decimating Digital Filter is a linear phase low pass decimation filter which is optimized for and filtering narrow band signals in a broad spectrum of a signal processing applications. The HSP43220/883 offers a single chip solution to signal processing application which have historically required several boards of IC's. This reduction in component count results in faster development times as well as reduction of hardware costs.

The HSP43220/883 is implemented as a two stage filter structure. As seen in the block diagram, the first stage is a high order decimation filter (HDF) which utilizes an efficient decimation (sample rate reduction) technique to obtain decimation up to 1024 through a coarse low-pass filtering process. The HDF provides up to 96dB aliasing rejection in the signal pass band. The second stage consists of a finite impulse response (FIR) decimation filter structured as a transversal FIR filter with up to 512 symmetric taps which can implement filters with sharp transition regions. The FIR can perform further decimation by up to 16 if required while preserving the 96dB aliasing attenuation obtained by the HDF. The combined total decimation capability is 16,384.

The HSP43220/883 accepts 16-bit parallel data in 2's complement format at sampling rates up to 30MSPS. It provides a 16-bit microprocessor compatible interface to simplify the task of programming and three-state outputs to allow the connection of several IC's to a common bus. The HSP43220/883 also provides the capability to bypass either the HDF or the FIR for additional flexibility.

### Block Diagram

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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.



File Number **2802.2**

## Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output Voltage Applied ..... GND-0.5V to $V_{CC}$+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C
ESD Classification ..... Class 1

## Reliability Information

| Thermal Resistance | $\theta_{ja}$ | $\theta_{jc}$ |
|---|---|---|
| Ceramic PGA Package ..... | 32.9°C/W | 7.2°C/W |

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package ..... 1.52 Watt
Gate Count ..... 48,250 Gates

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

**TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Devices Guaranteed and 100% Tested

| PARAMETER | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Logical One Input Voltage | $V_{IH}$ | $V_{CC}$ = 5.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | 2.2 | - | V |
| Logical Zero Input Voltage | $V_{IL}$ | $V_{CC}$ = 4.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 0.8 | V |
| Output HIGH Voltage | $V_{OH}$ | $I_{OH}$ = -400µA<br>$V_{CC}$ = 4.5V (Note 1) | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | 2.6 | - | V |
| Output LOW Voltage | $V_{OL}$ | $I_{OL}$ = +2.0mA<br>$V_{CC}$ = 4.5V (Note 1) | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{IN}$ = $V_{CC}$ or GND<br>$V_{CC}$ = 5.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | -10 | +10 | µA |
| Output Leakage Current | $I_O$ | $V_{OUT}$ = $V_{CC}$ or GND<br>$V_{CC}$ = 5.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | -10 | +10 | µA |
| Clock Input High | $V_{IHC}$ | $V_{CC}$ = 5.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | 3.0 | - | V |
| Clock Input Low | $V_{ILC}$ | $V_{CC}$ = 4.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 0.8 | V |
| Standby Power Supply Current | $I_{CCSB}$ | $V_{IN}$ = $V_{CC}$ or GND<br>$V_{CC}$ = 5.5 V,<br>Outputs Open | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 500 | µA |
| Operating Power Supply Current | $I_{CCOP}$ | f = 15.0MHz<br>$V_{CC}$ = 5.5V (Note 2) | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 120.0 | mA |
| Functional Test | FT | (Note 3) | 7, 8 | -55°C ≤ $T_A$ ≤ +125°C | - | - | |

NOTES:
1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8mA/MHz.
3. Tested as follows: f = 1MHz, $V_{IH}$ = 2.6, $V_{IL}$ = 0.4, VOH ≥ 1.5V, $V_{OL}$ ≤ 1.5V, $V_{IHC}$ = 3.4V, and $V_{ILC}$ = 0.4V.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS -15 (15MHz) MIN | LIMITS -15 (15MHz) MAX | LIMITS -25 (25.6MHz) MIN | LIMITS -25 (25.6MHz) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Input Clock Period | $T_{CK}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 66 | - | 39 | - | ns |
| FIR Clock Period | $T_{FIR}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 66 | - | 39 | - | ns |
| Clock Pulse Width Low | $T_{SPWL}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 26 | - | 16 | - | ns |
| Clock Pulse Width High | $T_{SPWH}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 26 | - | 16 | - | ns |
| Clock Skew Between FIR__CK and CK__IN | $T_{SK}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 0 | $T_{FIR}$ - 25 | 0 | $T_{FIR}$ - 19 | ns |
| RESET# Pulse Width Low | $T_{RSPW}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | $4T_{CK}$ | - | $4T_{CK}$ | - | ns |
| Recovery Time On RESET# | $T_{RTRS}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | $8T_{CK}$ | - | $8T_{CK}$ | - | ns |
| ASTARTIN# Pulse Width Low | $T_{AST}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | $T_{CK}$ + 10 | - | $T_{CK}$ + 10 | - | ns |
| STARTOUT# Delay From CK__IN | $T_{STOD}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | - | 35 | - | 20 | ns |
| STARTIN# Setup To CK__IN | $T_{STIC}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 25 | - | 15 | - | ns |
| Setup Time on DATA__IN | $T_{SET}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 20 | - | 16 | - | ns |
| Hold Time on All Inputs | $T_{HOLD}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 0 | - | 0 | - | ns |
| Write Pulse Width Low | $T_{WL}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 26 | - | 15 | - | ns |
| Write Pulse Width High | $T_{WH}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 26 | - | 20 | - | ns |
| Setup Time on Address Bus Before the Rising Edge of Write | $T_{STADD}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 28 | - | 24 | - | ns |
| Setup Time on Chip Select Before the Rising Edge of Write | $T_{STCS}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 28 | - | 24 | - | ns |
| Setup Time on Control Bus Before the Rising Edge of Write | $T_{STCB}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 28 | - | 24 | - | ns |
| DATA__RDY Pulse Width Low | $T_{DRPWL}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | $2T_{FIR}$ - 20 | - | $2T_{FIR}$ - 10 | - | ns |
| DATA__OUT Delay Relative to FIR__CK | $T_{FIRDV}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | - | 50 | - | 35 | ns |
| DATA__RDY Valid Delay Relative to FIR__CK | $T_{FIRDR}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | - | 35 | - | 25 | ns |
| DATA__OUT Delay Relative to OUT__SELH | $T_{OUT}$ | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | - | 30 | - | 25 | ns |
| Output Enable to Data Out Valid | $T_{OEV}$ | Note 2 | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | - | 20 | - | 20 | ns |

NOTES:

1. A.C. Testing: VCC = 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input and output timing measurements are made at 1.5V for both a Logic "1" and "0". CLK is driven at 4.0V and 0V and measured at 2.0V.
2. Transition is measured at ±200mV from steady state voltage with loading as specified by test load circuit and $C_L$ = 40pF.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETERS | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS -15 (15MHz) MIN | LIMITS -15 (15MHz) MAX | LIMITS -25 (25.6MHz) MIN | LIMITS -25 (25.6MHz) MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| CK__IN Pulse Width Low | $T_{CH1L}$ | | 1, 3 | $-55^oC \leq T_A \leq +125^oC$ | 29 | - | 19 | - | ns |
| CK__IN Pulse Width High | $T_{CH1H}$ | | 1, 3 | $-55^oC \leq T_A \leq +125^oC$ | 29 | - | 19 | - | ns |
| CK__IN Setup to FIR__CK | $T_{CIS}$ | | 1, 3 | $-55^oC \leq T_A \leq +125^oC$ | 27 | - | 17 | - | ns |
| CK__IN Hold from FIR__CK | $T_{CIH}$ | | 1, 3 | $-55^oC \leq T_A \leq +125^oC$ | 2 | - | 2 | - | ns |
| Input Capacitance | $C_{IN}$ | $V_{CC}$ = Open, f = 1MHz, All measurements are referenced to device GND. | 1 | $T_A = +25^oC$ | - | 12 | - | 12 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{CC}$ = Open, f = 1MHz, All measurements are referenced to device GND. | 1 | $T_A = +25^oC$ | - | 10 | - | 10 | pF |
| Output Disable Delay | $T_{OEZ}$ | | 1, 2 | $-55^oC \leq T_A \leq +125^oC$ | - | 20 | - | 20 | ns |
| Output Rise Time | $T_{OR}$ | | 1, 2 | $-55^oC \leq T_A \leq +125^oC$ | - | 8 | - | 8 | ns |
| Output Fall Time | $T_{OF}$ | | 1, 2 | $-55^oC \leq T_A \leq +125^oC$ | - | 8 | - | 8 | ns |

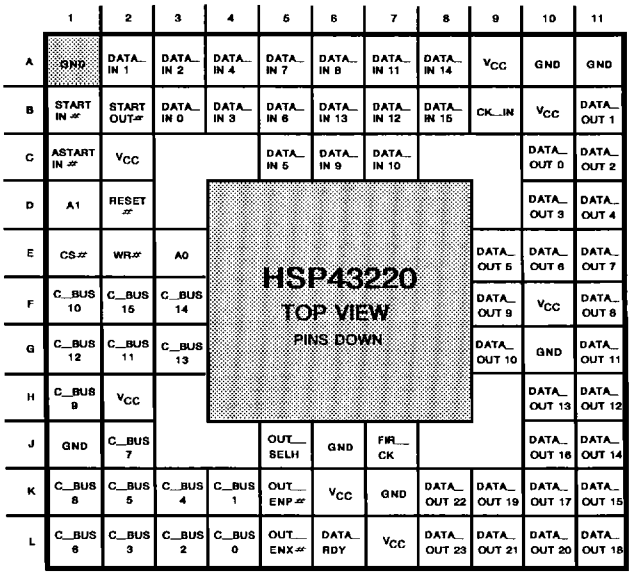
NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with $C_L$ = 40pF.
3. Applies only when H__BYP = 1 or H__DRATE = 0.

TABLE 4. APPLICABLE SUBGROUPS

| CONFORMANCE GROUPS | METHOD | SUBGROUPS |
|---|---|---|
| Initial Test | 100%/5004 | - |
| Interim Test | 100%/5004 | - |
| PDA | 100% | 1 |
| Final Test | 100% | 2, 3, 8A, 8B, 10, 11 |
| Group A | — | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 |
| Groups C & D | Samples/5005 | 1, 7, 9 |

## Burn-In Circuit




| PIN LEAD | PIN NAME | BURN-IN SIGNAL |
|---|---|---|
| A1 | GND | GND |
| A2 | DATA_IN 1 | F2 |
| A3 | DATA_IN 2 | F3 |
| A4 | DATA_IN 4 | F5 |
| A5 | DATA_IN 7 | F8 |
| A6 | DATA_IN 8 | F1 |
| A7 | DATA_IN 11 | F4 |
| A8 | DATA_IN 14 | F7 |
| A9 | $V_{CC}$ | $V_{CC}$ |
| A10 | GND | GND |
| A11 | GND | GND |
| B1 | STARTIN# | F15 |
| B2 | STARTOUT# | $V_{CC}/2$ |
| B3 | DATA_IN 0 | F1 |
| B4 | DATA_IN 3 | F4 |
| B5 | DATA_IN 6 | F7 |
| B6 | DATA_IN 13 | F6 |
| B7 | DATA_IN 12 | F5 |
| B8 | DATA_IN 15 | F8 |
| B9 | CK_IN | F0 |
| B10 | $V_{CC}$ | $V_{CC}$ |
| B11 | DATA_OUT 1 | $V_{CC}/2$ |

| PIN LEAD | PIN NAME | BURN-IN SIGNAL |
|---|---|---|
| C1 | ASTARTIN# | F15 |
| C2 | $V_{CC}$ | $V_{CC}$ |
| C5 | DATA_IN 5 | F6 |
| C6 | DATA_IN 9 | F2 |
| C7 | DATA_IN 10 | F3 |
| C10 | DATA_OUT 0 | $V_{CC}/2$ |
| C11 | DATA_OUT 2 | $V_{CC}/2$ |
| D1 | A1 | F14 |
| D2 | RESET# | F16 |
| D10 | DATA_OUT 3 | $V_{CC}/2$ |
| D11 | DATA_OUT 4 | $V_{CC}/2$ |
| E1 | CS# | F11 |
| E2 | WR# | F11 |
| E3 | A0 | F13 |
| E9 | DATA_OUT 5 | $V_{CC}/2$ |
| E10 | DATA_OUT 6 | $V_{CC}/2$ |
| E11 | DATA_OUT 7 | $V_{CC}/2$ |
| F1 | C_BUS 10 | F3 |
| F2 | C_BUS 15 | F8 |
| F3 | C_BUS 14 | F7 |
| F9 | DATA_OUT 9 | $V_{CC}/2$ |
| F10 | $V_{CC}$ | $V_{CC}$ |

| PIN LEAD | PIN NAME | BURN-IN SIGNAL |
|---|---|---|
| F11 | DATA_OUT 3 | $V_{CC}/2$ |
| G1 | C_BUS 12 | F5 |
| G2 | C_BUS 11 | F4 |
| G3 | C_BUS 13 | F6 |
| G9 | DATA_OUT 10 | $V_{CC}/2$ |
| G10 | GND | GND |
| G11 | DATA_OUT 11 | $V_{CC}/2$ |
| H1 | C_BUS 9 | F2 |
| H2 | $V_{CC}$ | $V_{CC}$ |
| H10 | DATA_OUT 13 | $V_{CC}/2$ |
| H11 | DATA_OUT 12 | $V_{CC}/2$ |
| J1 | GND | GND |
| J2 | C_BUS 7 | F8 |
| J5 | OUT_SELH | F10 |
| J6 | GND | GND |
| J8 | FIR_CK | F0 |
| J10 | DATA_OUT 16 | $V_{CC}/2$ |
| J11 | DATA_OUT 14 | $V_{CC}/2$ |
| K1 | C_BUS 8 | F1 |
| K2 | C_BUS 5 | F6 |
| K3 | C_BUS 4 | F5 |
| K4 | C_BUS 1 | F2 |

NOTES:
1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except $V_{CC}$ and GND.
3. $V_{CC}$ = 5.5 ±0.5V.
4. 0.1µF (min) capacitor between $V_{CC}$ and GND per position.
5. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2 ..... F16 = F15/2, 40% - 60% Duty Cycle.
6. Input voltage limits: $V_{IL}$ = 0.8 max, $V_{IH}$ = 4.5V ±10%.

## Burn-In Circuit (Continued)

| PIN LEAD | PIN NAME | BURN-IN SIGNAL |
|---|---|---|
| K5 | OUT_ENP# | F9 |
| K6 | $V_{CC}$ | $V_{CC}$ |
| K7 | GND | GND |
| K8 | DATA_OUT 22 | $V_{CC}/2$ |
| K9 | DATA_OUT 19 | $V_{CC}/2$ |
| K10 | DATA_OUT 17 | $V_{CC}/2$ |

| PIN LEAD | PIN NAME | BURN-IN SIGNAL |
|---|---|---|
| K11 | DATA_OUT 15 | $V_{CC}/2$ |
| L1 | C_BUS 6 | F7 |
| L2 | C_BUS 3 | F4 |
| L3 | C_BUS 2 | F3 |
| L4 | C_BUS 0 | F1 |
| L5 | OUT_ENX# | F9 |

| PIN LEAD | PIN NAME | BURN-IN SIGNAL |
|---|---|---|
| L6 | DATA_RDY# | $V_{CC}/2$ |
| L7 | $V_{CC}$ | $V_{CC}$ |
| L8 | DATA_OUT 23 | $V_{CC}/2$ |
| L9 | DATA_OUT 21 | $V_{CC}/2$ |
| L10 | DATA_OUT 20 | $V_{CC}/2$ |
| L11 | DATA_OUT 18 | $V_{CC}/2$ |

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except $V_{CC}$ and GND.
3. $V_{CC}$ = 5.5 ±0.5V.
4. 0.1µF (min) capacitor between $V_{CC}$ and GND per position.
5. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2 ..... F16 = F15/2, 40% - 60% Duty Cycle.
6. Input voltage limits: $V_{IL}$ = 0.8 max, $V_{IH}$ = 4.5V ±10%.

## Metal Topology

**DIE DIMENSIONS:**
348 x 349.2 x 19±1 mils

**METALLIZATION:**
Type: Si - Al or Si - Al - Cu
Thickness: 8kÅ

**WORST CASE CURRENT DENSITY:**
$1.18 \times 10^5 A/cm^2$

**GLASSIVATION:**
Type: Nitrox
Thickness: 10kÅ

## Metallization Mask Layout

**HSP43220/883**