HARRIS SEMICONDUCTOR

HSP43124

January 1997

Serial I/O Filter

Features

- 45MHz Clock Rate
- 256 Tap Programmable FIR Filter
- 24-Bit Data, 32-Bit Coefficients
- Cascade of up to 5 Half Band Filters
- Decimation from 1 to 256
- Two Pin Interface for Down Conversion by $F_S/4$
- Multiplier for Mixing or Scaling Input with an External Source
- Serial I/O Compatible with Most DSP Microprocessors

Applications

- Low Cost FIR Filter
- Filter Co-Processor
- Digital Tuner

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43124PC-45	0 to 70	28 Ld PDIP	E28.6
HSP43124PC-33	0 to 70	28 Ld PDIP	E28.6
HSP43124SC-45	0 to 70	28 Ld SOIC	M28.3
HSP43124SC-33	0 to 70	28 Ld SOIC	M28.3
HSP43124SI-40	-40 to 85	28 Ld SOIC	M28.3

Description

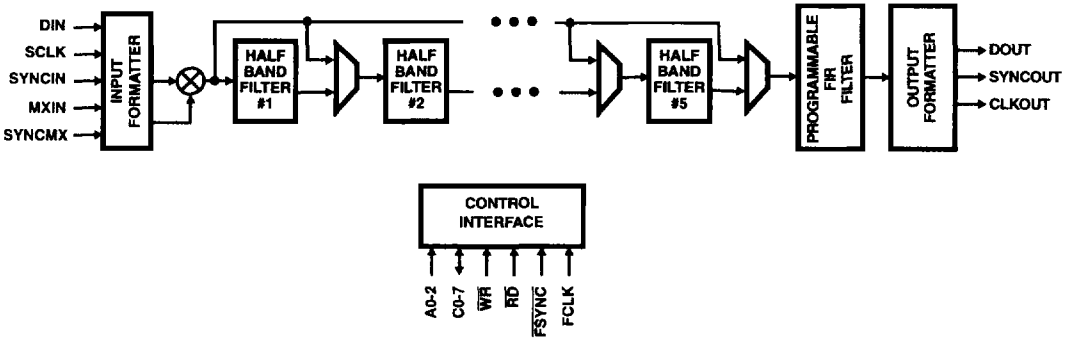
The Serial I/O Filter is a high performance filter engine that is ideal for off loading the burden of filter processing from a DSP microprocessor. It supports a variety of multistage filter configurations based on a user programmable filter and fixed coefficient halfband filters. These configurations include a programmable FIR filter of up to 256 taps, a cascade of from one to five halfband filters, or a cascade of halfband filters followed by a programmable FIR. The half band filters each decimate by a factor of two, and the FIR filter decimates from one to eight. When all six filters are selected, a maximum decimation of 256 is provided.

For digital tuning applications, a separate multiplier is provided which allows the incoming data stream to be multiplied, or mixed, by a user supplied mix factor. A two pin interface is provided for serially loading the mix factor from an external source or selecting the mix factor from an on-board ROM. The on-board ROM contains samples of a sinusoid capable of spectrally shifting the input data by one quarter of the sample rate, $F_S/4$. This allows the chip to function as a digital down converter when the filter stages are configured as a low-pass filter.

The serial interface for input and output data is compatible with the serial ports of common DSP microprocessors. Coefficients and configuration data are loaded over a bidirectional eight bit interface.

5 STANDARD PRODUCTS

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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