National Semiconductor

LMF40 High Performance 4th-Order Switched-Capacitor Butterworth Low-Pass Filter

General Description

The LMF40 is a versatile, easy to use, precision 4th-order Butterworth low-pass filter fabricated using National's high performance LMCMOS process. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency. The ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50-to-1 (LMF40-50) or 100-to-1 (LMF40-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, an external TTL or CMOS logic compatible clock can be applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading LMF40 sections together for higher-order filtering.

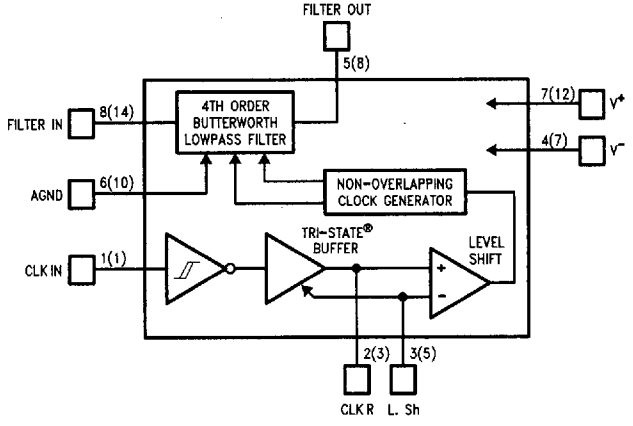
Features

- Cutoff frequency range of 0.1 Hz to 40 kHz
- Cutoff frequency accuracy of ±1.0%, maximum
- Low offset voltage, ±100 mV, maximum, ±5V supply
- Low clock feedthrough of 5 mV_{P-P}, typical
- Dynamic range of 88 dB, typical
- No external components required
- 8-pin mini-DIP or 14-pin wide-body small-outline packages
- 4V to 14V single/dual supply operation
- Cutoff frequency set by external or internal clock
- Pin-compatible with MF4

Applications

- Communication systems
- Instrumentation
- Automated control systems

Block and Connection Diagrams



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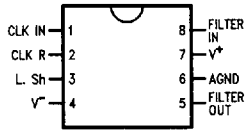
*Pin numbers in parentheses are for the 14-pin package

Dual-In-Line Package



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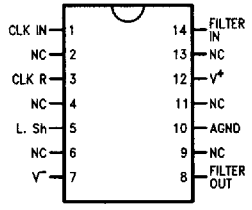
Top View

Small-Outline-Wide-Body Package



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Top View

Ordering Information

Industrial ($-40°C \le T_A \le +85°C$)	Package
LMF40CIN-50, LMF40CIN-100	N08E
LMF40CIWM-50	M14B
LMF40CIWM-100	M14B
Military ($-55°C \le T_A \le +125°C$)	
LMF40CMJ-50, LMF40CMJ-100	J08A

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Absolute Maximum Ratings

(Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	15V
Voltage at Any Pin	$V^- - 0.2V$ to $V^+ + 0.2V$
Input Current at Any Pin (Note 13)	5 mA
Package Input Current (Note 13)	20 mA
Power Dissipation (Note 14)	500 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, Soldering (10 sec.)	+260°C
J Package, Soldering (10 sec.)	+300°C
WM Package, Vapor Phase (60 sec.) (Note 16)	+215°C
WM Package, Infrared (15 sec.)	+220°C
ESD Susceptibility (Note 12)	2000V
Pin 1 CLK IN	1700V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF40CIN-50, LMF40CIN-100	
LMF40CIWM-50,	
LMF40CIWM-100	$-40°C \le T_A \le +85°C$
LMF40CMJ-50, LMF40CMJ-100	$-55°C \le T_A \le +125°C$
Supply Voltage Range ($V^+ - V^-$)	4V to 14V

Filter Electrical Characteristics

The following specifications apply for f_{CLK} = 500 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
$V^+ = +5V, V^- = -5V$					
f_{CLK}	Clock Frequency Range (Note 17)		5	**2**	Hz (min) MHz (max)
I_S	Supply Current	CMJ CIN, CIJ, CIWM		3.5 / **7.0** 3.5 / **5.0**	mA (max) mA (max)
H_O	DC Gain	$R_{Source} \le 2\ k\Omega$		+0.05 / **+0.05** −0.15 / **−0.20**	dB (max) dB (min)
f_{CLK}/f_c	Clock to Cutoff Frequency Ratio (Note 3) LMF40-50 LMF40-100			 49.80 ± 0.8% / **49.80 ± 1.0%** 99.00 ± 0.8% / **99.00 ± 1.0%**	 (max) (max)
$\Delta f_{CLK}/f_c/\Delta T$	Clock to Cutoff Frequency Ratio Temperature Coefficient LMF40-50 LMF40-100		 5 5		 ppm/°C ppm/°C
A_{MIN}	Stopband Attenuation	At 2 f_c		**24.0**	dB (min)

Filter Electrical Characteristics (Continued)

The following specifications apply for f_{CLK} = 500 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
V^+ = +5V, V^- = −5V (Continued)					
V_{OS}	Unadjusted DC Offset Voltage LMF40-50 LMF40-100			 ±80 / **±100** ±80 / **±100**	 mV (max) mV (max)
V_O	Output Swing	R_L = 5 kΩ		+3.9 / **+3.7** −4.2 / **−4.0**	V (min) V (max)
I_{SC}	Output Short Circuit Current (Note 8)	Source Sink	90 2.2		mA mA
	Dynamic Range (Note 4)		88		dB
	Additional Magnitude Response Test Points (Note 6) LMF40-50	 f_{IN} = 12 kHz f_{IN} = 9 kHz		 −7.50 ±0.26 / **−7.50 ±0.30** −1.46 ±0.12 / **−1.46 ±0.16**	 dB (max) dB (max)
	LMF40-100	f_{IN} = 6 kHz f_{IN} = 4.5 kHz		−7.15 ±0.26 / **−7.15 ±0.30** −1.42 ±0.12 / **−1.42 ±0.16**	dB (max) dB (max)
	Clock Feedthrough	Filter Output V_{IN} = 0V	5		mV_{P-P}

Filter Electrical Characteristics

The following specifications apply for f_{CLK} = 250 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
V^+ = +2.5V, V^- = −2.5V					
f_{CLK}	Clock Frequency Range (Note 17)		5	 **1.0**	Hz (min) MHz (max)
I_S	Supply Current	CMJ CIN, CIJ, CIWM		2.1 / **4.0** 2.1 / **3.0**	mA (max) mA (max)
H_O	DC Gain	$R_S \leq 2$ kΩ f_{CLK} = 250 kHz		+0.05 / **+0.05** −0.15 / **−0.20**	dB (max) dB (min)
		f_{CLK} = 500 kHz	−0.1		dB
f_{CLK}/f_c	Clock to Cutoff Frequency Ratio LMF40-50	 f_{CLK} = 250 kHz		 **49.80 ±0.8%**	 (max)
		f_{CLK} = 500 kHz	49.80 ±0.6%		
	LMF40-100 (Note 3)	f_{CLK} = 250 kHz		99.00 ±1.0% / **99.00 ±1.2%**	(max)
		f_{CLK} = 500 kHz	99.00 ±1.2%		

Filter Electrical Characteristics (Continued)

The following specifications apply for f_{CLK} = 250 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
V^+ = +2.5V, V^- = −2.5V (Continued)					
$\Delta f_{CLK}/f_c/\Delta T$	Clock to Cutoff Frequency Ratio Temperature Coefficient				
	LMF40-50		5		ppm/°C
	LMF40-100		5		ppm/°C
A_{MIN}	Stopband Attenuation	At 2 f_c		**−24.0**	dB (min)
V_{OS}	Unadjusted DC Offset Voltage				
	LMF40-50			±80 / ±**100**	mV (max)
	LMF40-100			±80 / ±**100**	mV (max)
V_O	Output Swing	R_L = 5 kΩ		+1.4 / +**1.2**	V (min)
				−2.0 / −**1.8**	V (max)
I_{SC}	Output Short Circuit Current (Note 8)	Source	42		mA
		Sink	0.9		mA
	Dynamic Range (Note 4)		81		dB
	Additional Magnitude Response Test Points (Note 6)				
	LMF40-50	f_{IN} = 6 kHz		−7.50 ±0.26 / −**7.50** ±**0.30**	dB (max)
		f_{IN} = 4.5 kHz		−1.46 ±0.12 / −**1.46** ±**0.16**	dB (max)
	LMF40-100	f_{IN} = 3 kHz		−7.15 ±0.26 / −**7.15** ±**0.30**	dB (max)
		f_{IN} = 2.25 kHz		−1.42 ±0.12 / −**1.42** ±**0.16**	dB (max)
	Clock Feedthrough	Filter Output V_{IN} = 0V	5		mV_{P-P}

Logic Input-Output Characteristics

The following specifications apply for V^- = 0V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
TTL CLOCK INPUT, CLK R PIN (Note 9)					
	TTL CLK R Pin Input Voltage	V^+ = +5V, V^- = −5V			
	Logic "1"			2.0 / **2.1**	V (min)
	Logic "0"			0.8 / **0.8**	V (max)
	CLK R Input Voltage	V^+ = +2.5V, V^- = −2.5V			
	Logic "1"			2.0 / **2.0**	V (min)
	Logic "0"			0.6 / **0.4**	V (max)
	Maximum Leakage Current at CLK R Pin		2.0		μA
SCHMITT TRIGGER					
V_T+	Positive Going Input Threshold Voltage CLK IN Pin	V^+ = +10V		6.1 / **6.0**	V (min)
				8.8 / **8.9**	V (max)
		V^+ = +5V		3.0 / **2.9**	V (min)
				4.3 / **4.4**	V (max)

Logic Input-Output Characteristics (Continued) The following specifications apply for V^- = 0V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
SCHMITT TRIGGER (Continued)					
V_T-	Negative Going Input Threshold Voltage CLK IN Pin	$V^+ = +10V$		1.4 / **1.3** 3.8 / **3.9**	V (min) V (max)
		$V^+ = +5V$		0.7 / **0.6** 1.9 / **2.0**	V (min) V (max)
$V_T+ - V_T-$	Hysteresis CLK IN Pin	$V^+ = +10V$		2.3 / **2.1** 7.4 / **7.6**	V (min) V (max)
		$V^+ = +5V$		1.1 / **0.9** 3.6 / **3.8**	V (min) V (max)
	Logical "1" Output Voltage CLK R Pin	$I_O = -10\ \mu A$ $V^+ = +10V$ $V^+ = +5V$		 9.1 / **9.0** 4.6 / **4.5**	 V (min) V (min)
	Logical "0" Output Voltage CLK R Pin	$I_O = -10\ \mu A$ $V^+ = +10V$ $V^+ = +5V$		 0.9 / **1.0** 0.4 / **0.5**	 V (max) V (max)
	Output Source Current CLK R Pin	CLK R to V^- $V^+ = +10V$ $V^+ = +5V$		 4.9 / **3.7** 1.6 / **1.2**	 mA (min) mA (min)
	Output Sink Current CLK R Pin	CLK R to V^+ $V^+ = +10V$ $V^+ = +5V$		 4.9 / **3.7** 1.6 / **1.2**	 mA (min) mA (min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating range.

Note 2: All voltages are specified with respect to ground.

Note 3: The filter's cutoff frequency is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 4: For ±5V supplies the dynamic range is referenced to 2.62 V_{rms} (3.7V peak) where the wideband noise over a 20 kHz bandwidth is typically 100 μV_{rms} for the LMF40. For ±2.5V supplies the dynamic range is referenced to 0.849 V_{rms} (1.2V peak) where the wideband noise over a 20 kHz bandwidth is typically 75 μV_{rms} for the LMF40.

Note 5: The specifications for the LMF40 have been given for a clock frequency (f_{CLK}) of 500 kHz at ±5V and 250 kHz at ±2.5V. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.8% over the temperature range, but the filter still maintains its magnitude characteristics. See Application Information, Section 1.4.

Note 6: The filter's magnitude response is tested at the cutoff frequency, f_c, $f_S = 2\ f_c$, and at these other two additional frequencies.

Note 7: For simplicity all logic levels have been referenced to $V^- = 0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 8: The short circuit source current is measured by forcing the output that is being tested to its maximum positive swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage and then shorting that output to the positive supply. These are worst case conditions.

Note 9: The LMF40 is operated with symmetrical supplies and L. Sh. is tied to ground.

Note 10: Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.

Note 11: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 13: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 14: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $PD = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMF40, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W for the LMF40CIN, 62°C/W for the LMF40CIJ and LMF40CMJ, and 78°C/W for the LMC40CIWM.

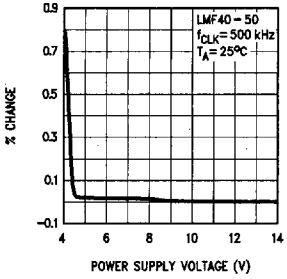
Note 15: In popular usage the term cutoff frequency defines that frequency at which a filter's gain drops 3.01 dB below its DC value. Equations (2) and (3) and design example 2.1, however, use the term cutoff frequency (f_b) to define that frequency at which a filter's gain drops by a variable amount as determined from the given design specifications.

Note 16: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices or see the section titled "Surface Mount" in the *Linear Data Book*.

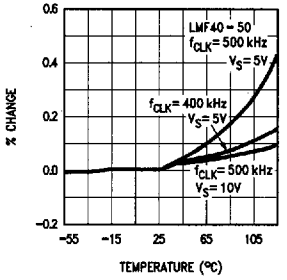
Note 17: The nominal ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50-to-1 (LMF40-50) or 100-to-1 (LMF40-100).

Typical Performance Characteristics

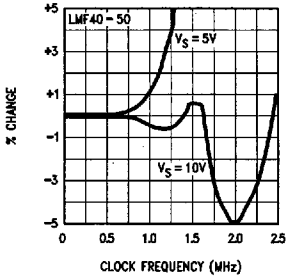
f_{CLK}/f_c Deviation vs Power Supply Voltage



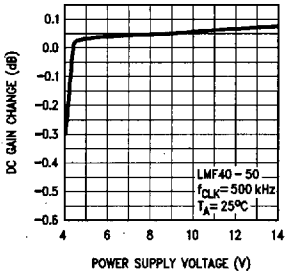
f_{CLK}/f_c Deviation vs Temperature



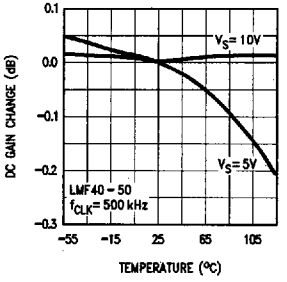
f_{CLK}/f_c Deviation vs Clock Frequency



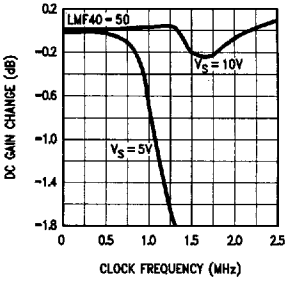
DC Gain Deviation vs Power Supply Voltage



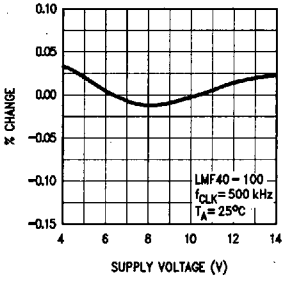
DC Gain Deviation vs Temperature



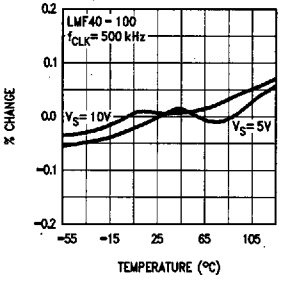
DC Gain Deviation vs Clock Frequency



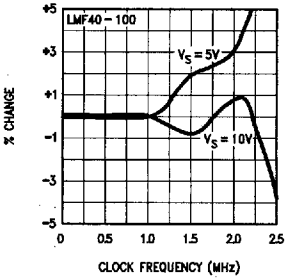
f_{CLK}/f_c Deviation vs Power Supply Voltage



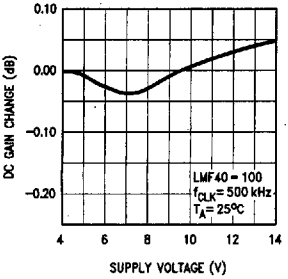
f_{CLK}/f_c Deviation vs Temperature



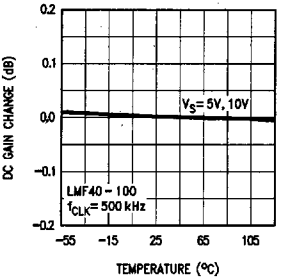
f_{CLK}/f_c Deviation vs Clock Frequency



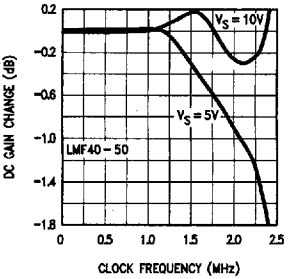
DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Temperature



DC Gain Deviation vs Clock Frequency



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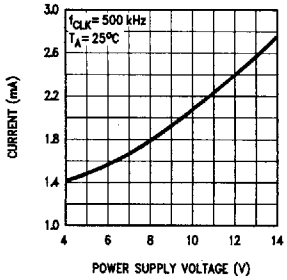
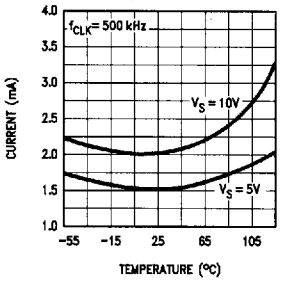
Typical Performance Characteristics (Continued)

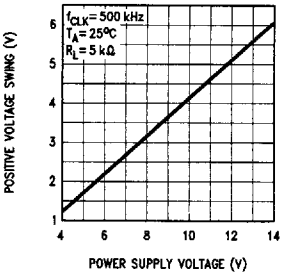
Power Supply Current vs Power Supply Voltage



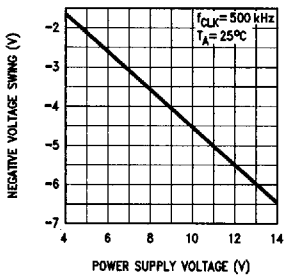
Power Supply Current vs Temperature



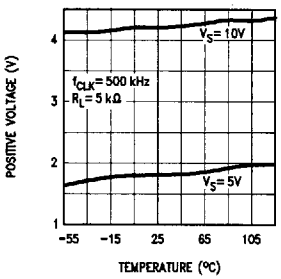
Positive Voltage Swing vs Power Supply Voltage



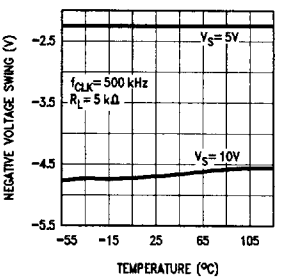
Negative Voltage Swing vs Power Supply Voltage



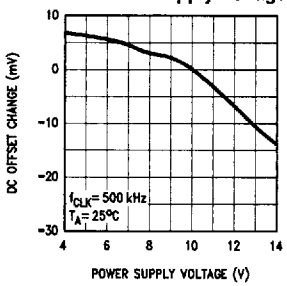
Positive Voltage Swing vs Temperature



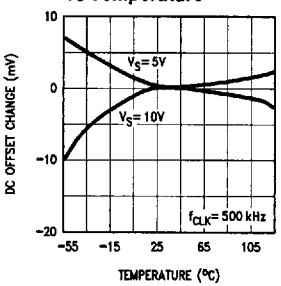
Negative Voltage Swing vs Temperature



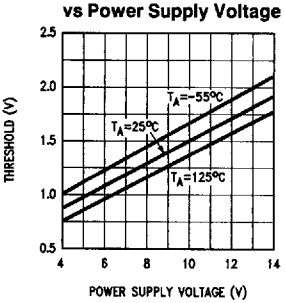
DC Offset Voltage Deviation vs Power Supply Voltage



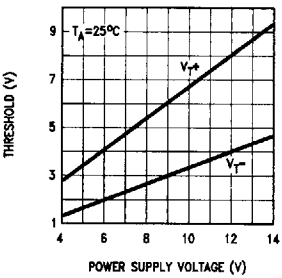
DC Offset Voltage Deviation vs Temperature



CLK R Trigger Threshold vs Power Supply Voltage



Schmitt Trigger Threshold vs Power Supply Voltage



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Pin Descriptions

(Numbers in ( ) are for 14-pin package).

Pin #	Pin Name	Function
1 (1)	CLK IN	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self clocking Schmitt-trigger oscillator (see Section 1.1).
2 (3)	CLK R	A TTL logic level clock input when in split supply operation (± 2.0V to ± 7V) with L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^-. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see Section 1.1). The TTL input signal must not exceed the supply voltages by more than 0.2V.
3 (5)	L. Sh	Level shift pin; selects the logic threshold levels for the clock. When tied to V^- it enables an internal TRI-STATE® buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output. When the voltage level at this input exceeds 25% $(V^+ - V^-) + V^-$ the internal TRI-STATE buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level-shift stage. The CLK R threshold level is now 2V above the voltage on the L. Sh pin. The CLK R pin will be compatible with TTL logic levels when the LMF40 is operated on split supplies with the L. Sh pin connected to system ground.
5 (8)	FILTER OUT	The output of the low-pass filter.
6 (10)	AGND	The analog ground pin. This pin sets the DC bias level for the filter section and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see Section 1.2). When tied to mid-supply this pin should be well bypassed.
7, 4 (7, 12)	V^+, V^-	The positive and negative supply pins. The total power supply range is 4V, to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
8 (14)	FILTER IN	The input to the low-pass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (see Section 3). For single supply operation the input signal must be biased to mid-supply or AC coupled through a capacitor.

1.0 LMF40 Application Information

The LMF40 is a non-inverting unity gain low-pass fourth-order Butterworth switched-capacitor filter. The switched-capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock-to-cutoff-frequency ratio (f_{CLK}/f_c) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock-to-cutoff-frequency ratio the closer this approximation is to the theoretical Butterworth response.

1.1 CLOCK INPUTS

The LMF40 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. Pin 3 is connected to V^-, making Pin 2 a low impedance output. The oscillator's frequency is nominally

$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{t-}}{V_{CC} - V_{t+}}\right)\left(\frac{V_{t+}}{V_{t-}}\right)\right]} \quad (1)$$

which is typically

$$f_{CLK} \cong \frac{1}{1.37\,RC} \quad (1a)$$

for $V_{CC} = 10$V.

Note that f_{CLK} is dependent on the buffer's threshold levels as well as the resistor/capacitor tolerance (see *Figure 1*). Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accurate cutoff frequency is required, an external clock can be used to drive the CLK R input of the LMF40. This input is TTL logic level compatible and also presents a very light load to the external clock source (~ 2 μA). With split supplies and the level shift (L. Sh) tied to system ground, the logic level is about 2V. (See the Pin Description for L. Sh).

1.0 LMF40 Application Information (Continued)

1.2 POWER SUPPLY

The LMF40 can be powered from a single supply or split supplies. The split supply mode shown in *Figure 2* is the most flexible and easiest to implement. Supply voltages of ±5V to ±7V enable the use of TTL or CMOS clock logic levels. *Figure 3* shows AGND resistor-biased to $V^+/2$ for single supply operation. In this mode only CMOS clock logic levels can be used, and input signals should be capacitor-coupled or biased near mid-supply.

1.3 INPUT IMPEDANCE

The LMF40 low-pass filter input (FILTER IN) is not a high impedance buffer input. This input is a switched-capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the filter's input can be seen in *Figure 4*. The input capacitor charges to V_{IN} during the first half of the clock period; during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{IN} V_{IN}$, and since current is defined as the flow of charge per unit time, the average input current becomes

$$I_{IN} = Q/T$$

(where T equals one clock period) or

$$I_{IN\,AVE} = \frac{C_{IN} V_{IN}}{T} = C_{IN} V_{IN} f_{CLK}$$

The equivalent input resistor (R_{IN}) then can be expressed as

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{1}{C_{IN} f_{CLK}}$$

The input capacitor is 2 pF for the LMF40-50 and 1 pF for the LMF40-100, so for the LMF40-100

$$R_{IN} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_c \times 100} = \frac{1 \times 10^{10}}{f_c}$$

and

$$R_{IN} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

for the LMF40-50. The above equation shows that for a given cutoff frequency (f_c), the input resistance of the LMF40-50 is the same as that of the LMF40-100. The higher the clock-to-cutoff-frequency ratio, the greater equivalent input resistance for a given clock frequency.

This input resistance will form a voltage divider with the source impedance (R_{Source}). Since R_{IN} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to attenuate the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity, the overall gain is given by:

$$A_V = \frac{R_{IN}}{R_{IN} + R_{Source}}$$

If the LMF40-50 or the LMF40-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{IN} = \frac{1 \times 10^{10}}{10\ \text{kHz}} = 1\ \text{M}\Omega$$

As an example, with a source impedance of 10 kΩ the overall gain would be:

$$A_V = \frac{1\ \text{M}\Omega}{10\ \text{k}\Omega + 1\ \text{M}\Omega} = 0.99009 \text{ or } -0.086\ \text{dB}$$

Since the maximum overall gain error for the LMF40 is +0.05, −0.15 dB @ 25°C with $R_S \leq 2$ kΩ the actual gain error for this case would be −0.04 dB to −0.24 dB.

1.4 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit due to leakage currents through the internal switches draining the charge stored on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error. For example:

$$f_{CLK} = 100\ \text{Hz},\ I_{Leakage} = 1\ \text{pA},\ C = 1\ \text{pF}$$

$$V = \frac{1\ \text{pA}}{1\ \text{pF}\ (100\ \text{Hz})} = 10\ \text{mV}$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors limit the filter's accuracy at high clock frequencies. The amplitude characteristic on ±5V supplies will typically stay flat until f_{CLK} exceeds 1.5 MHz and then peak at about 0.1 dB at the corner frequency with a 2 MHz clock. As supply voltage drops to ±2.5V, a shift in the f_{CLK}/f_c ratio occurs which will become noticeable when the clock frequency exceeds 500 kHz. The response of the LMF40 is still a good approximation of the ideal Butterworth low-pass characteristic shown in *Figure 5*.

2.0 Designing with the LMF40

Given any low-pass filter specification, two equations will come in handy in trying to determine whether the LMF40 will do the job. The first equation determines the order of the low-pass filter required to meet a given response specification:

$$n = \frac{\log\left[(10^{0.1A_{min}} - 1)/(10^{0.1A_{max}} - 1)\right]}{2 \log\left(f_s/f_b\right)} \qquad (2)$$

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at cutoff frequency f_b (Note 15). If the result of this equation is greater than 4, more than one LMF40 will be required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}\,(f) = 10 \log\left[1 + (10^{0.1A_{max}} - 1)(f/f_b)^{2n}\right]\text{dB} \qquad (3)$$

where n = 4 for the LMF40.

2.1 A LOW-PASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 6* is given. Can the LMF40 be used? The order of the Butterworth approximation will have to be determined using (1):

$$A_{min} = 18\ \text{dB},\ A_{max} = 1.0\ \text{dB},\ f_s = 2\ \text{kHz},\ \text{and}\ f_b = 1\ \text{kHz}$$

$$n = \frac{\log\left[(10^{1.8} - 1)/(10^{0.1} - 1)\right]}{2 \log(2)} = 3.95$$

Since n can only take on integer values, n = 4. Therefore the LMF40 can be used. In general, if n is 4 or less a single LMF40 can be utilized.

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2.0 Designing with the LMF40 (Continued)

Likewise, the attenuation at f_s can be found using (3) with the above values and n = 4:

$$\text{Attn (2 kHz)} = 10 \log[1 + 10^{0.1} - 1)\,(2\text{ kHz}/1\text{ kHz})^8]$$
$$= 18.28\text{ dB}$$

This result also meets the design specification given in *Figure 6* again verifying that a single LMF40 section will be adequate.

Since the LMF40's cutoff frequency (f_c), which corresponds to a gain attenuation of −3.01 dB, was not specified in this example, it needs to be calculated. Solving equation (3) where f = f_c as follows:

$$f_c = f_b\left[\frac{10^{0.1(3.01\text{ dB})} - 1}{(10^{0.1A_{max}} - 1)}\right]^{1/(2n)}$$
$$= 1\text{ kHz}\left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/8}$$
$$= 1.184\text{ kHz}$$

where $f_c = f_{CLK}/50$ or $f_{CLK}/100$. To implement this example for the LMF40-50 the clock frequency will have to be set to f_{CLK} = 50(1.184 kHz) = 59.2 kHz, or for the LMF40-100, f_{CLK} = 100 (1.184 kHz) = 118.4 kHz.

2.2 CASCADING LMF40s

When a steeper stopband attenuation rate is required, two LMF40s can be cascaded *(Figure 7)* yielding an 8th order slope of 48 dB per octave. Because the LMF40 is a Butterworth filter and therefore has no ripple in its passband, when LMF40s are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 8a*.

In determining whether the cascaded LMF40s will yield a filter that will meet a particular amplitude response specification, as above, equations (4) and (5) can be used, shown below.

$$n = \frac{\log[(10,^{0.05A_{min}} - 1)/(10^{0.05A_{max}} - 1)]}{2\log(f_s/f_b)} \quad (4)$$

$$\text{Attn (f)} = 10\log[1 + (10^{0.05A_{max}} - 1)\,(f/f_b)^2]\text{dB} \quad (5)$$

where n = 4 (the order of each filter).

Equation (4) will determine whether the order of the filter is adequate (n ≤ 4) while equation (5) can determine the actual stopband attenuation and cutoff frequency (f_c) necessary to obtain the desired frequency response. The design procedure would be identical to the one shown in Section 2.0.

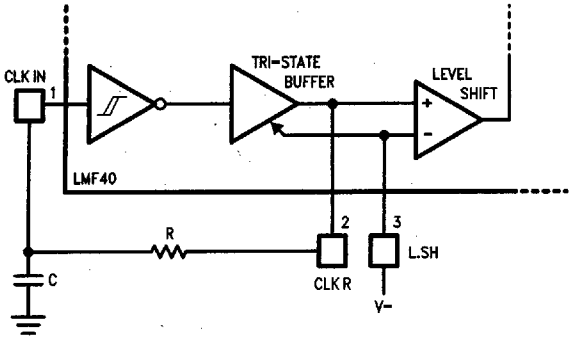
2.3 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The LMF40 responds well to an instantaneous change in clock frequency. If the control signal in *Figure 9* is low the LMF40-50 has a 100 kHz clock making f_c = 2 kHz; when this signal goes high the clock frequency changes to 50 kHz yielding f_c = 1 kHz. As *Figure 9* illustrates, the output signal changes quickly and smoothly in response to a sudden change in clock frequency.

The step response of the LMF40 in *Figure 10* is dependent on f_c. The LMF40 responds as a classical fourth-order Butterworth low-pass filter.

2.4 ALIASING CONSIDERATIONS

Aliasing effects have to be considered when input signal frequencies exceed half the sampling rate. For the LMF40 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency $f_{CLK}/2$, as in *Figure 11a*, that component will be "reflected" about $f_{CLK}/2$ into the frequency range below $f_{CLK}/2$, as in *Figure 11b*. If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore, if frequency components in the input signal exceed $f_{CLK}/2$ they must be attenuated before being applied to the LMF40 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level.



$$f = \frac{1}{RC\ln\left[\left(\frac{V_{CC} - V_{t-}}{V_{CC} - V_{t+}}\right)\left(\frac{V_{t+}}{V_{t-}}\right)\right]}$$

$$f \cong \frac{1}{1.37\,RC}$$

(V_{CC} = 10V)

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FIGURE 1. Schmitt Trigger R/C Oscillator

2.0 Designing with the LMF40 (Continued)

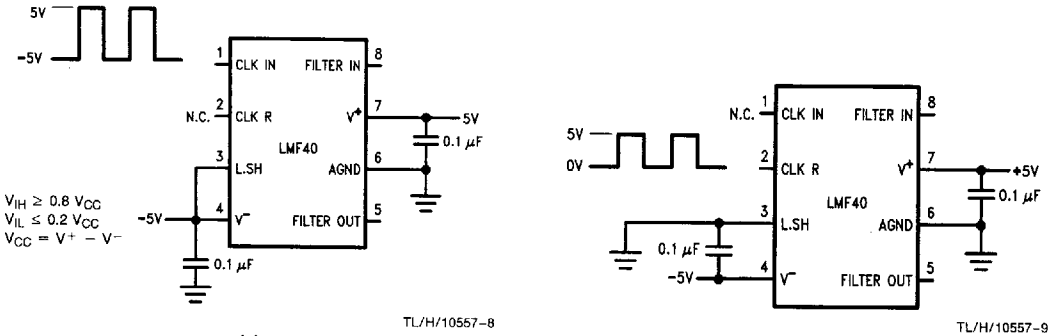

FIGURE 2. Split Supply Operation with CMOS Level Clock (a), and TTL Level Clock (b)

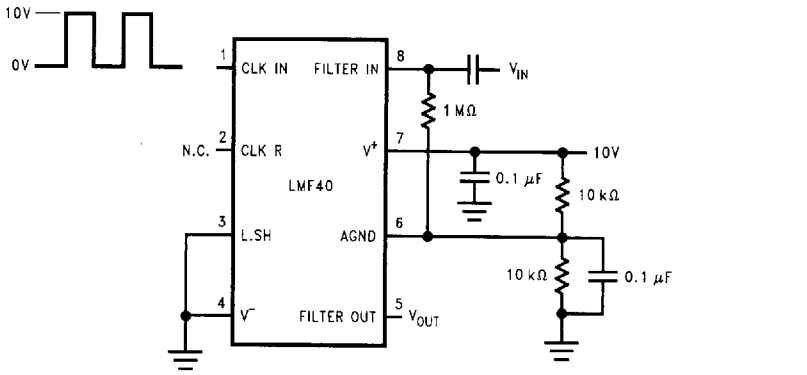

FIGURE 3. Single Supply Operation. AGND Resistor Biased to $V^+/2$

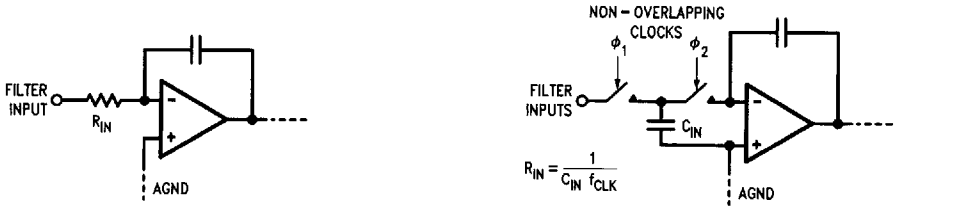

FIGURE 4. LMF40 Filter Input

2.0 Designing with the LMF40 (Continued)

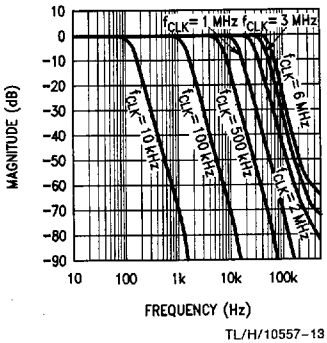

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FIGURE 5a. LMF40-100 Amplitude Response with ±5V Supplies

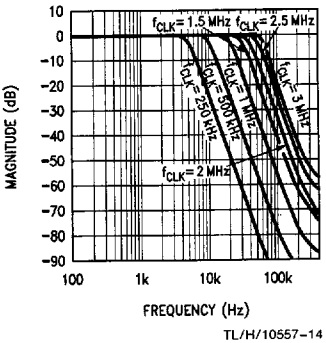

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FIGURE 5b. LMF40-50 Amplitude Response with ±5V Supplies

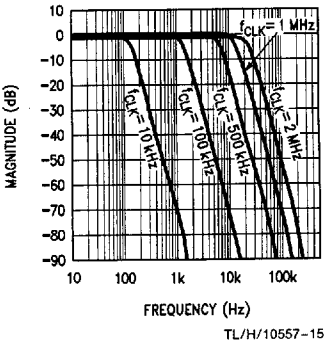

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FIGURE 5c. LMF40-100 Amplitude Response with ±2.5V Supplies

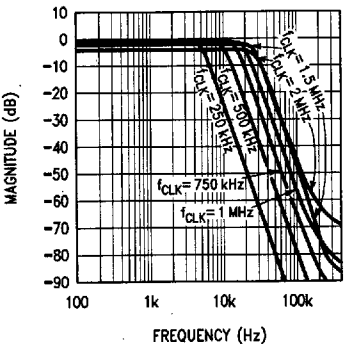

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FIGURE 5d. LMF40-50 Amplitude Response with ±2.5V Supplies

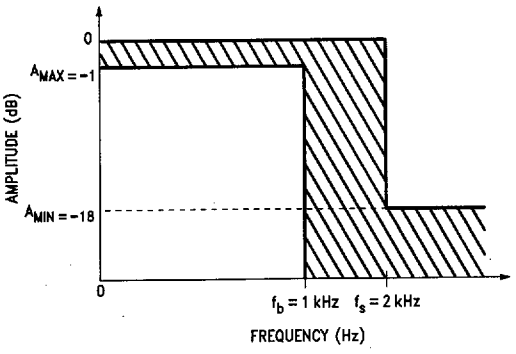

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FIGURE 6. Design Example Magnitude Response Specification. The response of the filter design must fall within the shaded area of the specification.

2.0 Designing with the LMF40 (Continued)

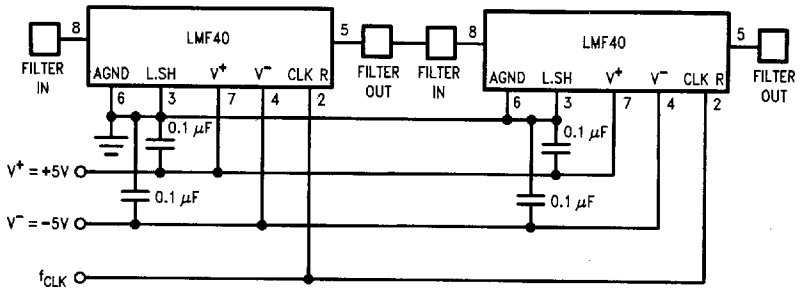

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FIGURE 7. Cascading Two LMF40s

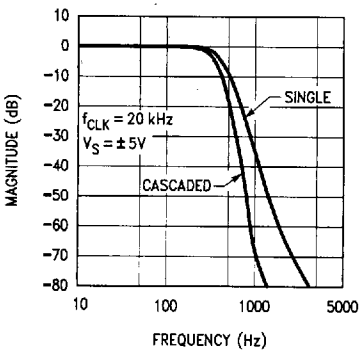

FIGURE 8a. One LMF40-50 vs Two LMF40-50s Cascaded

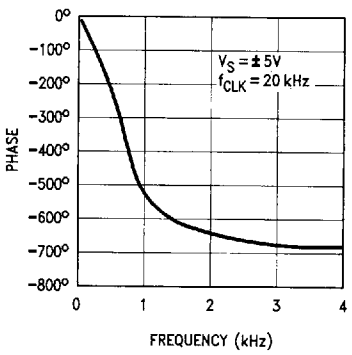

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FIGURE 8b. Phase Response of Two Cascaded LMF40-50s

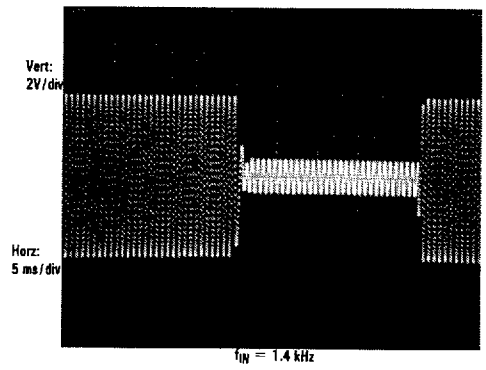

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FIGURE 9. LMF40-50 Abrupt Clock Frequency Change

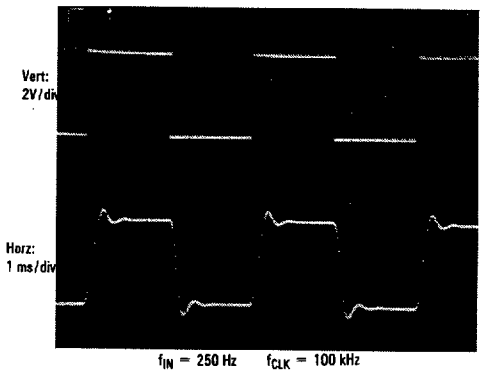

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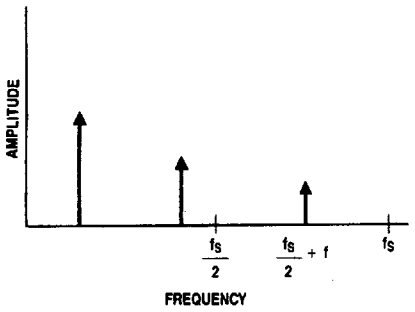
FIGURE 10. LMF40-50 Input Step Response

2.0 Designing with the LMF40 (Continued)



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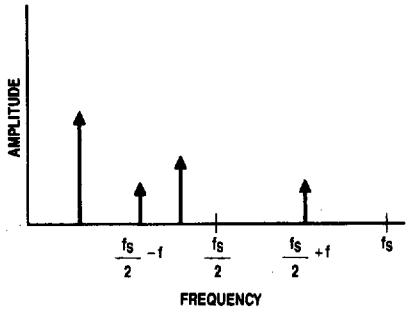
(a) Input Signal Spectrum



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(b)Output Signal Spectrum. Note that the input signal at $f_S/2 + f$ causes an output signal to appear at $f_S/2 - f$.

FIGURE 11. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the LMF40, $f_S = f_{CLK}$.