HARRIS SEMICONDUCTOR

HSP43168

December 1996

Dual FIR Filter

Features

- **Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR**
- **10-Bit Data and Coefficients**
- **On-Board Storage for 32 Programmable Coefficient Sets**
- **Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 19-Bit Data and Coefficients**
- **Programmable Decimation to 16**
- **Programmable Rounding on Output**
- **Standard Microprocessor Interface**

Applications

- **Quadrature, Complex Filtering**
- **Image Processing**
- **Polyphase Filtering**
- **Adaptive Filtering**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43168VC-33	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168VC-40	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168VC-45	0 to 70	100 Ld MQFP	Q100.14x20
HSP43168JC-33	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JC-40	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JC-45	0 to 70	84 Ld PLCC	N84.1.15
HSP43168JI-40	-40 to 85	84 Ld PLCC	N84.1.15
HSP43168GC-33	0 to 70	84 Ld CPGA	G84.A
HSP43168GC-45	0 to 70	84 Ld CPGA	G84.A

Description

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

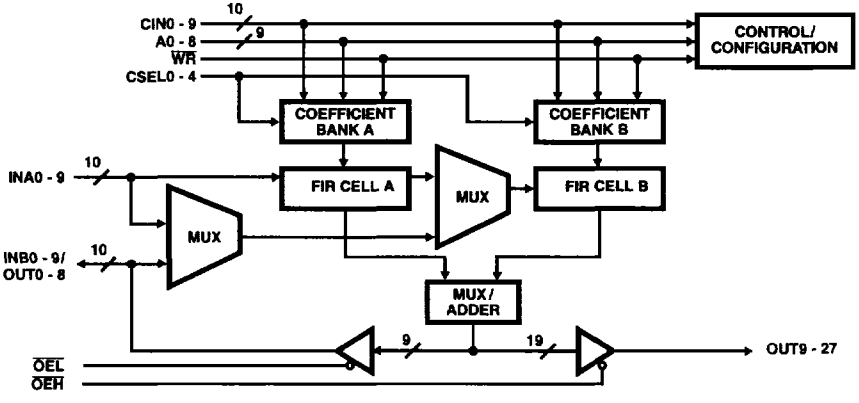
The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the decimation registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16x16

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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