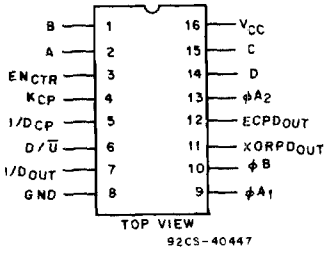
# CD54/74HC297
# CD54/74HCT297

File Number **1852**

## High-Speed CMOS Logic




**TERMINAL ASSIGNMENT**

## Digital Phase-Locked-Loop Filter

**Type Features:**

- *Digital design avoids analog compensation errors*
- *Easily cascadable for higher order loops*
- *Useful frequency range:*
  *DC to 55 MHz typical (k-clock)*
  *DC to 35 MHz typical (I/D-clock)*
- *Dynamically variable bandwidth*
- *Very narrow bandwidth attainable*
- *Power-on reset*
- *Output capability:*
  *Standard - $XORPD_{OUT}$, $ECPD_{OUT}$*
  *Bus driver - $I/D_{OUT}$*

The RCA-CD54/74HC/HCT297 are high-speed silicon-gate CMOS devices that are pin-compatible with low power Schottky TTL (LSTTL).

These devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. They contain all the necessary circuits, with the exception of the divide-by-N counter, to build first-order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled phase detectors (ECPD) are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

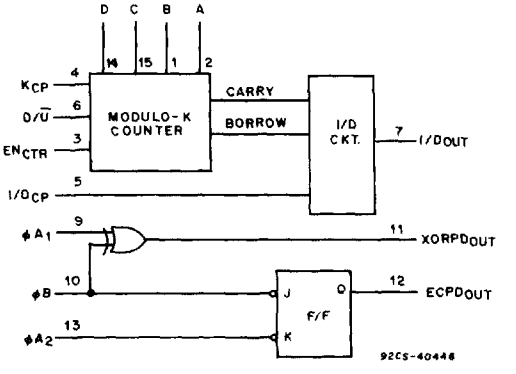
Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 2) or to cascade to higher order phase-locked-loops.

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengths the lock time. Real-time control of loop bandwidth by manipulating the A to D inputs can maximum the overall performance of the digital phase-locked-loop.

The CD54/74HC/HCT297 can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by VCC and temperature variations but depends solely on accuracies of the K-clock and loop propagation delays.

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity:*
  *$N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$; @ $V_{CC}$ = 5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$ = 0.8 V Max., $V_{IH}$ = 2 V Min.*
  *CMOS Input Compatibility*
  *$I_I \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*




**FUNCTIONAL DIAGRAM**

# CD54/74HC297
# CD54/74HCT297

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error ($\phi$IN - $\phi$OUT). Within these limits the phase detector output varies linearly with the input phase error according to the gain $K_d$, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{phase detector output} = \frac{\%\text{HIGH} - \%\text{LOW}}{100}$$

The output of the phase detector will be $K_d\phi_e$, where the phase error

$\phi_e = \phi_{IN} - \phi_{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain ($K_d$) for an XORPD is 4 because its output remains HIGH ($XORPD_{OUT}$ = 1) for a phase error of ¼ cycle.

Similarly, $K_d$ for the ECPD is 2 since its output remains HIGH for a phase error of ½ cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a $\phi_e$ defined to be zero. For the basic DPLL system of Fig. 3, $\phi_e$ = 0 when the phase detector output is a square wave.

The XORPD inputs are ¼ cycle out-of-phase for zero phase error. For the ECPD, $\phi_e$ = 0 when the inputs are ½ cycle out of phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency $Mf_c$ which is a multiple M of the loop center frequency $f_c$. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio $Mf_c/K$, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(K_d\phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is ½ of the input clock ($I/D_{CP}$). The input clock is just a multiple, 2N, of the loop center frequency. In response to a carry of borrow pulse, the I/D circuit will either add or delete a pulse at $I/D_{OUT}$. Thus the output of the I/D circuit will be $Nf_c + (K_d\phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus:

$f_o = f_c + (K_d\phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or $f_c/K$ for M = 2N.

Thus, the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

The CD54HC297 and CD54HCT297 are supplied in 16-lead hermetic dual-in-line frit-seal ceramic packages (F suffix). The CD74HC297 and CD74HCT297 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

**K COUNTER FUNCTION TABLE**
**(DIGITAL CONTROL)**

| D | C | B | A | MODULO (K) |
|---|---|---|---|---|
| L | L | L | L | Inhibited |
| L | L | L | H | $2^3$ |
| L | L | H | L | $2^4$ |
| L | L | H | H | $2^5$ |
| L | H | L | L | $2^6$ |
| L | H | L | H | $2^7$ |
| L | H | H | L | $2^8$ |
| L | H | H | H | $2^9$ |
| H | L | L | L | $2^{10}$ |
| H | L | L | H | $2^{11}$ |
| H | L | H | L | $2^{12}$ |
| H | L | H | H | $2^{13}$ |
| H | H | L | L | $2^{14}$ |
| H | H | L | H | $2^{15}$ |
| H | H | H | L | $2^{16}$ |
| H | H | H | H | $2^{17}$ |

**FUNCTION TABLE**
**EXCLUSIVE-OR PHASE DETECTOR**

| $\phi A_1$ | $\phi B$ | XORPD OUT |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

**FUNCTION TABLE**
**EDGE-CONTROLLED PHASE DETECTOR**

| $\phi A_2$ | $\phi B$ | ECPD OUT |
|---|---|---|
| H or L | ↘ | H |
| ↘ | H or L | L |
| H or L | ↗ | No Change |
| ↗ | H or L | No Change |

H = steady-state high level
L = steady-state low level
↘ = transition from high to low
↗ = transition from low to high

# CD54/74HC297
# CD54/74HCT297

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CD74HC297/CD54HC297 | | | | | | | | | | | CD74HCT297/CD54HCT297 | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | | 74HC/54HC TYPES | | | 74HC TYPES | | 54HC TYPES | | TEST CONDITIONS | | 74HCT/54HCT TYPES | | | 74HCT TYPES | | 54HCT TYPES | | |
| | | | | | +25°C | | | -40/ +85°C | | -55/ +125°C | | | | +25°C | | | -40/ +85°C | | -55/ +125°C | | |
| | $V_I$ V | $I_O$ mA | | $V_{CC}$ V | Min | Typ | Max | Min | Max | Min | Max | $V_I$ V | $V_{CC}$ V | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 to 5.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | | | | | | | | |
| | | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | | 2 | — | — | 0.5 | — | 0.5 | — | 0.5 | — | 4.5 to 5.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | | 4.5 | — | — | 1.35 | — | 1.35 | — | 1.35 | | | | | | | | | | |
| | | | | 6 | — | — | 1.8 | — | 1.8 | — | 1.8 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | -0.02 | | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | | | | | | | |
| TTL Loads Bus Driver and Standard Output | $V_{IL}$ or $V_{IH}$ | # -4 -5.2 | I/D -6 -7.8 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | | | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | | | | | | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | 0.02 | | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| | | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| TTL Loads Bus Driver and Standard Output | $V_{IL}$ or $V_{IH}$ | # 4 5.2 | I/D 6 7.8 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | | | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | | | | | | | |
| Input Leakage Current $I_I$ | $V_{CC}$ or Gnd | | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | Any Voltage Between $V_{CC}$ & Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | 0 | | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Device Current per input pin: 1 unit load $\Delta I_{CC}$* | | | | | | | | | | | | $V_{CC}$ -2.1 | 4.5 to 5.5 | — | 100 | 360 | — | 450 | — | 490 | μA |

*For dual-supply systems theoretical worst case ($V_I$ = 2.4 V, $V_{CC}$ = 5.5 V) specification is 1.8 mA.

# XORPD, ECPD

### HCT INPUT LOADING TABLE

| INPUT | UNIT LOADS * |
|---|---|
| $EN_{CTR}$, $D/\overline{U}$ | 0.3 |
| A, B, C, D, $K_{CP}$, $\phi A_2$ | 0.6 |
| $I/D_{CP}$, $\phi A_1$, $\phi B$ | 1.5 |

* Unit Load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

# CD54/74HC297
# CD54/74HCT297

## PRE-REQUISITE FOR SWITCHING FUNCTION

| CHARACTERISTIC | | $V_{CC}$ | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | |
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Maximum Clock | | 2 | 6 | — | — | — | 5 | — | — | — | 4 | — | — | — | |
| Frequency | $f_{MAX}$ | 4.5 | 30 | — | 30 | — | 24 | — | 24 | — | 20 | — | 20 | — | MHz |
| $K_{CP}$ | | 6 | 35 | — | — | — | 28 | — | — | — | 24 | — | — | — | |
| | | 2 | 4 | — | — | — | 3 | — | — | — | 2 | — | — | — | |
| $1/D_{CP}$ | | 4.5 | 20 | — | 20 | — | 16 | — | 16 | — | 13 | — | 13 | — | MHz |
| | | 6 | 24 | — | — | — | 19 | — | — | — | 15 | — | — | — | |
| Clock Pulse Width | $t_w$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | |
| | | 4.5 | 16 | — | 16 | — | 20 | — | 20 | — | 24 | — | 24 | — | ns |
| $K_{CP}$ | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |
| | | 2 | 125 | — | — | — | 155 | — | — | — | 190 | — | — | — | |
| $1/D_{CP}$ | | 4.5 | 25 | — | 25 | — | 31 | — | 31 | — | 38 | — | 38 | — | ns |
| | | 6 | 21 | — | — | — | 26 | — | — | — | 32 | — | — | — | |
| Setup Time | | 2 | 100 | — | — | — | 125 | — | — | — | 150 | — | — | — | |
| $D/\overline{U}$, $EN_{CTR}$ to $K_{CP}$ | $t_{SU}$ | 4.5 | 20 | — | 20 | — | 25 | — | 25 | — | 30 | — | 30 | — | ns |
| | | 6 | 17 | — | — | — | 21 | — | — | — | 26 | — | — | — | |
| Hold Time | | 2 | 0 | — | — | — | 0 | — | — | — | 0 | — | — | — | |
| $D/\overline{U}$, $EN_{CTR}$ to $K_{CP}$ | $t_H$ | 4.5 | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| | | 6 | 0 | — | — | — | 0 | — | — | — | 0 | — | — | — | |

## SWITCHING CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$, $t_f$ = 6 ns)

| CHARACTERISTIC | | $V_{CC}$ | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | |
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay, | $t_{PLH}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | |
| $I/D_{CP}$ to $I/D_{OUT}$ | $t_{PHL}$ | 4.5 | — | 35 | — | 35 | — | 44 | — | 44 | — | 53 | — | 53 | |
| | | 6 | — | 30 | — | — | — | 34 | — | — | — | 43 | — | — | |
| | | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | |
| $\phi A_1$, $\phi B$ to $XORPD_{OUT}$ | | 4.5 | — | 30 | — | 30 | — | 38 | — | 38 | — | 45 | — | 45 | |
| | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| | | 2 | — | 200 | — | — | — | 250 | — | — | — | 300 | — | — | |
| $\phi B$, $\phi A_2$ to $ECPD_{OUT}$ | | 4.5 | — | 40 | — | 40 | — | 50 | — | 50 | — | 60 | — | 60 | ns |
| | | 6 | — | 34 | — | — | — | 43 | — | — | — | 51 | — | — | |
| Output Transition Time | | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | |
| $XORPD_{OUT}$, | $t_{TLH}$ | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | |
| $ECPD_{OUT}$, | $t_{TLH}$ | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |
| | | 2 | — | 60 | — | — | — | 75 | — | — | — | 90 | — | — | |
| $I/D_{OUT}$ | | 4.5 | — | 12 | — | 12 | — | 15 | — | 15 | — | 18 | — | 18 | |
| | | 6 | — | 10 | — | — | — | 13 | — | — | — | 15 | — | — | |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | pF |

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# CD54/74HCT297

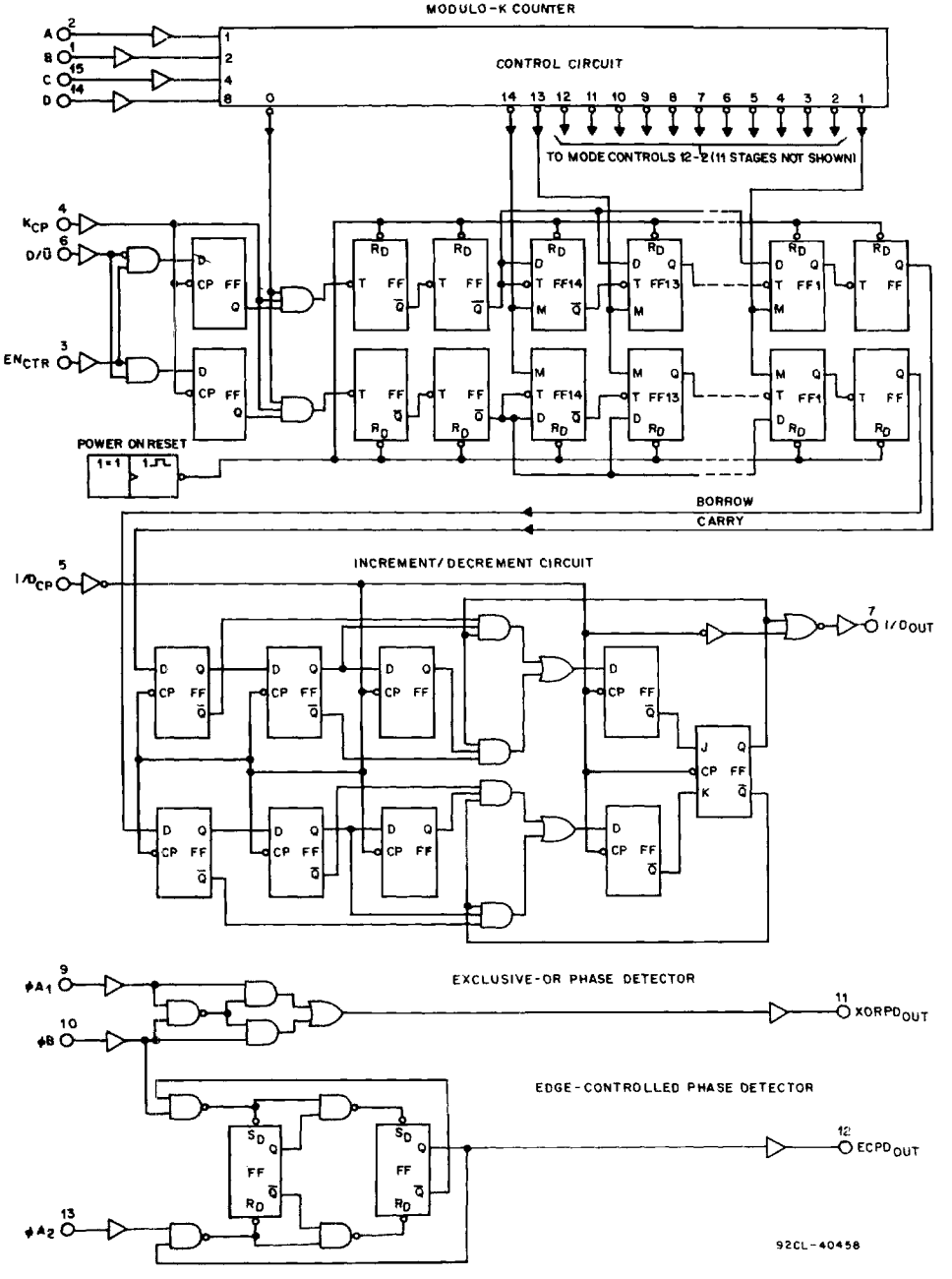



*Fig. 1 - Logic diagram.*

# CD54/74HC297
# CD54/74HCT297

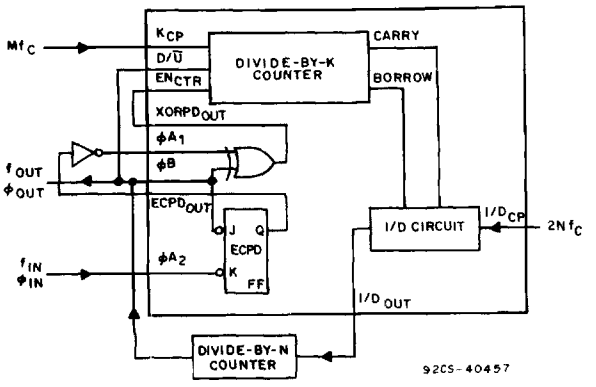



*Fig. 2 - DPLL using both phase detectors in a ripple-cancellation scheme.*

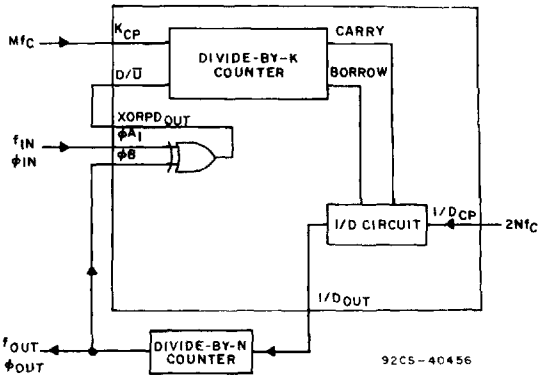



*Fig. 3 - DPLL using EXCLUSIVE-OR phase detection.*

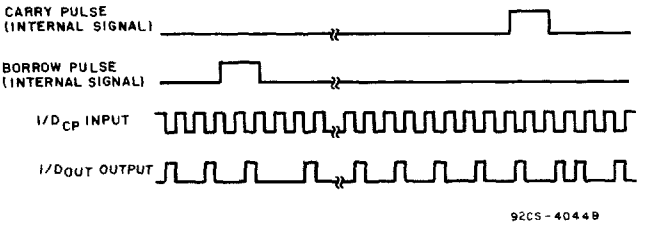



*Fig. 4 - Timing diagram: $I/D_{OUT}$ in-lock condition.*

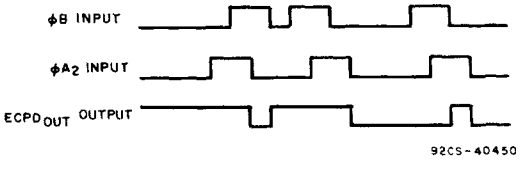



*Fig. 5 - Timing diagram: edge-controlled phase comparator waveforms.*

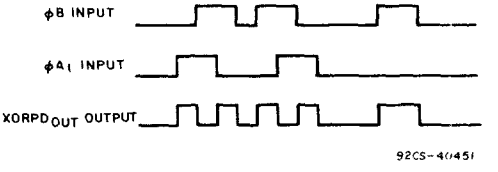



*Fig. 6 - Timing diagram: EXLUSIVE-OR phase detector waveforms.*

# CD54/74HC297
# CD54/74HCT297

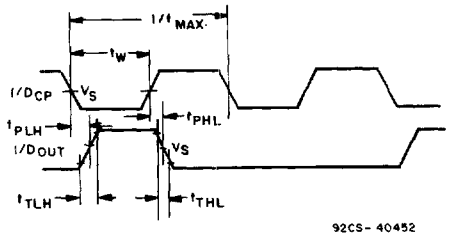



Fig. 7 - Waveforms showing the clock ($I/D_{CP}$) to output ($I/D_{OUT}$) propagation delays, clock pulse width, output transition times and maximum clock pulse frequency.

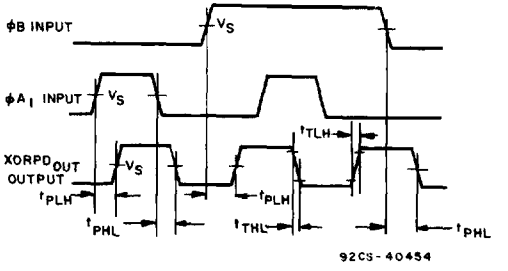



Fig. 8 - Waveforms showing the phase input ($\phi B$, $\phi A_1$) to output ($XORPD_{OUT}$) propagation delays and output transition times.

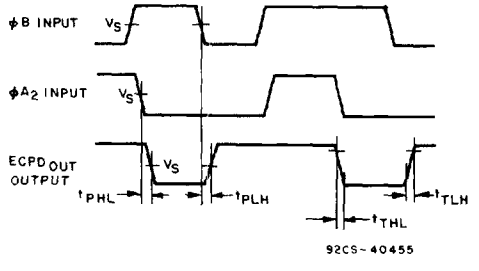
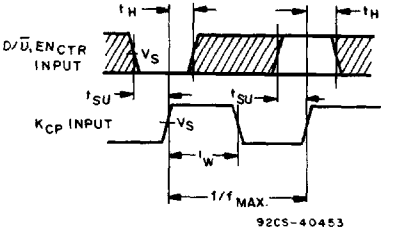



Fig. 9 - Waveforms showing the phase input ($\phi B$, $\phi A_2$) to output ($ECPD_{OUT}$) propagation delays and output transition times.




NOTE: THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE.

Fig. 10 - Waveforms showing the clock ($K_{CP}$) pulse width and maximum clock pulse frequency, and the input ($D/\overline{U}$, $EN_{CTR}$) to clock ($K_{CP}$) set-up and hold times.

| | 54/74HC | 54/74HCT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| Switching Voltage, $V_S$ | 50% $V_{CC}$ | 1.3 V |