Clock-Tunable, Quad Second Order, Filter Building Blocks

FEATURES

- **Four Identical 2nd Order Filter Sections in an SSOP Package**
- **2nd Order Section Center Frequency Error: ±0.3% Typical and ±0.8% Maximum**
- **Low Noise per 2nd Order Section, Q ≤ 5: LTC1068-200 50μV_{RMS}, LTC1068 50μV_{RMS} LTC1068-50 75μV_{RMS}, LTC1068-25 90μV_{RMS}**
- Low Power Supply Current: 4.5mA, Single 5V, LTC1068-50
- Operation with ±5V Power Supply, Single 5V Supply or Single 3.3V Supply

APPLICATIONS

- Lowpass or Highpass Filters: LTC1068-200, 0.5Hz to 25kHz; LTC1068, 1Hz to 50kHz; LTC1068-50, 2Hz to 50kHz; LTC1068-25, 4Hz to 200kHz
- Bandpass or Bandreject (Notch) Filters: LTC1068-200, 0.5Hz to 15kHz; LTC1068, 1Hz to 30kHz; LTC1068-50, 2Hz to 30kHz; LTC1068-25, 4Hz to 140kHz

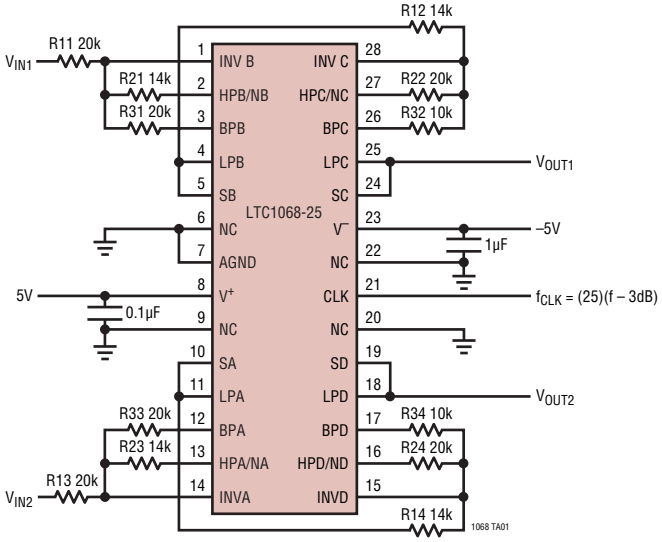
DESCRIPTION

The LTC®1068 product family consists of four monolithic clock-tunable filter building blocks. Each product contains four matched, low noise, high accuracy 2nd order switched-capacitor filter sections. An external clock tunes the center frequency of each 2nd order filter section. The LTC1068 products differ only in their clock-to-center frequency ratio. The clock-to-center frequency ratio is set to 200:1 (LTC1068-200), 100:1 (LTC1068), 50:1 (LTC1068-50) or 25:1 (LTC1068-25). External resistors can modify the clock-to-center frequency ratio. High performance, quad 2nd order, dual 4th order or 8th order filters can be designed with an LTC1068 family product. Designing filters with an LTC1068 product is fully supported by FilterCAD™ filter design software for Windows.

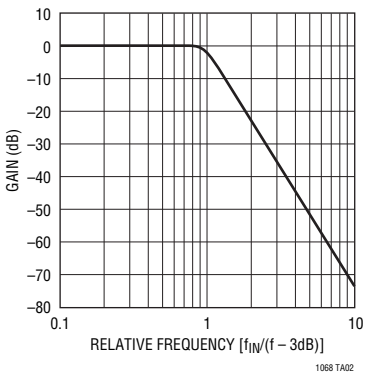
The LTC1068 products are available in a 28-pin SSOP surface mount package. A customized version of an LTC1068 family product can be obtained in a 16-lead SO package with internal thin-film resistors. Please contact LTC Marketing for details.

TYPICAL APPLICATION

Dual, Matched, 4th Order Butterworth Lowpass Filters, Clock-Tunable Up to 200kHz f – 3dB = f_{CLK}/25, 4th Order Filter Noise = 60μV_{RMS}



Gain vs Frequency

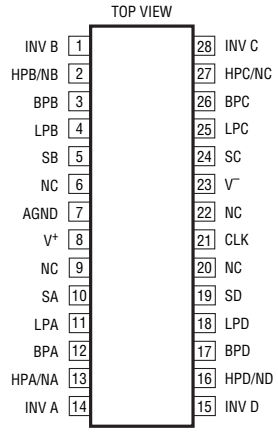


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12V
Power Dissipation 500mW
Input Voltage at Any Pin..... $V^- - 0.3V \le V_{IN} \le V^+ + 0.3V$
Storage Temperature Range..... –65°C to 150°C

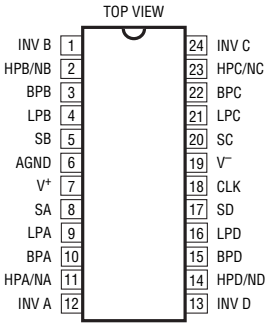
Operating Temperature Range
LTC1068C ..... 0°C to 70°C
LTC1068I..... –40°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 110°C, θ_{JA} = 95°C/W



N PACKAGE
24-LEAD PDIP

T_{JMAX} = 110°C, θ_{JA} = 65°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1068CG#PBF	LTC1068CG#TRPBF	LTC1068	28-Lead Plastic SSOP	0°C to 70°C
LTC1068IG#PBF	LTC1068IG#TRPBF	LTC1068	28-Lead Plastic SSOP	–40°C to 85°C
LTC1068-200CG#PBF	LTC1068-200CG#TRPBF	LTC1068	28-Lead Plastic SSOP	0°C to 70°C
LTC1068-200IG#PBF	LTC1068-200IG#TRPBF	LTC1068	28-Lead Plastic SSOP	–40°C to 85°C
LTC1068-50CG#PBF	LTC1068-50CG#TRPBF	LTC1068	28-Lead Plastic SSOP	0°C to 70°C
LTC1068-50IG#PBF	LTC1068-50IG#TRPBF	LTC1068	28-Lead Plastic SSOP	–40°C to 85°C
LTC1068-25CG#PBF	LTC1068-25CG#TRPBF	LTC1068	28-Lead Plastic SSOP	0°C to 70°C
LTC1068-25IG#PBF	LTC1068-25IG#TRPBF	LTC1068	28-Lead Plastic SSOP	–40°C to 85°C
LTC1068CN#PBF	NA	LTC1068	24-Lead PDIP	0°C to 70°C
LTC1068IN#PBF	NA	LTC1068	24-Lead PDIP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

LTC1068 (Internal Op Amps). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			3.14		±5.5	V
Voltage Swings	V_S = 3.14V, R_L = 5k (Note 2) V_S = 4.75V, R_L = 5k (Note 3) V_S = ±5V, R_L = 5k	● ● ●	1.2 2.6 ±3.4	1.6 3.2 ±4.1		V_{P-P} V_{P-P} V
Output Short-Circuit Current (Source/Sink)	V_S = ±4.75V V_S = ±5V			17/6 20/15		mA mA
DC Open-Loop Gain	R_L = 5k			85		dB
GBW Product	V_S = ±5V			6		MHz
Slew Rate	V_S = ±5V			10		V/µs
Analog Ground Voltage (Note 4)	V_S = 5V, Voltage at AGND			2.5V ±2%		V

LTC1068 (Complete Filter) V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Center Frequency Ratio (Note 5)	V_S = 4.75V, f_{CLK} = 1MHz, Mode 1 (Note 3), f_0 = 10kHz, Q = 5, V_{IN} = 0.5V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	●		100 ±0.3	100 ±0.8 100 ±0.9	% %
	V_S = ±5V, f_{CLK} = 1MHz, Mode 1, f_0 = 10kHz, Q = 5, V_{IN} = 1V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	●		100 ±0.3	100 ±0.8 100 ±0.9	% %
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 5)	V_S = 4.75V, f_{CLK} = 1MHz, Q = 5 (Note 3) V_S = ±5V, f_{CLK} = 1MHz, Q = 5	● ●		±0.25 ±0.25	±0.9 ±0.9	% %
Q Accuracy (Note 5)	V_S = 4.75V, f_{CLK} = 1MHz, Q = 5 (Note 3) V_S = ±5V, f_{CLK} = 1MHz, Q = 5	● ●		±1 ±1	±3 ±3	% %
f_0 Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (Note 5) (See Table 1)	V_S = ±5V, f_{CLK} = 1MHz, V_{OS1} (DC Offset of Input Inverter)	●		0	±15	mV
	V_S = ±5V, f_{CLK} = 1MHz, V_{OS2} (DC Offset of First Integrator)	●		±2	±25	mV
	V_S = ±5V, f_{CLK} = 1MHz, V_{OS3} (DC Offset of Second Integrator)	●		±5	±40	mV
Clock Feedthrough	V_S = ±5V, f_{CLK} = 1MHz			0.1		mV_{RMS}
Max Clock Frequency (Note 6)	V_S = ±5V, Q ≤ 2.0, Mode 1			5.6		MHz
Power Supply Current	V_S = 3.14V, f_{CLK} = 1MHz (Note 2) V_S = 4.75V, f_{CLK} = 1MHz (Note 3) V_S = ±5V, f_{CLK} = 1MHz	● ● ●		3.5 6.5 9.5	8 11 15	mA mA mA

ELECTRICAL CHARACTERISTICS

LTC1068-200 (Internal Op Amps). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			3.14		±5.5	V
Voltage Swings	V_S = 3.14V, R_L = 5k (Note 2) V_S = 4.75V, R_L = 5k (Note 3) V_S = ±5V, R_L = 5k	● ● ●	1.2 2.6 ±3.4	1.6 3.2 ±4.1		V_{P-P} V_{P-P} V
Output Short-Circuit Current (Source/Sink)	V_S = ±4.75V V_S = ±5V			17/6 20/15		mA mA
DC Open-Loop Gain	R_L = 5k			85		dB
GBW Product	V_S = ±5V			6		MHz
Slew Rate	V_S = ±5V			10		V/µs
Analog Ground Voltage (Note 4)	V_S = 5V, Voltage at AGND			2.5V ±2%		V

LTC1068-200 (Complete Filter) V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Center Frequency Ratio (Note 5)	V_S = 4.75V, f_{CLK} = 1MHz, Mode 1 (Note 3), f_O = 5kHz, Q = 5, V_{IN} = 0.5V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	● ●		200 ±0.3	200 ±0.8 200 ±0.9	% %
	V_S = ±5V, f_{CLK} = 1MHz, Mode 1, f_O = 5Hz, Q = 5, V_{IN} = 1V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	● ●		200 ±0.3	200 ±0.8 200 ±0.9	% %
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 5)	V_S = 4.75V, f_{CLK} = 1MHz, Q = 5 (Note 3) V_S = ±5V, f_{CLK} = 1MHz, Q = 5	● ●		±0.25 ±0.25	±0.9 ±0.9	% %
Q Accuracy (Note 5)	V_S = 4.75V, f_{CLK} = 1MHz, Q = 5 (Note 3) V_S = ±5V, f_{CLK} = 1MHz, Q = 5	● ●		±1 ±1	±3 ±3	% %
f_O Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (Note 5) (See Table 1)	V_S = ±5V, f_{CLK} = 1MHz, V_{OS1} (DC Offset of Input Inverter)	●		0	±15	mV
	V_S = ±5V, f_{CLK} = 1MHz, V_{OS2} (DC Offset of First Integrator)	●		±2	±25	mV
	V_S = ±5V, f_{CLK} = 1MHz, V_{OS3} (DC Offset of Second Integrator)	●		±5	±40	mV
Clock Feedthrough	V_S = ±5V, f_{CLK} = 1MHz			0.1		mV_{RMS}
Max Clock Frequency (Note 6)	V_S = ±5V, Q ≤ 2.0, Mode 1			5.6		MHz
Power Supply Current	V_S = 3.14V, f_{CLK} = 1MHz (Note 2) V_S = 4.75V, f_{CLK} = 1MHz (Note 3) V_S = ±5V, f_{CLK} = 1MHz	● ● ●		3.5 6.5 9.5	8 11 15	mA mA mA

ELECTRICAL CHARACTERISTICS

LTC1068-50 (Internal Op Amps). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			3.14		±5.5	V
Voltage Swings	V_S = 3.14V, R_L = 5k (Note 2) V_S = 4.75V, R_L = 5k (Note 3) V_S = ±5V, R_L = 5k	● ● ●	1.2 2.6 ±3.4	1.8 3.6 ±4.1		V_{P-P} V_{P-P} V
Output Short-Circuit Current (Source/Sink)	V_S = ±3.14V V_S = ±5V			17/6 20/15		mA mA
DC Open-Loop Gain	R_L = 5k			85		dB
GBW Product	V_S = ±5V			4		MHz
Slew Rate	V_S = ±5V			7		V/µs
Analog Ground Voltage (Note 4)	V_S = 5V, Voltage at AGND			2.175V ±2%		V

LTC1068-50 (Complete Filter) V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Center Frequency Ratio (Note 5)	V_S = 3.14V, f_{CLK} = 250kHz, Mode 1 (Note 2), f_O = 5kHz, Q = 5, V_{IN} = 0.34V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	●		50 ±0.3	50 ±0.8 50 ±0.9	% %
	V_S = ±5V, f_{CLK} = 500kHz, Mode 1, f_O = 10kHz, Q = 5, V_{IN} = 1V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	●		50 ±0.3	50 ±0.8 50 ±0.9	% %
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 5)	V_S = 3.14V, f_{CLK} = 250kHz, Q = 5 (Note 2) V_S = ±5V, f_{CLK} = 500kHz, Q = 5	● ●		±0.25 ±0.25	±0.9 ±0.9	% %
Q Accuracy (Note 5)	V_S = 3.14V, f_{CLK} = 250kHz, Q = 5 (Note 2) V_S = ±5V, f_{CLK} = 500kHz, Q = 5	● ●		±1 ±1	±3 ±3	% %
f_O Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (Note 5) (See Table 1)	V_S = ±5V, f_{CLK} = 500kHz, V_{OS1} (DC Offset of Input Inverter)	●		0	±15	mV
	V_S = ±5V, f_{CLK} = 500kHz, V_{OS2} (DC Offset of First Integrator)	●		–2	±25	mV
	V_S = ±5V, f_{CLK} = 500kHz, V_{OS3} (DC Offset of Second Integrator)	●		–5	±40	mV
Clock Feedthrough	V_S = ±5V, f_{CLK} = 500kHz			0.16		mV_{RMS}
Max Clock Frequency (Note 6)	V_S = ±5V, Q ≤ 1.6, Mode 1			3.4		MHz
Power Supply Current	V_S = 3.14V, f_{CLK} = 250kHz (Note 2) V_S = 4.75V, f_{CLK} = 250kHz (Note 3) V_S = ±5V, f_{CLK} = 500kHz	● ● ●		3.0 4.3 6.0	5 8 11	mA mA mA

ELECTRICAL CHARACTERISTICS

LTC1068-25 (Internal Op Amps). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			3.14		±5.5	V
Voltage Swings	V_S = 3.14V, R_L = 5k (Note 2) V_S = 4.75V, R_L = 5k (Note 3) V_S = ±5V, R_L = 5k	● ● ●	1.2 2.6 ±3.4	1.6 3.4 ±4.1		V_{P-P} V_{P-P} V
Output Short-Circuit Current (Source/Sink)	V_S = ±4.75V V_S = ±5V			17/6 20/15		mA mA
DC Open-Loop Gain	R_L = 5k			85		dB
GBW Product	V_S = ±5V			6		MHz
Slew Rate	V_S = ±5V			10		V/µs
Analog Ground Voltage (Note 4)	V_S = 5V, Voltage at AGND			2.5V ±2%		V

LTC1068-25 (Complete Filter) V_S = ±5V, T_A = 25°V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Center Frequency Ratio (Note 5)	V_S = 4.75V, f_{CLK} = 500kHz, Mode 1 (Note 3), f_O = 20kHz, Q = 5, V_{IN} = 0.5V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	●		25 ±0.3	25 ±0.8 25 ±0.9	% %
	V_S = ±5V, f_{CLK} = 1MHz, Mode 1, f_O = 40kHz, Q = 5, V_{IN} = 1V_{RMS}, R1 = R3 = 49.9k, R2 = 10k	●		25 ±0.3	25 ±0.8 25 ±0.9	% %
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 5)	V_S = 4.75V, f_{CLK} = 500kHz, Q = 5 (Note 3) V_S = ±5V, f_{CLK} = 1MHz, Q = 5	● ●		±0.25 ±0.25	±0.9 ±0.9	% %
Q Accuracy (Note 5)	V_S = 4.75V, f_{CLK} = 500kHz, Q = 5 (Note 3) V_S = ±5V, f_{CLK} = 1MHz, Q = 5	● ●		±1 ±1	±3 ±3	% %
f_O Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (Note 5) (See Table 1)	V_S = ±5V, f_{CLK} = 1MHz, V_{OS1} (DC Offset of Input Inverter)	●		0	±15	mV
	V_S = ±5V, f_{CLK} = 1MHz, V_{OS2} (DC Offset of First Integrator)	●		–2	±25	mV
	V_S = ±5V, f_{CLK} = 1MHz, V_{OS3} (DC Offset of Second Integrator)	●		–5	±40	mV
Clock Feedthrough	V_S = ±5V, f_{CLK} = 1MHz			0.25		mV_{RMS}
Max Clock Frequency (Note 6)	V_S = ±5V, Q ≤ 1.6, Mode 1			5.6		MHz
Power Supply Current	V_S = 3.14V, f_{CLK} = 1MHz (Note 2) V_S = 4.75V, f_{CLK} = 1MHz (Note 3) V_S = ±5V, f_{CLK} = 1MHz	● ● ●		3.5 6.5 9.5	8 11 15	mA mA mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Production testing for single 3.14V supply is achieved by using the equivalent dual supplies of ±1.57V.

Note 3: Production testing for single 4.75V supply is achieved by using the equivalent dual supplies of ±2.375V.

Note 4: Pin 7 (AGND) is the internal analog ground of the device. For single supply applications this pin should be bypassed with a 1µF capacitor. The biasing voltage of AGND is set with an internal resistive divider from Pin 8 to Pin 23 (see Block Diagram).

Note 5: Side D is guaranteed by design.

Note 6: See Typical Performance Characteristics.

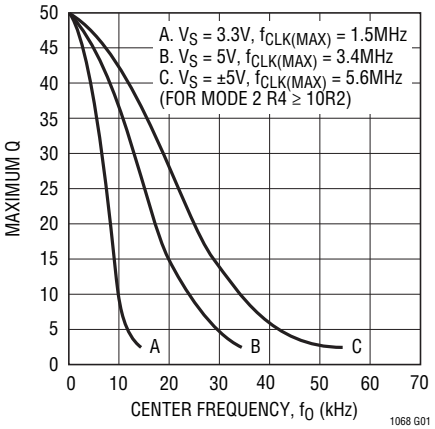
ELECTRICAL CHARACTERISTICS

Table 1. Output DC Offsets One 2nd Order Section

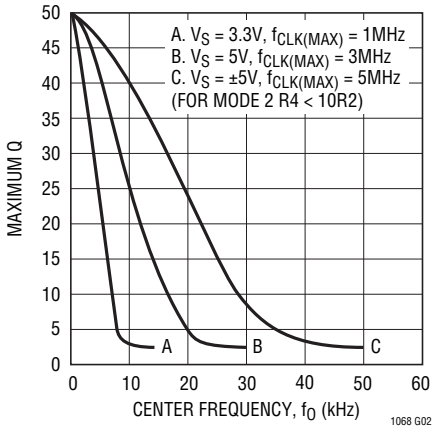
MODE	V_{OSN}	V_{OSBP}	V_{OSLP}
1	$V_{OS1}[(1/Q) + 1 + \|\|HOLP\|\|] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)X [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1}[1 + R4/R1 + R4/R2 + R4/R3] - V_{OS2}(R4/R2) - V_{OS3}(R4/R3)$

TYPICAL PERFORMANCE CHARACTERISTICS

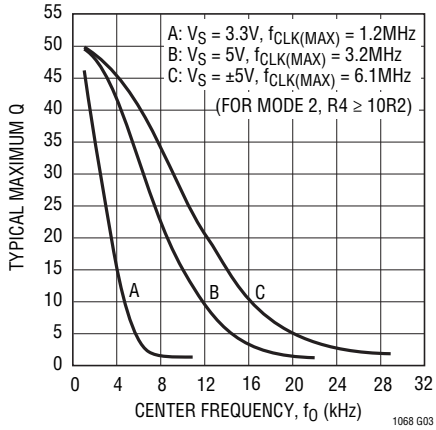
LTC1068
Maximum Q vs Center Frequency
(Modes 1, 1b, 2)



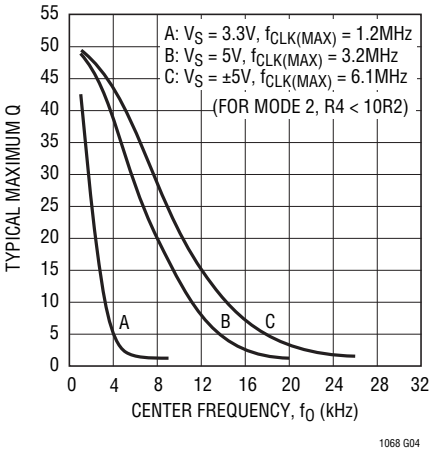
LTC1068
Maximum Q vs Center Frequency
(Modes 2, 3)



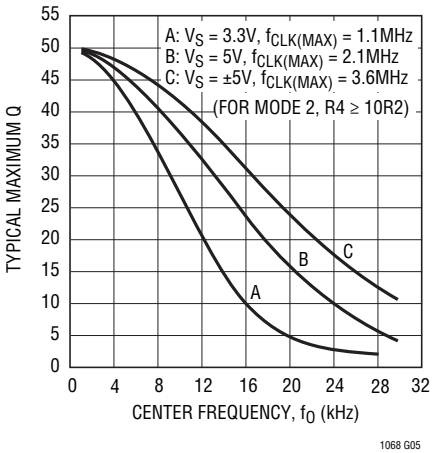
LTC1068-200
Maximum Q vs Center Frequency
(Modes 1, 1b, 2)



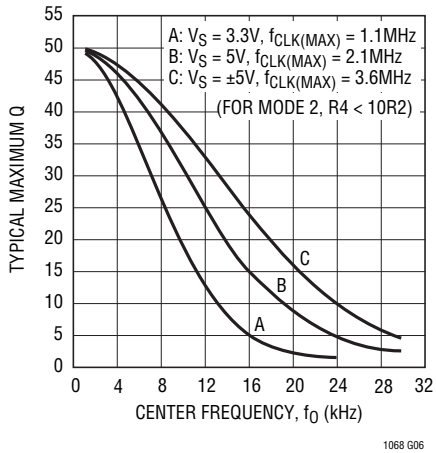
LTC1068-200
Maximum Q vs Center Frequency
(Modes 2, 3)



LTC1068-50
Maximum Q vs Center Frequency
(Modes 1, 1b, 2)

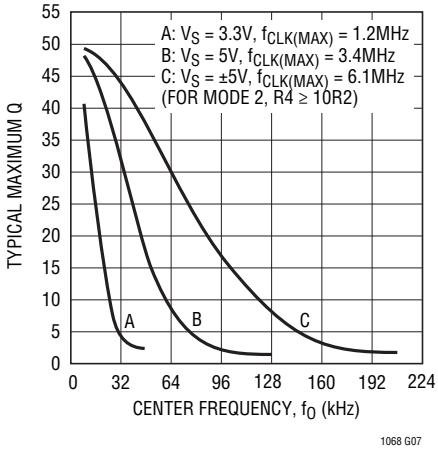


LTC1068-50
Maximum Q vs Center Frequency
(Modes 2, 3)

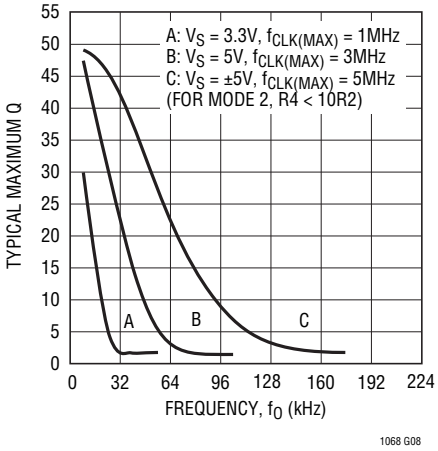


TYPICAL PERFORMANCE CHARACTERISTICS

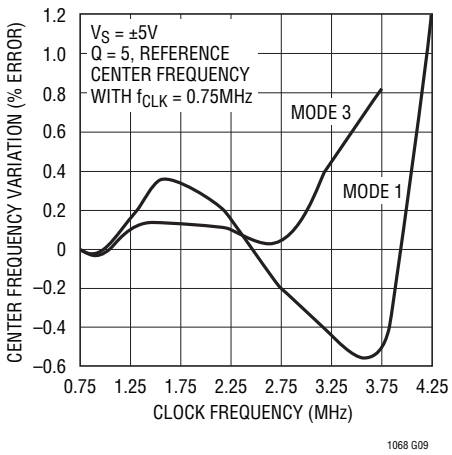
LTC1068-25
Maximum Q vs Center Frequency
(Modes 1, 1b, 2)



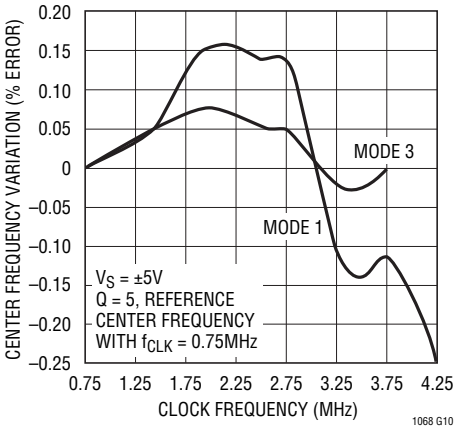
LTC1068-25
Maximum Q vs Center Frequency
(Modes 2, 3)



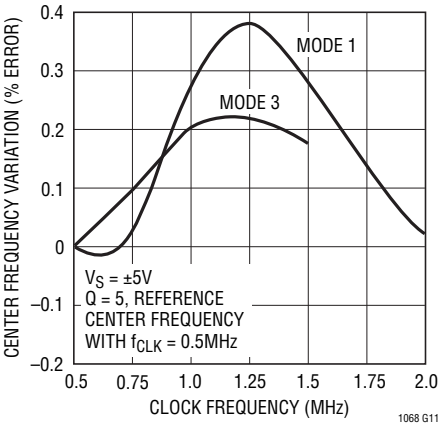
LTC1068 Center Frequency
Variation vs Clock Frequency



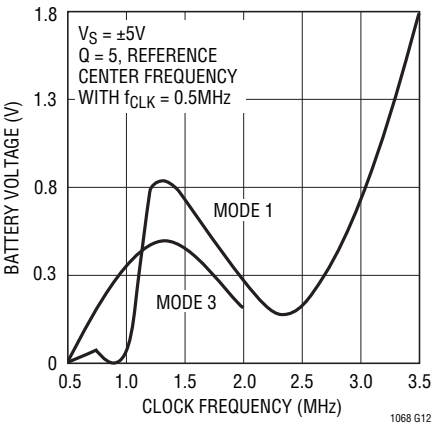
LTC1068-200 Center Frequency
Variation vs Clock Frequency



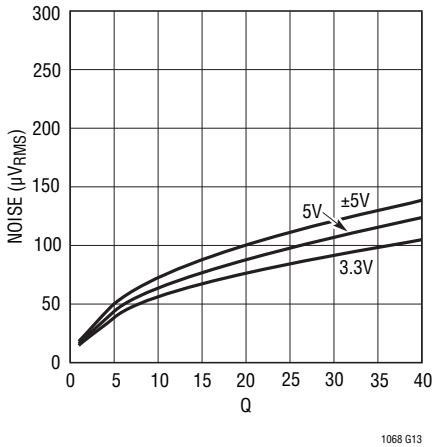
LTC1068-50 Center Frequency
Variation vs Clock Frequency



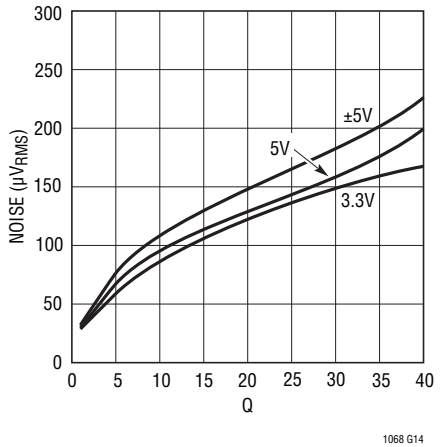
LTC1068-25 Center Frequency
Variation vs Clock Frequency



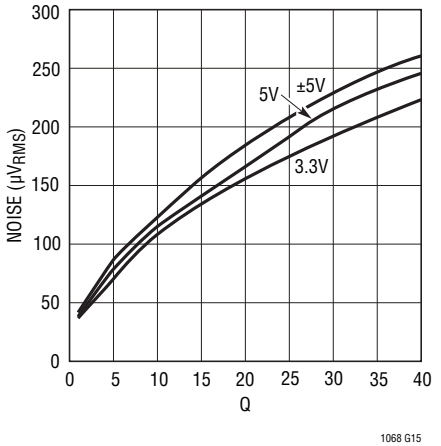
LTC1068/LTC1068-200
Noise vs Q



LTC1068-50 Noise vs Q

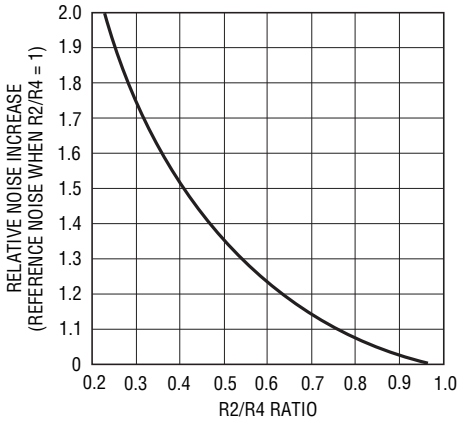


LTC1068-25 Noise vs Q

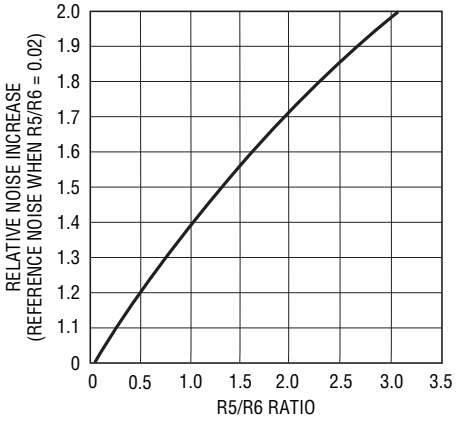


TYPICAL PERFORMANCE CHARACTERISTICS

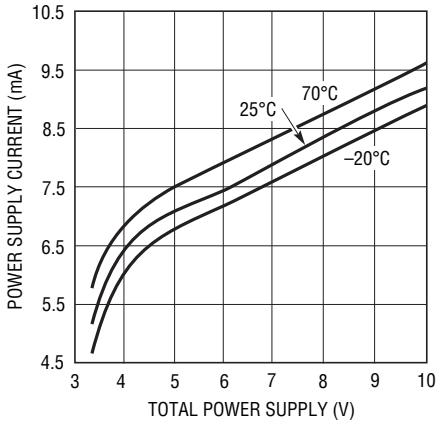
Noise Increase vs R2/R4 Ratio (Mode 3)



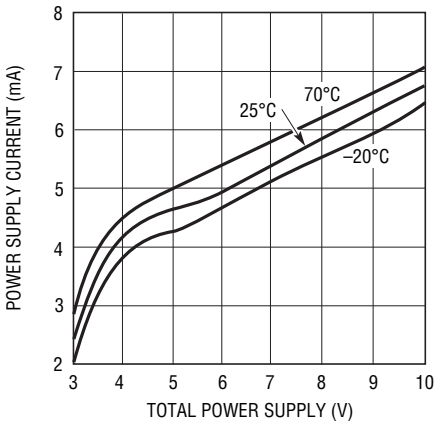
Noise Increase vs R5/R6 Ratio (Mode 1b)



LTC1068/LTC1068-200/ LTC1068-25 Power Supply Current vs Power Supply



LTC1068-50 Power Supply Current vs Power Supply



PIN FUNCTIONS

Power Supply Pins

The V^+ and V^- pins should each be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. Figures 1 and 2 show typical connections for dual and single supply operation.

Analog Ground Pin

The filter's performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For single supply operation, AGND should be bypassed to the analog ground plane with at least a 0.47µF capacitor (Figure 2).

Two internal resistors bias the analog ground pin. For the LTC1068, LTC1068-200 and LTC1068-25, the voltage at the analog ground pin (AGND) for single supply is $0.5 \times V^+$ and for the LTC1068-50 it is $0.435 \times V^+$.

Clock Input Pin

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 2 shows the clock's low and high level threshold values for dual or single supply operation.

Table 2. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±5V	≥ 1.53V	≤ 0.53V
Single Supply = 5V	≥ 1.53V	≤ 0.53V
Single Supply = 3.3V	≥ 1.20V	≤ 0.53V

A pulsed generator can be used as a clock source provided the high level ON time is at least 25% of the pulse period. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal

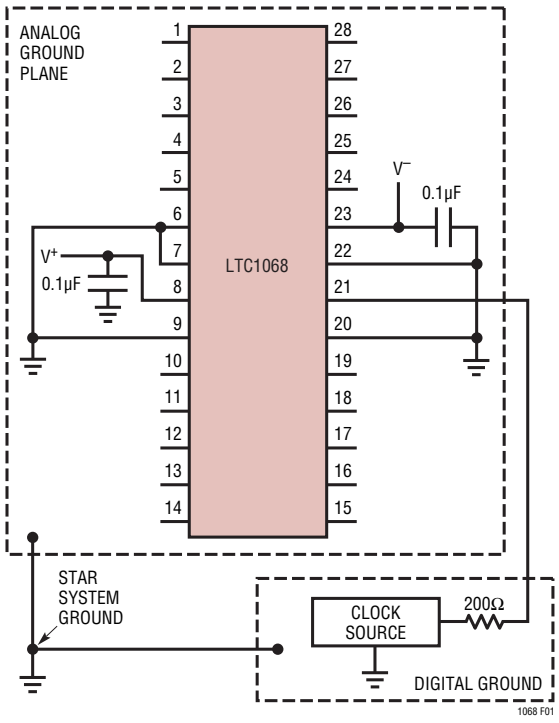


Figure 1. Dual Supply Ground Plane Connections

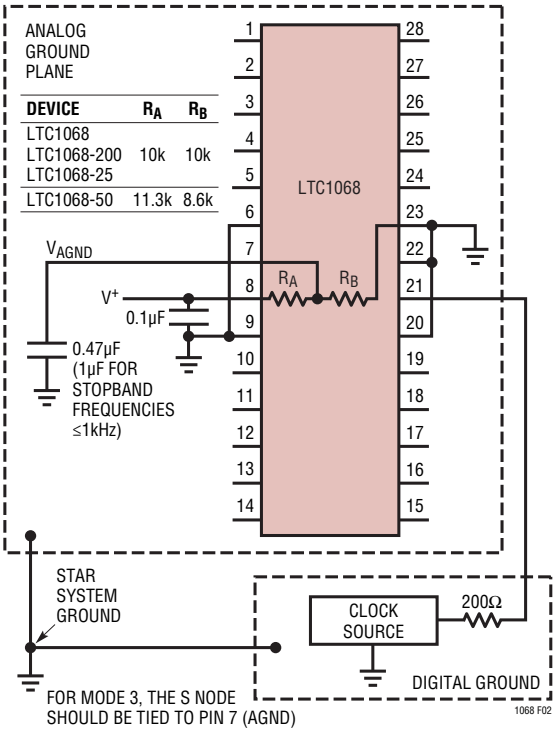


Figure 2. Single Supply Ground Plane Connections

PIN FUNCTIONS

path. A 200Ω resistor between clock source and Pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 1 and 2).

Output Pins

Each 2nd order section of an LTC1068 device has three outputs that typically source 17mA and sink 6mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion performance of any filter design. When evaluating the distortion or noise performance of a particular filter design implemented with a LTC1068 device, the final output of the filter should be buffered with a wideband, noninverting high slew rate amplifier (Figure 3).

Inverting Input Pins

These pins are the inverting inputs of internal op amps and are susceptible to stray capacitive coupling from low impedance signal outputs and power supply lines.

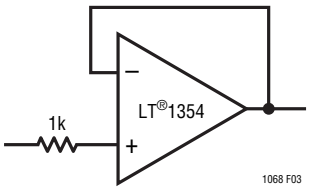


Figure 3. Wideband Buffer

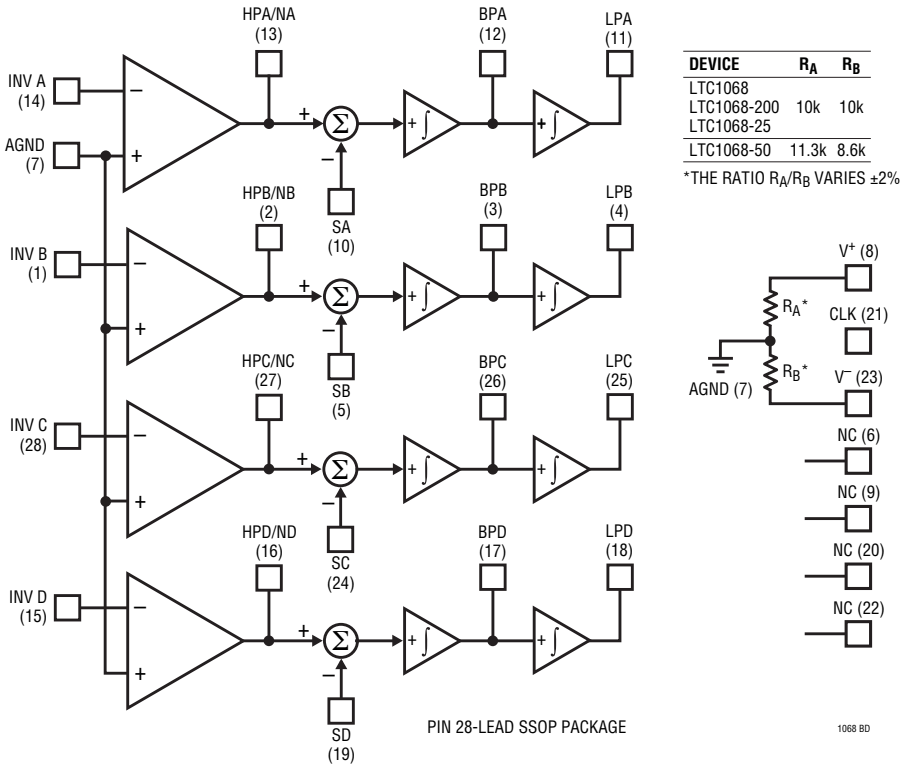
In a printed circuit layout any signal trace, clock source trace or power supply trace should be at least 0.1 inches away from any inverting input pins

Summing Input Pins

These are voltage input pins. If used, they should be driven with a source impedance below 5k. When they are not used, they should be tied to the analog ground pin.

The summing pin connections determine the circuit topology (mode) of each 2nd order section. Please refer to Modes of Operation.

BLOCK DIAGRAM



DEVICE	R_A	R_B
LTC1068 LTC1068-200 LTC1068-25	10k	10k
LTC1068-50	11.3k	8.6k

*THE RATIO R_A/R_B VARIES ±2%

MODES OF OPERATION

Linear Technology's universal switched-capacitor filters are designed for a fixed internal, nominal f_{CLK}/f_O ratio. The f_{CLK}/f_O ratio is 100 for the LTC1068, 200 for the LTC1068-200, 50 for the LTC1068-50 and 25 for the LTC1068-25. Filter designs often require the f_{CLK}/f_O ratio of each section to be different from the nominal ratio and in most cases different from each other. Ratios other than the nominal value are possible with external resistors. Operating modes use external resistors, connected in different arrangements to realize different f_{CLK}/f_O ratios. By choosing the proper mode, the f_{CLK}/f_O ratio can be increased or decreased from the part's nominal ratio.

The choice of operating mode also effects the transfer function at the HP/N pins. The LP and BP pins always give the lowpass and bandpass transfer functions respectively, regardless of the mode utilized. The HP/N pins have a different transfer function depending on the mode used. Mode 1 yields a notch transfer function. Mode 3 yields a highpass transfer function. Mode 2 yields a highpass notch transfer function (i.e., a highpass with a stopband notch). More complex transfer functions, such as lowpass notch, allpass or complex zeros, are achieved by summing two or more of the LP, BP or HP/N outputs. This is illustrated in sections Mode 2n and Mode 3a.

Choosing the proper mode(s) for a particular application is not trivial and involves much more than just adjusting the f_{CLK}/f_O ratio. Listed here are four of the nearly twenty modes available. To make the design process simpler and quicker, Linear Technology has developed the FilterCAD for Widows design software. FilterCAD is an easy-to-use, powerful and interactive filter design program. The designer can enter a few filter specifications and the program produces a full schematic. FilterCAD allows the designer to concentrate on the filter's transfer function and not get bogged down in the details of the design. Alternatively, those who have experience with the Linear Technology family of parts can control all of the details themselves. For a complete listing of all the operating modes, consult the appendices of the FilterCAD manual or the Help files in FilterCAD. FilterCAD can be obtained free of charge on the Linear Technology web site (www.linear.com) or you can order the FilterCAD CD-ROM by contacting Linear Technology Marketing.

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at the part's nominal ratio. Figure 4 illustrates Mode 1 providing 2nd order notch, lowpass and bandpass outputs. Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency. Mode 1 is faster than Mode 3.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

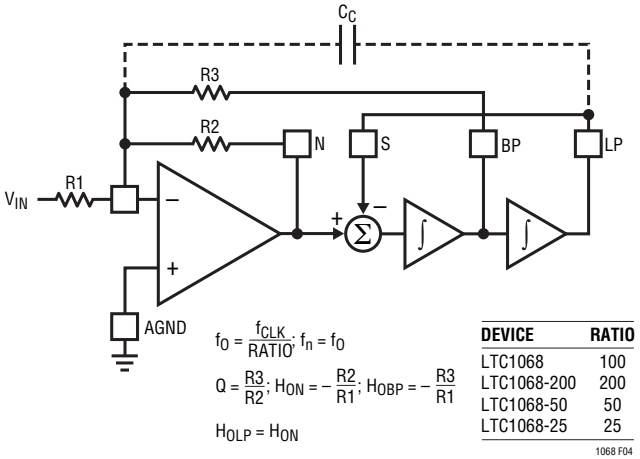


Figure 4. Mode 1, 2nd Order Filter Providing Notch, Bandpassing and Lowpass Outputs

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b (Figure 5) two additional resistors R5 and R6 are added to lower the amount of voltage fed back from the lowpass output into the input of the SA (or SB) switched-capacitor summer. This allows the filter's clock-to-center frequency ratio to be adjusted beyond the part's nominal ratio. Mode 1b maintains the speed advantages of Mode 1 and should be considered an optimum mode for high Q designs with f_{CLK} to f_{CUTOFF} (or f_{CENTER}) ratios greater than the part's nominal ratio.

The parallel combination of R5 and R6 should be kept below 5k.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

MODES OF OPERATION

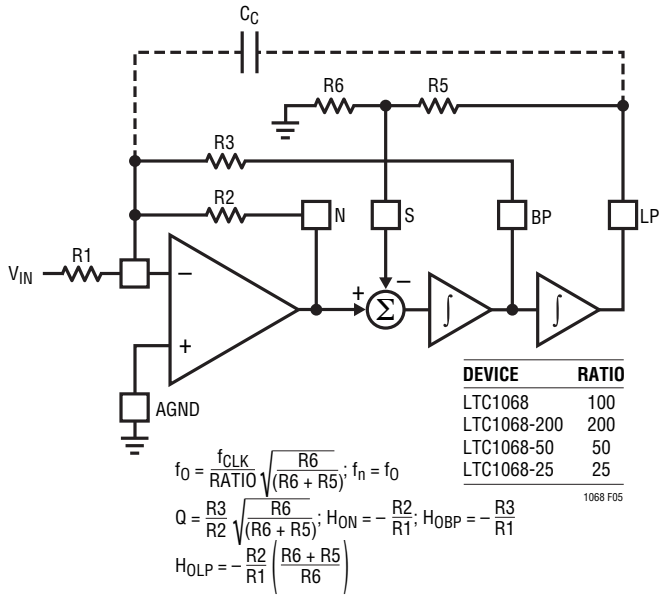


Figure 5. Mode 1b, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

Mode 3

In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below the parts nominal ratio. Figure 6 illustrates Mode 3, the classical state variable configuration, providing highpass, bandpass and lowpass 2nd order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass and highpass filters.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, shown in Figure 7. With Mode 2, the clock-to-center frequency ratio, f_{CLK}/f_O, is always less than the part's nominal ratio. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. Mode 2 has a highpass notch output where the notch frequency depends solely on the clock frequency and is therefore less than the center frequency, f_O.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

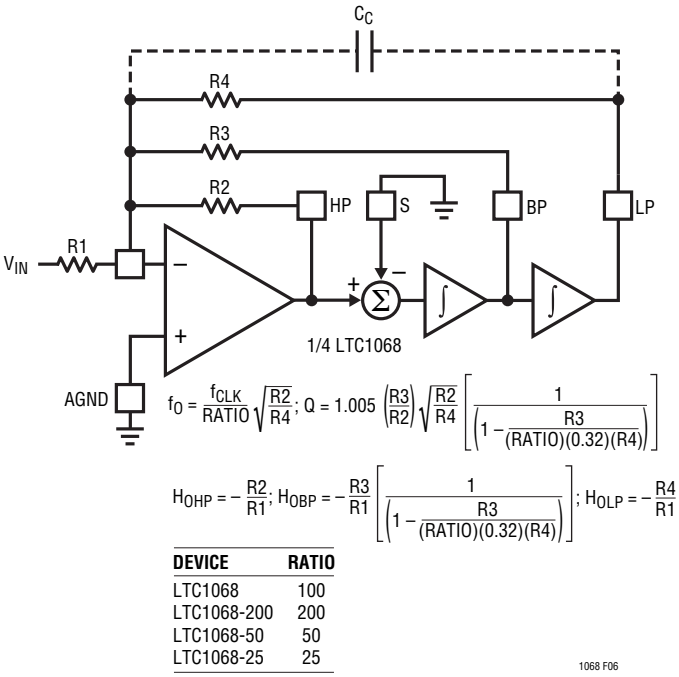


Figure 6. Mode 3, 2nd Order Section Providing Highpass, Bandpass and Lowpass Outputs

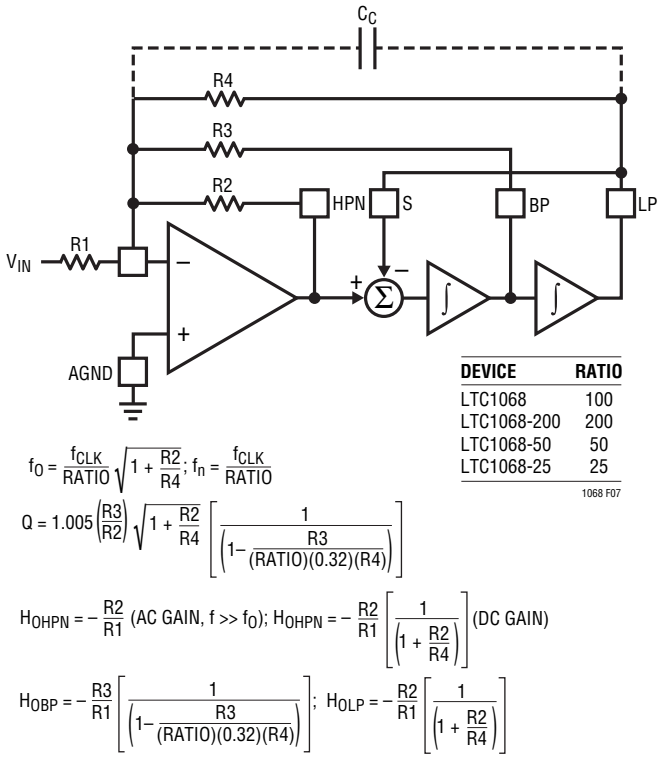


Figure 7. Mode 2, 2nd Order Filter Providing Highpass Notch, Bandpass and Lowpass Outputs

APPLICATIONS INFORMATION

Operating Limits

The Maximum Q vs Center Frequency (f_O) graphs, under Typical Performance Characteristics, define an upper limit of operating Q for each LTC1068 device 2nd order section. These graphs indicate the power supply, f_O and Q value conditions under which a filter implemented with an LTC1068 device will remain stable when operated at temperatures of 70°C or less. For a 2nd order section, a bandpass gain error of 3dB or less is arbitrarily defined as a condition for stability.

When the passband gain error begins to exceed 1dB, the use of capacitor C_C will reduce the gain error (capacitor C_C is connected from the lowpass node to the inverting node of a 2nd order section). Please refer to Figures 4 through 7. The value of C_C can be best determined experimentally, and as a guide it should be about 5pF for each 1dB of gain error and not to exceed 15pF. When operating an LTC1068 device near the limits defined by the Maximum Q vs Frequency graphs, passband gain variations of 2dB or more should be expected.

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pins. The clock feedthrough is tested with the filter's input grounded and depends on PC board layout and on the value of the power supplies. With proper layout techniques, the typical values of clock feedthrough are listed under Electrical Characteristics.

Any parasitic switching transients during the rising and falling edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, can be greatly reduced by adding a simple RC lowpass network at the final filter output. This RC will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and cannot be reduced with post filtering. For a notch filter the noise of the filter is centered at the notch frequency.

The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

For a specific filter design, the total noise depends on the Q of each section and the cascade sequence. Please refer to the Noise vs Q graphs under the Typical Performance Characteristics.

Aliasing

Aliasing is an inherent phenomenon of switched-capacitor filters and occurs when the frequency of the input signals that produce the strongest aliased components have a frequency, f_{IN}, such as ($f_{SAMPLING} - f_{IN}$) that falls into the filter's passband. For an LTC1068 device the sampling frequency is twice f_{CLK}. If the input signal spectrum is not band-limited, aliasing may occur.

Demonstration Circuit 104

DC104 is a surface mount printed circuit board for the evaluation of Linear Technology's LTC1068 product family in a 28-lead SSOP package. The LTC1068 product family consists of four monolithic clock-tunable filter building blocks.

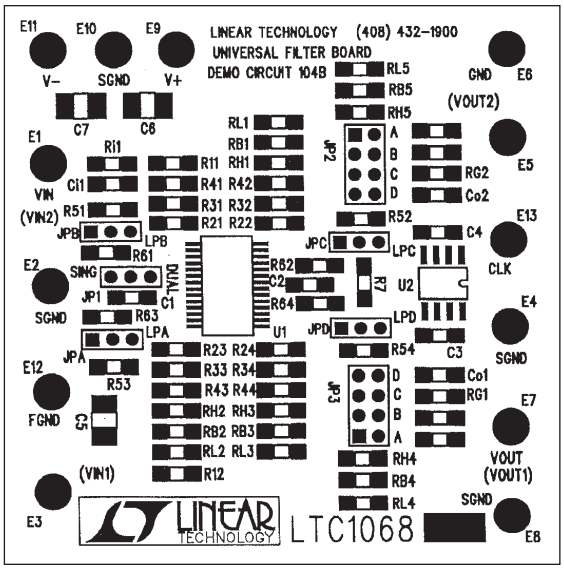
Demo Board 104 is available in four assembled versions: Assembly 104-A features the low noise LTC1068CG (clock-to-center frequency ratio = 100), assembly 104-B features the low noise LTC1068-200CG (clock-to-center frequency ratio = 200), assembly 104-C features the high frequency LTC1068-25CG (clock-to-center frequency ratio = 25) and assembly 104-D features the low power LTC1068-50CG (clock-to-center frequency ratio = 50).

All DC104 boards are assembled with input, output and power supply test terminals, a 28-lead SSOP filter device (LTC1068CG Series), a dual op amp in an SO-8 for input or output buffers and decoupling capacitors for the filter and op amps. The filter and dual op amps share the power

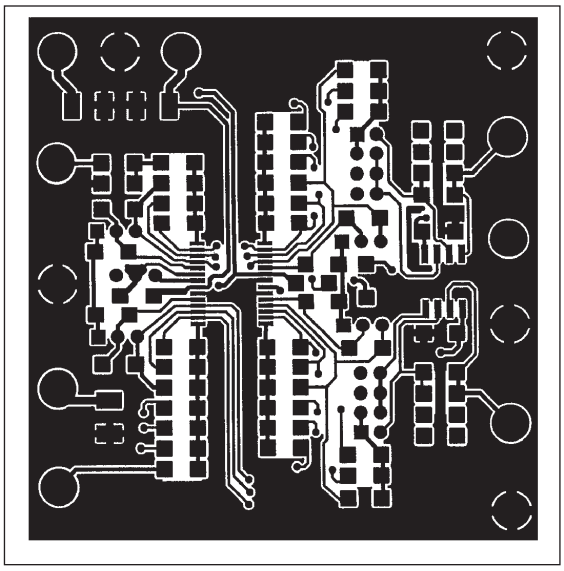
APPLICATIONS INFORMATION

supply inputs to the board. Jumpers JPA to JPD on the board configure the filter's second order circuit modes, jumper JP1 configures the filter for dual or single supply operation and jumpers JP2 (A-D) to JP3 (A-D) configure the op amp buffers as inverting or noninverting. Surface mount pads are available on the board for 1206 size surface mount resistors. The printed circuit layout of DC104 is arranged so that most of the resistor connections for one 8th order filter or two 4th order filters are available on the board. A resistor makes a connection between two filter nodes on the board and for most filter designs, no wiring is required.

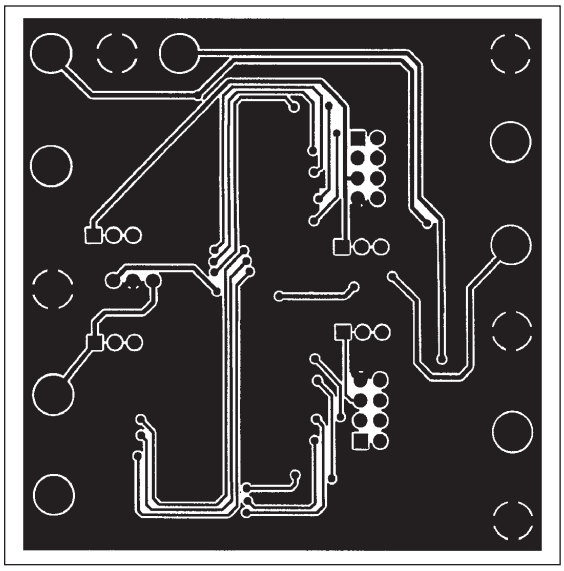
DC104 Component Side Silkscreen



DC104 Component Side

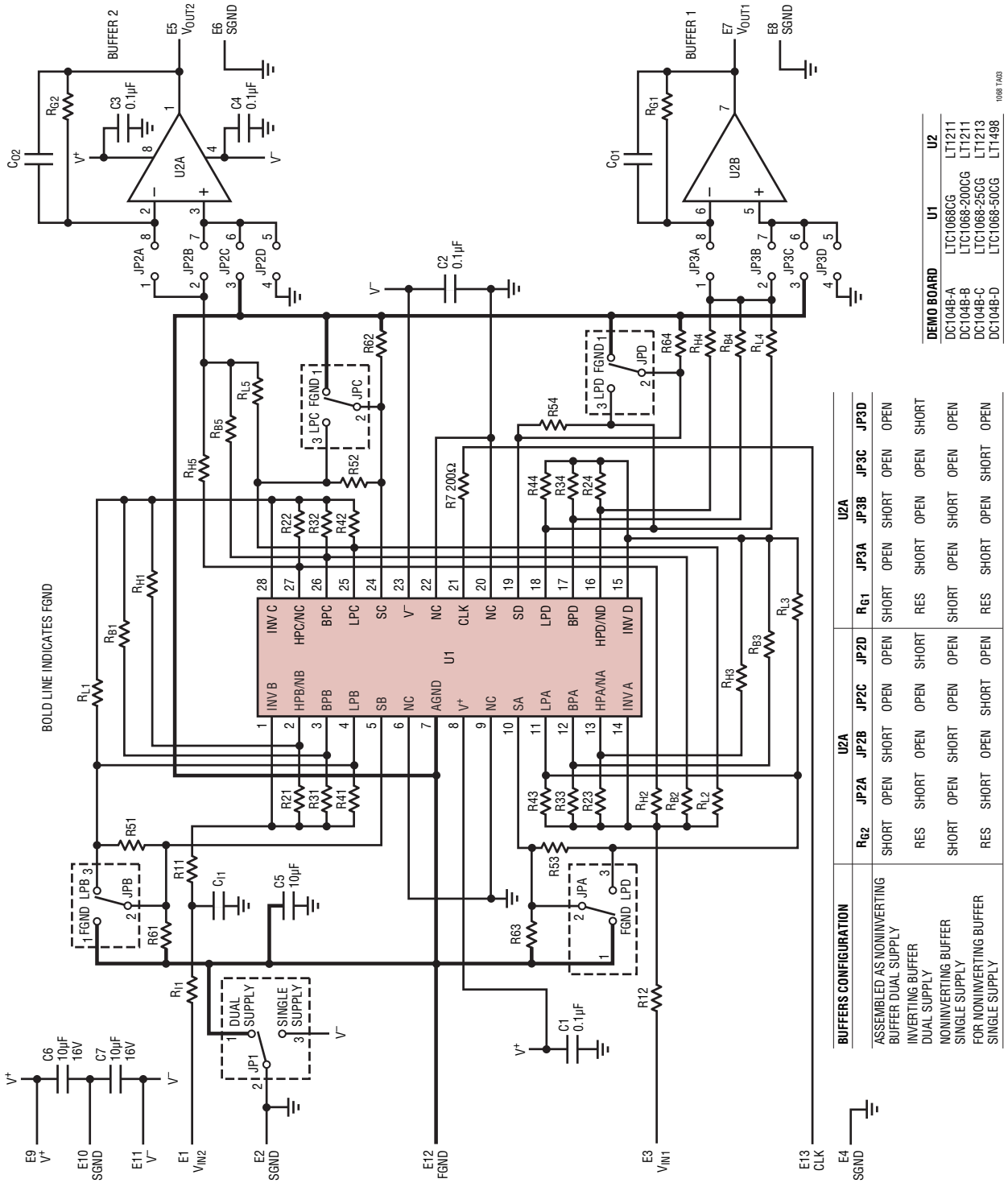


DC104 Solder Side



APPLICATIONS INFORMATION

DC104 Schematic



BUFFERS CONFIGURATION	U2A					U2A				
	R_{G2}	JP2A	JP2B	JP2C	JP2D	R_{G1}	JP3A	JP3B	JP3C	JP3D
ASSEMBLED AS NONINVERTING BUFFER DUAL SUPPLY	SHORT	OPEN	SHORT	OPEN	OPEN	SHORT	OPEN	SHORT	OPEN	OPEN
INVERTING BUFFER DUAL SUPPLY	RES	SHORT	OPEN	OPEN	SHORT	RES	SHORT	OPEN	OPEN	SHORT
NONINVERTING BUFFER SINGLE SUPPLY	SHORT	OPEN	SHORT	OPEN	OPEN	SHORT	OPEN	SHORT	OPEN	OPEN
FOR NONINVERTING BUFFER SINGLE SUPPLY	RES	SHORT	OPEN	SHORT	OPEN	RES	SHORT	OPEN	SHORT	OPEN

DEMO BOARD	U1	U2
DC104B-A	LTC1068CG	LT1211
DC104B-B	LTC1068-200CG	LT1211
DC104B-C	LTC1068-25CG	LT1213
DC104B-D	LTC1068-50CG	LT1498

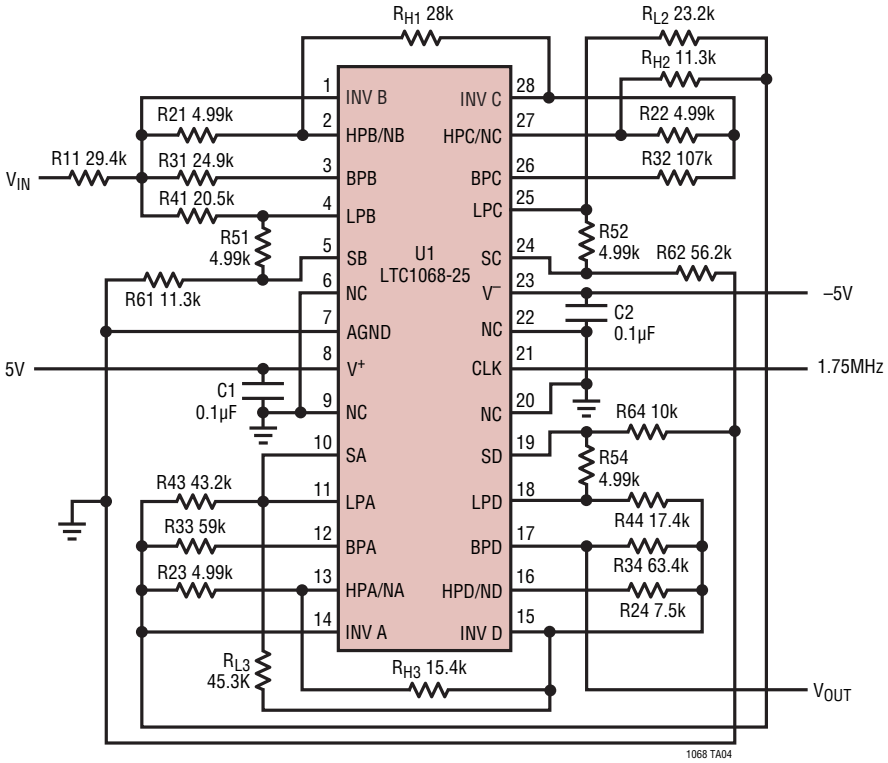
1068 TA03

APPLICATIONS INFORMATION

A Surface Mount Printed Circuit Layout

A very compact surface mount printed circuit layout can be designed with 0603 size surface mount resistors, capacitors and a 28-pin SSOP of the LTC1068 product family. An example of a printed circuit layout is shown in the following figures for an 8th order elliptic bandpass filter. The total board area of this 8th order filter is 1" by 0.8". No attempt was made to design the smallest possible printed circuit layout.

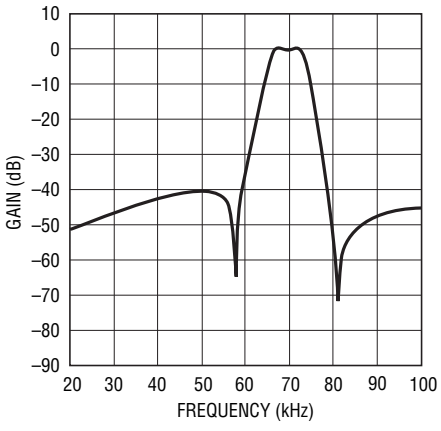
70kHz Elliptic Bandpass Filter, $f_{CENTER} = f_{CLK}/25$ (Maximum f_{CENTER} is 80kHz, $V_S = \pm 5V$)



FilterCAD Custom Inputs for f_C = 70kHz

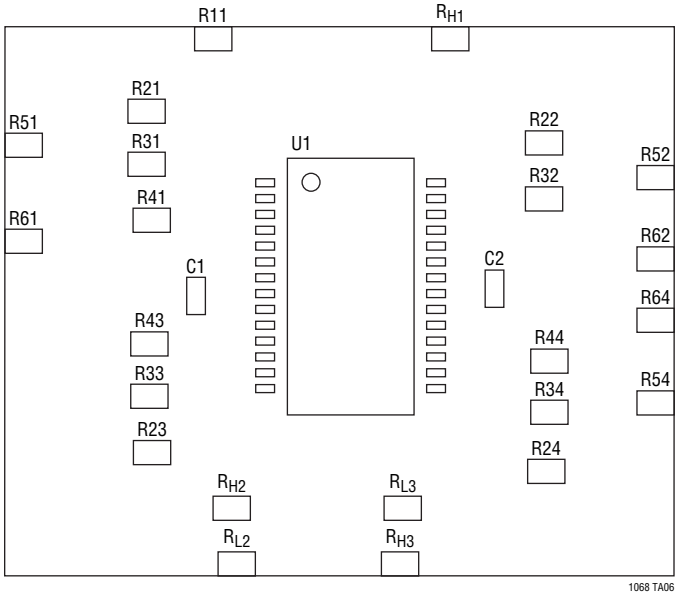
2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	TYPE	MODE
B	67.7624	5.7236	58.3011	HPN	2b
C	67.0851	20.5500	81.6810	LPN	1bn
A	73.9324	15.1339	81.0295	LPN	2n
D	73.3547	16.3491		BP	2b

Gain vs Frequency

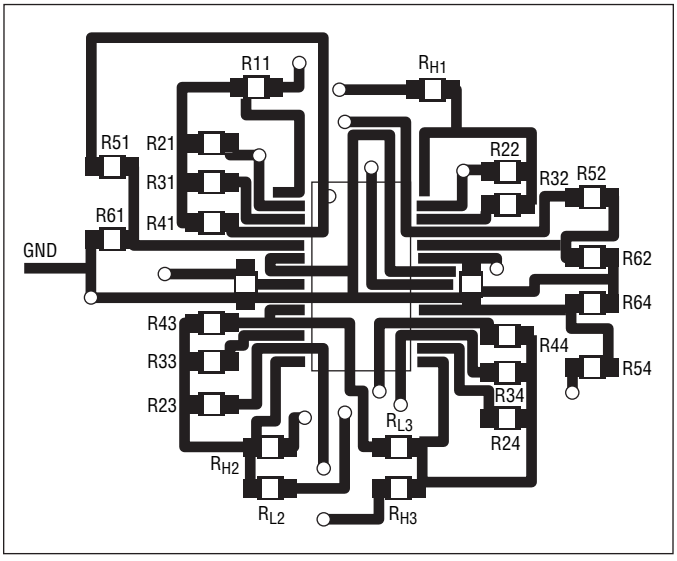


APPLICATIONS INFORMATION

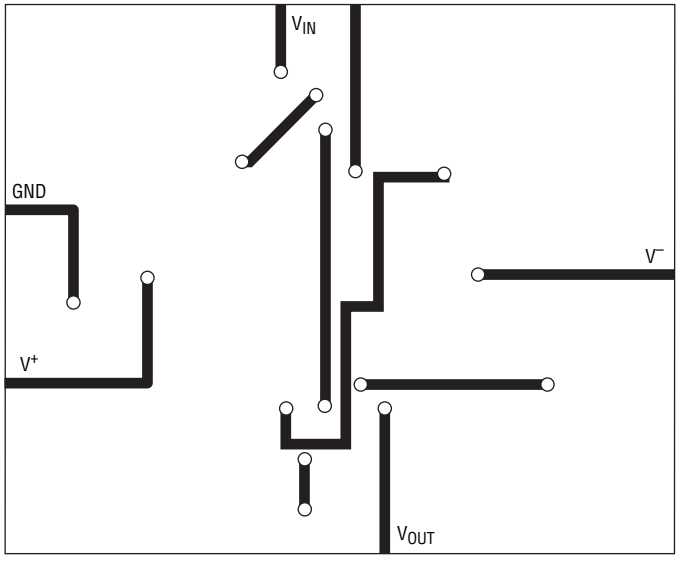
Surface Mount Components
(Board Area = 1" × 0.8")



Component Side

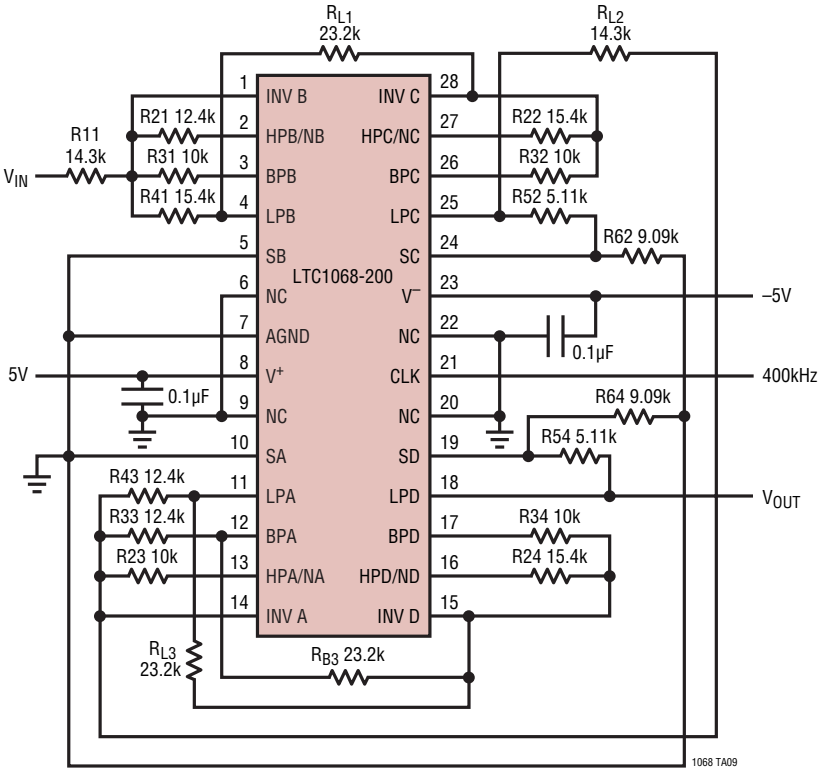


Solder Side

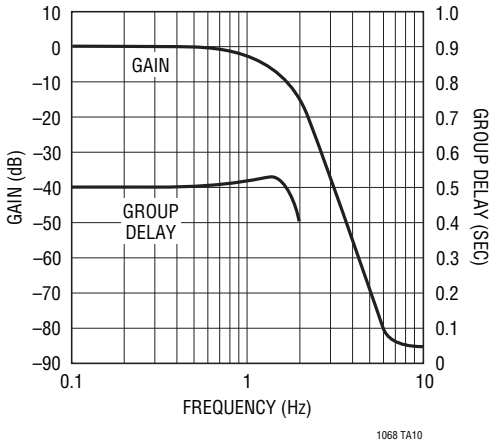


TYPICAL APPLICATIONS

LTC1068-200 8th Order Linear Phase Lowpass, $f_{CUTOFF} = f_{CLK}/400$ for Ultralow Frequency Applications



Gain and Group Delay vs Frequency

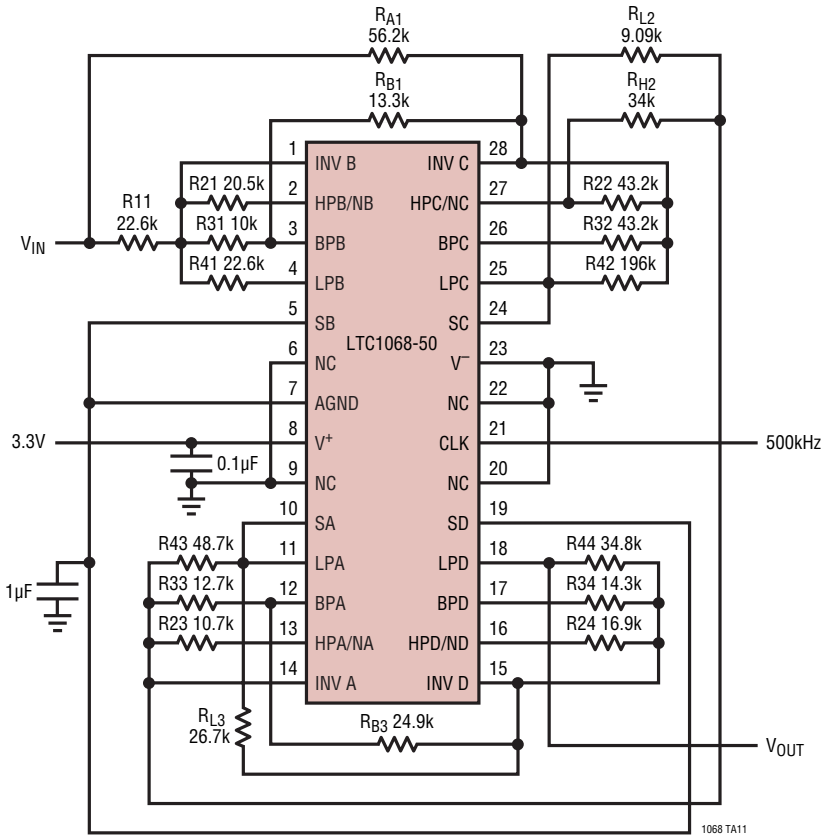


FilterCAD Custom Inputs for f_C = 1Hz

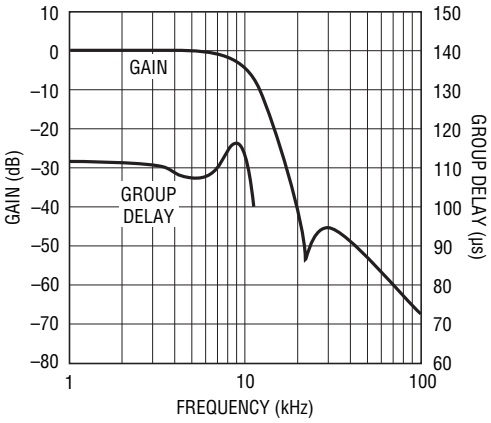
2nd ORDER SECTION	f_0 (kHz)	Q	Q_N	TYPE	MODE
B	1.7947	0.7347		LP	3
C	1.6002	0.5195		LP	1b
A	1.7961	1.1369	1.0159	LPBP	3s
D	1.6070	0.5217		LP	1b

TYPICAL APPLICATIONS

LTC1068-50 8th Order Linear Phase Lowpass, $f_{CUTOFF} = f_{CLK}/50$ for Single Supply Low Power Applications. Maximum f_{CUTOFF} is 20kHz with a 3.3V Supply and 40kHz with a 5V Supply



Gain and Group Delay vs Frequency

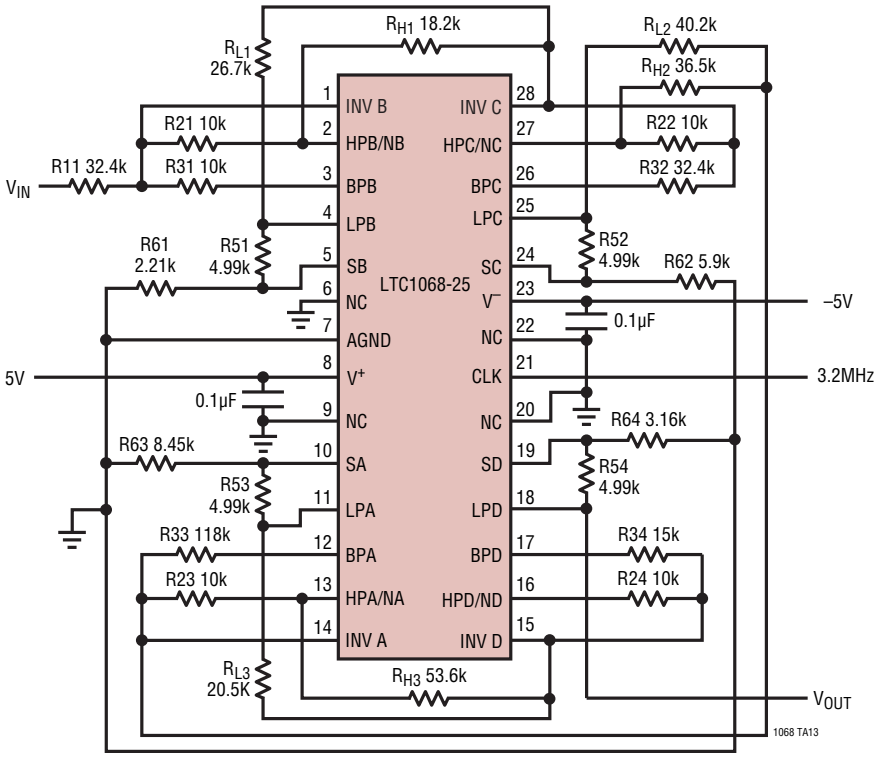


FilterCAD Custom Inputs for f_C = 10kHz

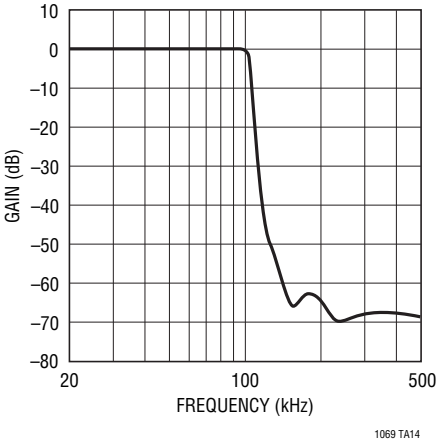
2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	Q_N	TYPE	MODE
B	9.5241	0.5248		0.5248	AP	4a3
C	11.0472	1.1258	21.7724		LPN	2n
A	11.0441	1.3392		1.5781	LPBP	2s
D	6.9687	0.6082			LP	3

TYPICAL APPLICATIONS

LTC1068-25 8th Order Lowpass, $f_{CUTOFF} = f_{CLK}/32$, Attenuation –50dB at (1.25) (f_{CUTOFF}) and –60dB at (1.5)(f_{CUTOFF}). Maximum f_{CUTOFF} = 120kHz



Gain vs Frequency

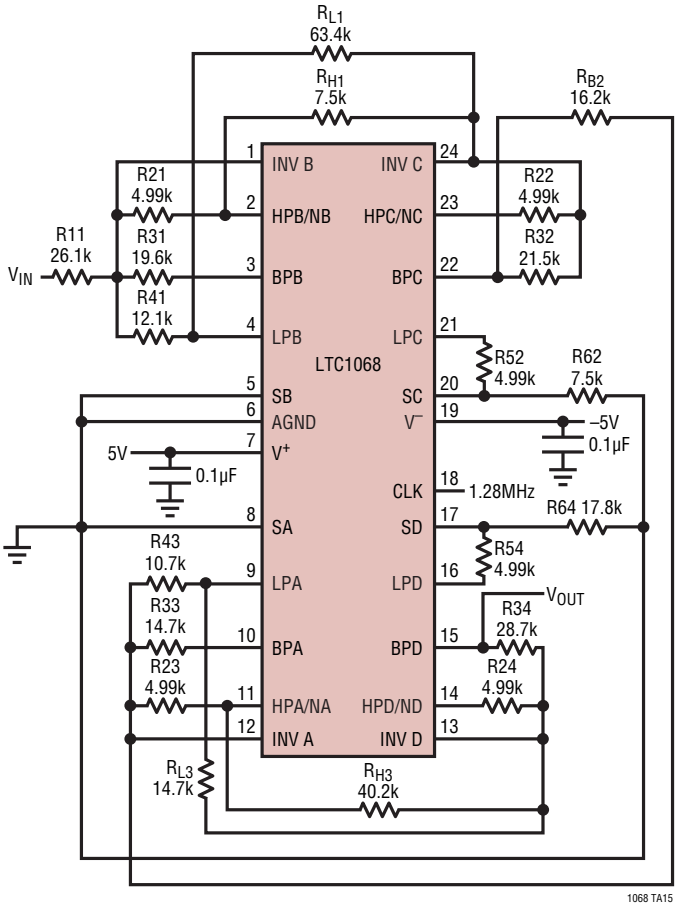


FilterCAD Custom Inputs for f_C = 100kHz

2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	TYPE	MODE
B	70.9153	0.5540	127.2678	LPN	1bn
C	94.2154	2.3848	154.1187	LPN	1bn
A	101.4936	9.3564	230.5192	LPN	1bn
D	79.7030	0.9340		LP	1b

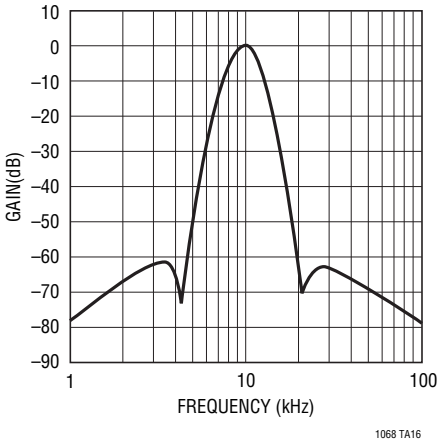
TYPICAL APPLICATIONS

LTC1068 8th Order Linear Phase Bandpass, $f_{CENTER} = f_{CLK}/128$, Passband –3dB at (0.88)(f_{CENTER}) and (1.12)(f_{CENTER}). Maximum f_{CENTER} = 40kHz with ±5V Supplies



24-Lead Package

Gain vs Frequency

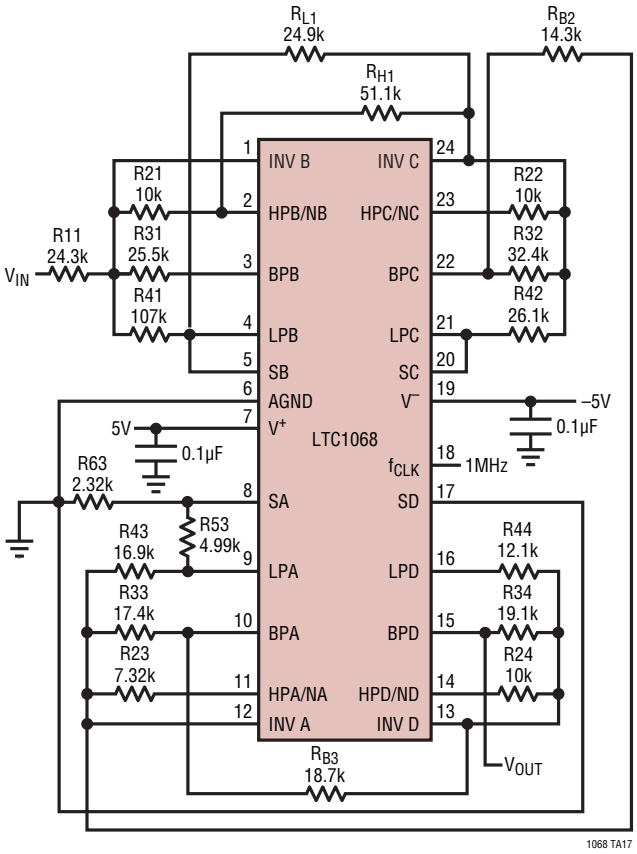


FilterCAD Custom Inputs for f_C = 10kHz

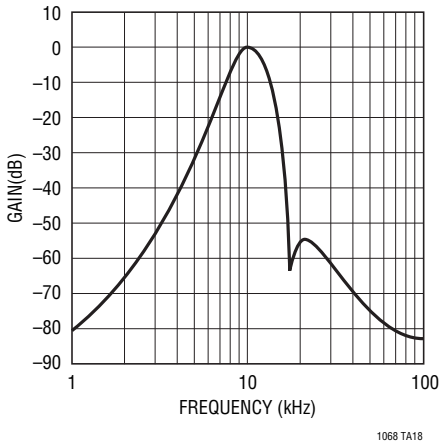
2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	TYPE	MODE
B	8.2199	2.6702	4.4025	HPN	3a
C	9.9188	3.3388		BP	1b
A	8.7411	2.1125	21.1672	LPN	3a
D	11.3122	5.0830		BP	1b

TYPICAL APPLICATIONS

LTC1068 8th Order Linear Phase Bandpass, $f_{CENTER} = f_{CLK}/100$, Passband –3dB at (0.88)(f_{CENTER}) and (1.12)(f_{CENTER}). Maximum f_{CENTER} = 50kHz with ±5V Supplies



Gain vs Frequency



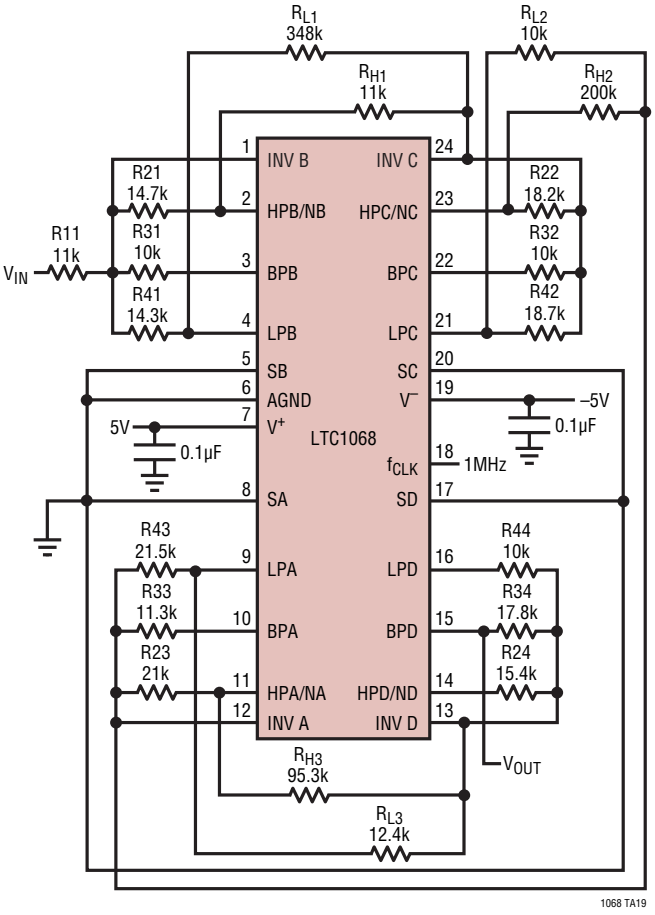
24-Lead Package

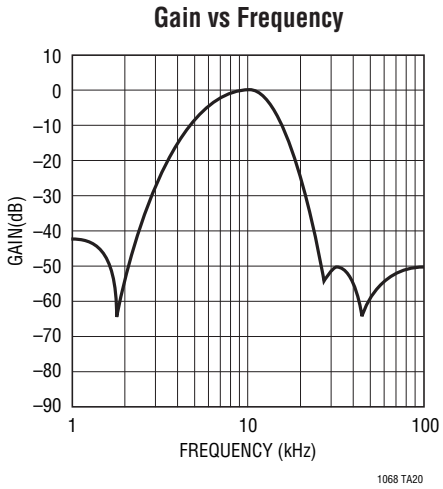
FilterCAD Custom Inputs for f_C = 10kHz

2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	TYPE	MODE
B	10.4569	2.6999	17.4706	LPN	2n
C	11.7607	3.9841		BP	2
A	8.6632	2.1384		BP	2b
D	9.0909	1.8356		BP	3

TYPICAL APPLICATIONS

LTC1068 8th Order Linear Phase Bandpass, $f_{CENTER} = f_{CLK}/100$, Passband –3dB at (0.7)(f_{CENTER}) and (1.3)(f_{CENTER}), Superior Sinewave Burst Response, Maximum f_{CENTER} = 60kHz with ±5V Supplies





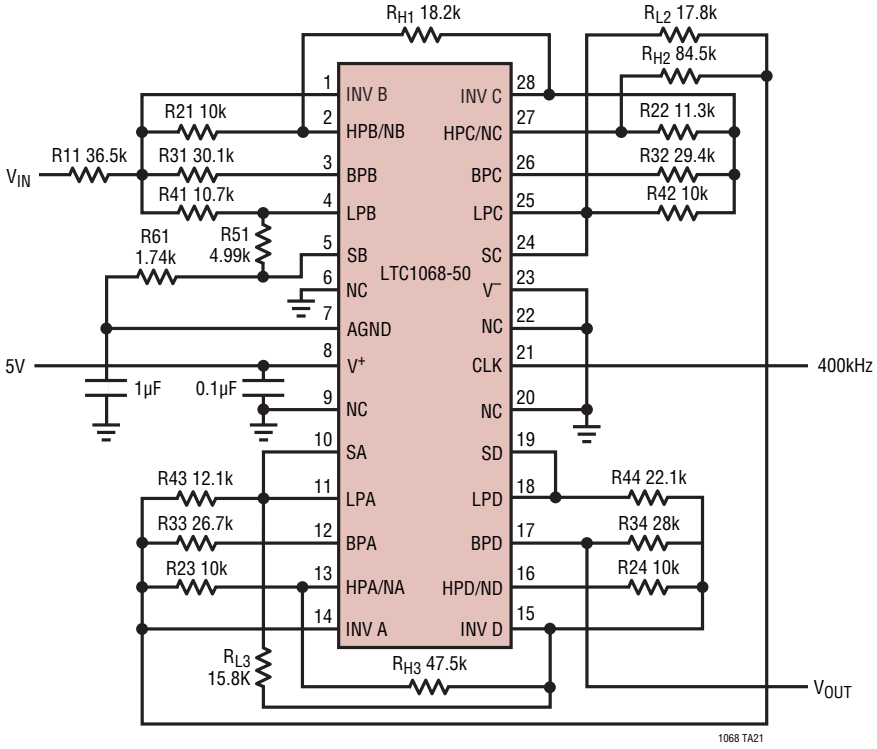
24-Lead Package

FilterCAD Custom Inputs for f_C = 10kHz

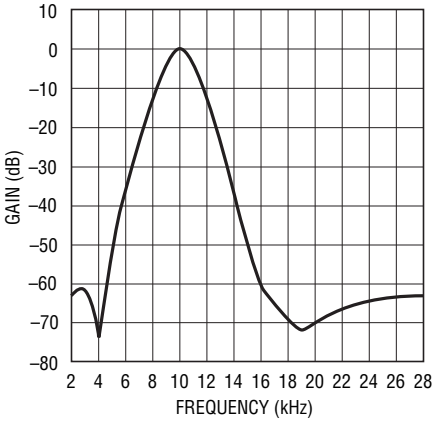
2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	Q_N	TYPE	MODE
B	10.1389	0.7087	1.7779		HPN	3a
C	9.8654	0.5540	44.7214		LPN	3a
A	9.8830	0.5434	27.7227		LPN	3a
D	12.4097	1.5264			BP	3

TYPICAL APPLICATIONS

LTC1068-50 8th Order Linear Phase Bandpass, $f_{CENTER} = f_{CLK}/40$, Passband –3dB at (0.8)(f_{CENTER}) and (1.2)(f_{CENTER}) for Single Supply Low Power Applications. Maximum f_{CENTER} = 25kHz with a Single 5V Supply



Gain vs Frequency

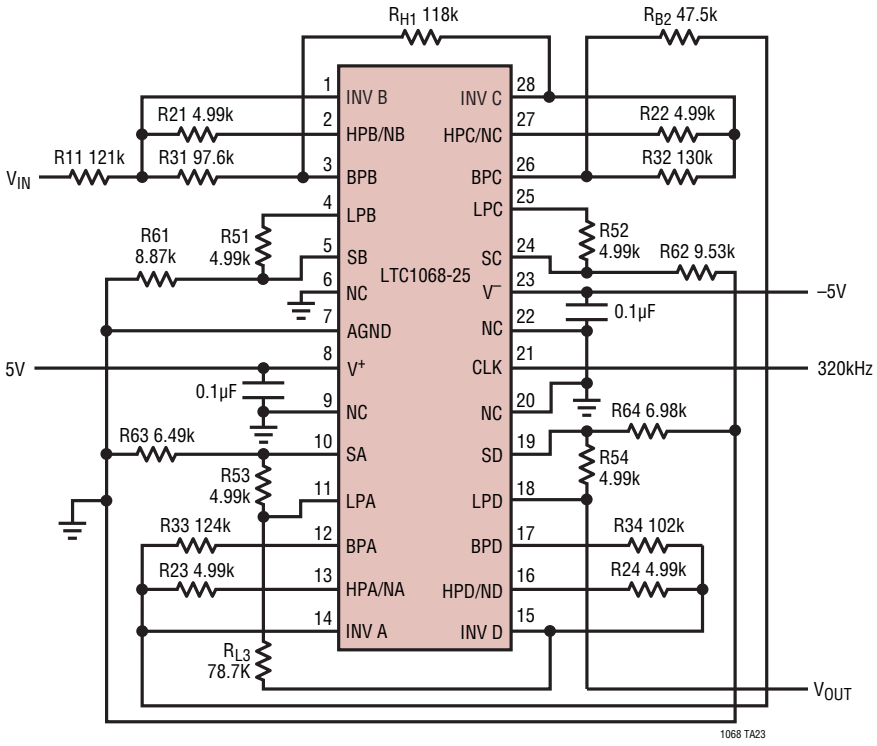


FilterCAD Custom Inputs for f_C = 10kHz

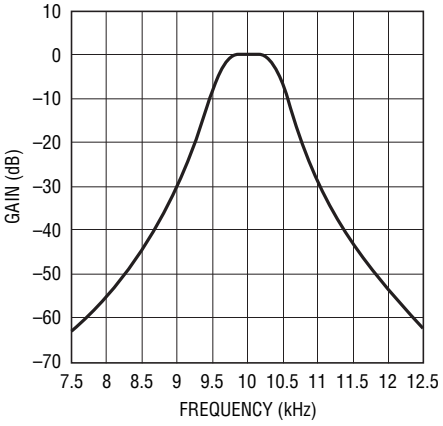
2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	TYPE	MODE
B	8.7384	4.0091	4.0678	HPN	2b
C	11.6756	4.6752	19.1786	LPN	2n
A	10.8117	4.2066	16.0127	LPN	2n
D	9.6415	3.6831		BP	2

TYPICAL APPLICATIONS

LTC1068-25 8th Order Order Bandpass, $f_{CENTER} = f_{CLK}/32$, Passband –3dB at (0.965)(f_{CENTER}) and (1.35)(f_{CENTER}). Maximum f_{CENTER} = 80kHz with ±5V Supplies



Gain vs Frequency

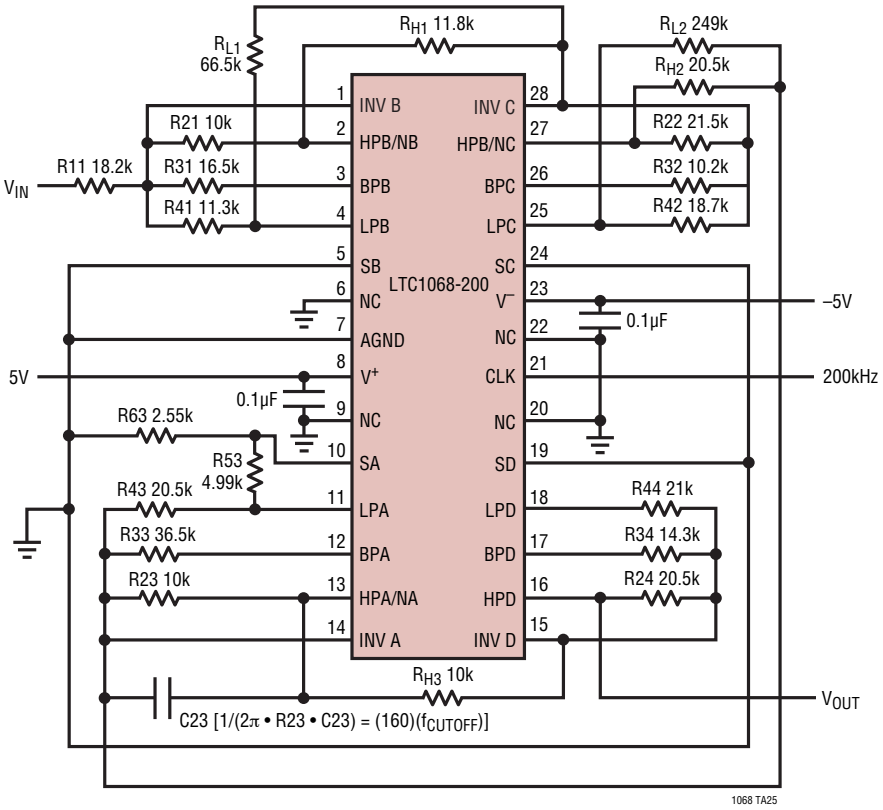


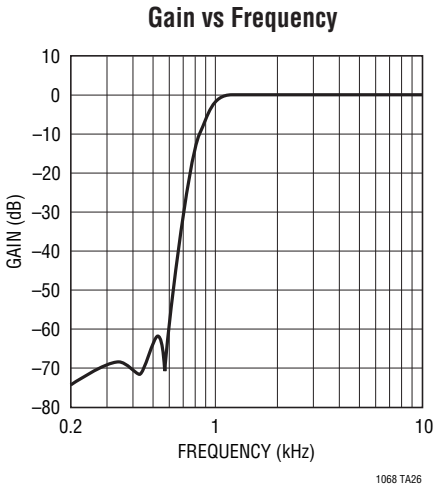
FilterCAD Custom Inputs for f_C = 10kHz

2nd ORDER SECTION	f_0 (kHz)	Q	TYPE	MODE
B	10.2398	15.6469	BP	1b
C	10.3699	21.1060	BP	1b
A	9.6241	18.6841	LP	1b
D	9.7744	15.6092	LP	1b

TYPICAL APPLICATIONS

LTC1068-200 8th Order Highpass, $f_{CENTER} = f_{CLK}/200$, Attenuation –60dB at (0.6)(f_{CENTER}). Maximum f_{CUTOFF} = 20kHz with ±5V Supplies





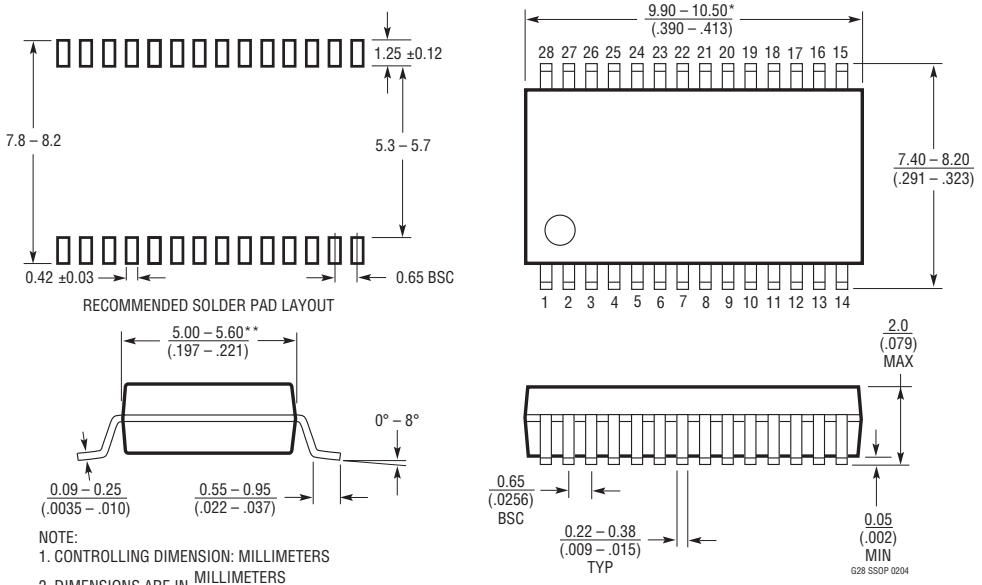
FilterCAD Custom Inputs for f_C = 1kHz

2nd ORDER SECTION	f_0 (kHz)	Q	f_N (kHz)	TYPE	MODE
B	0.9407	1.5964	0.4212	HPN	3a
C	1.0723	0.5156	0.2869	HPN	3a
A	0.9088	3.4293	0.5815	HPN	2b
D	0.9880	0.7001	0.0000	HP	3

PACKAGE DESCRIPTION

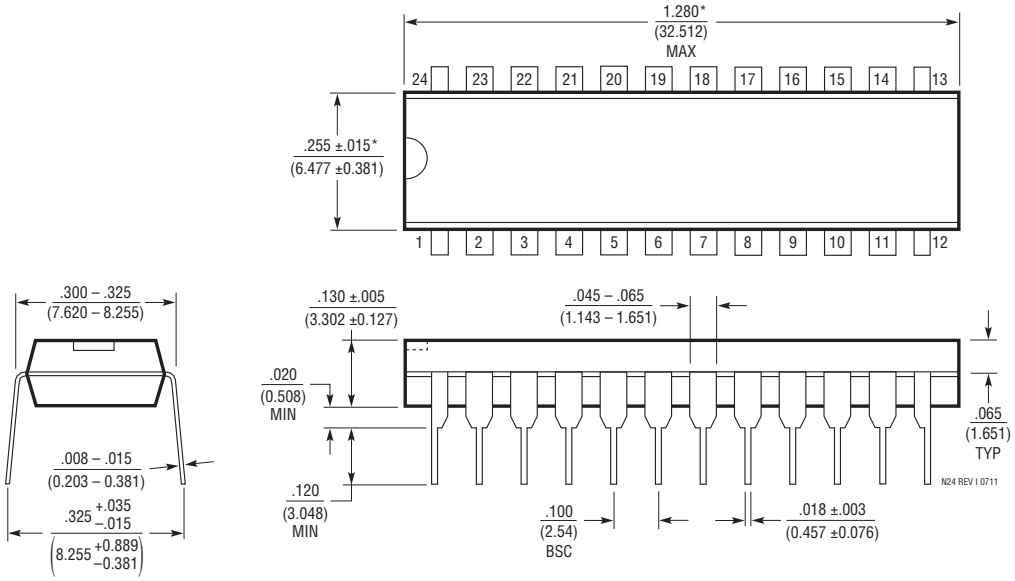
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

N Package
24-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



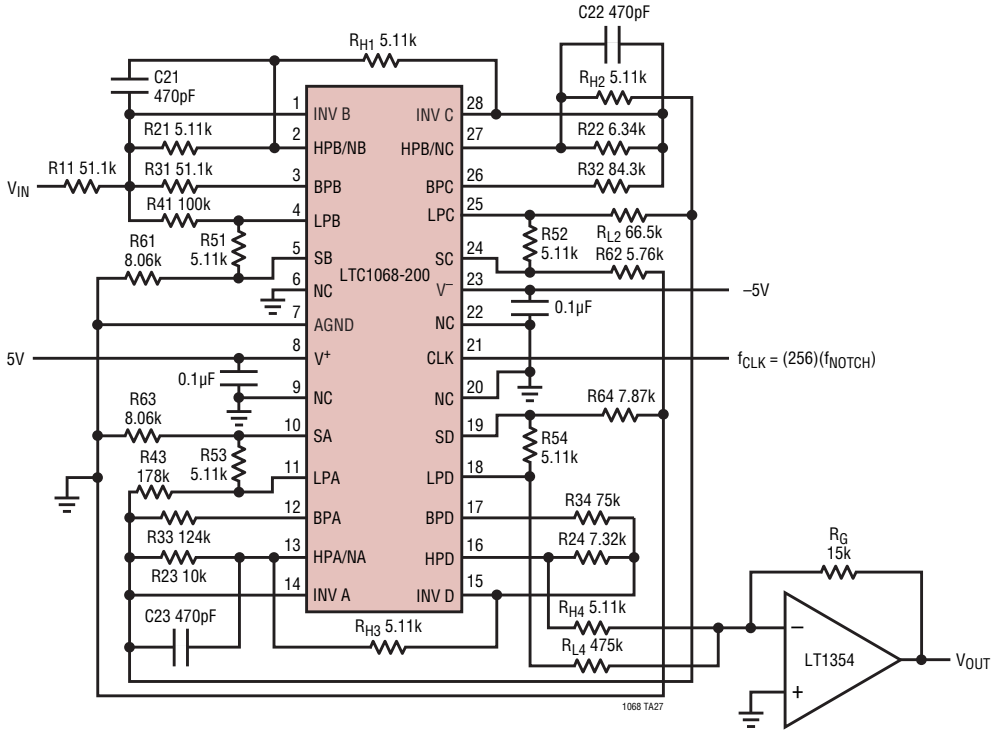
NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

REVISION HISTORY (Revision history begins at Rev C)

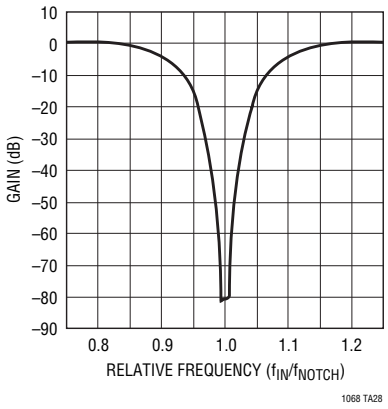
REV	DATE	DESCRIPTION	PAGE NUMBER
C	10/12	Correction to Electrical Characteristics table to identify characteristics of LTC1068-50	5

TYPICAL APPLICATION

LTC1068-200 8th Order Notch, $f_{NOTCH} = f_{CLK}/256$, f – 3dB at (0.9) (f_{NOTCH}) and (1.05)(f_{NOTCH}), Attenuation at f_{NOTCH} Greater Than 70dB for f_{NOTCH} in the Frequency Range 200Hz to 5kHz



Gain vs Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1064	Universal Filter, Quad 2nd Order	50:1 and 100:1 Clock-to-f_0 Ratios, f_0 to 100kHz, V_S = Up to ±7.5V
LTC1067/LTC1067-50	Low Power, Dual 2nd Order	Rail-to-Rail, V_S = 3V to ±5V
LTC1164	Low Power Universal Filter, Quad 2nd Order	50:1 and 100:1 Clock-to-f_0 Ratios, f_0 to 20kHz, V_S = Up to ±7.5V
LTC1264	High Speed Universal Filter, Quad 2nd Order	20:1 Clock-to-f_0 Ratio, f_0 to 200kHz, V_S = Up to ±7.5V

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