FAIRCHILD
A Schlumberger Company

F9423
FIFO Buffer Memory

Microprocessor Product

Description

The Fairchild F9423 is an expandable fall-through-type high-speed first-in, first-out (FIFO) buffer memory that is optimized for high-speed disk or tape controller and communication buffer applications. It is organized as 64 words by 4 bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The F9423 has 3-state outputs that provide added versatility, and is fully compatible with all TTL families.

- **Serial or Parallel Input**
- **Serial or Parallel Output**
- **Expandable Without Additional Logic**
- **3-State Outputs**
- **Fully Compatible With All TTL Families**
- **Slim 24-Pin Package**

Device Organization

As shown in figure 1, the F9423 consists of three sections:

1. An input register with parallel and serial data inputs, as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit-wide, 62-word-deep fall-through stack with self-contained control logic.
3. An output register with parallel and serial data outputs, as well as control inputs and outputs for output handshaking and expansion.

These three sections operate asynchronously and are virtually independent of one another.

Signal Functions

The F9423 FIFO signal functions are described in table 1

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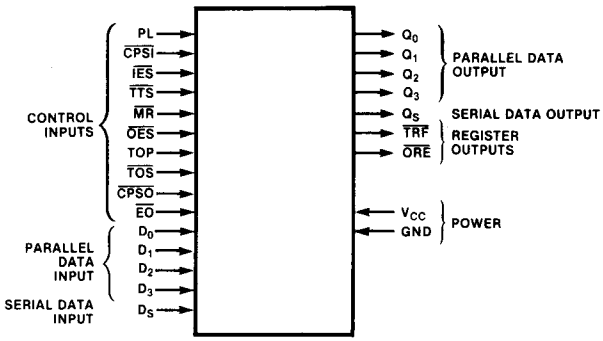
Signal Functions



Connection Diagram

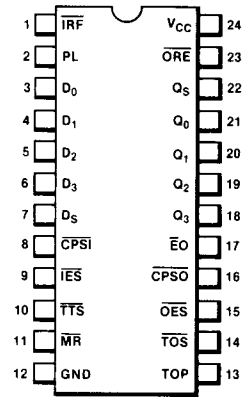
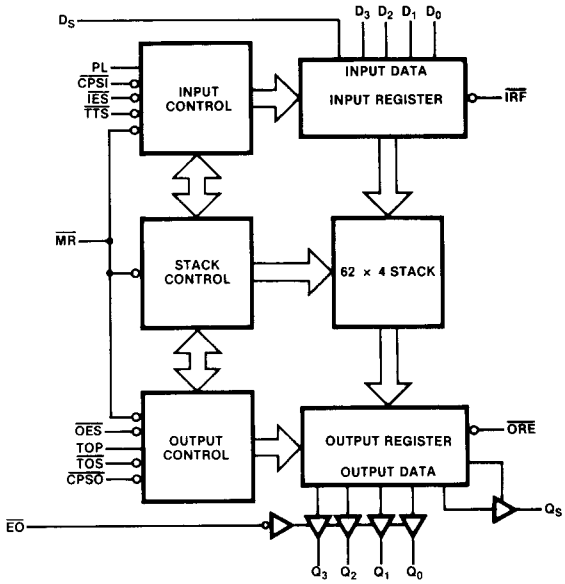


Table 1 Signal Functions

Mnemonic	Pin No.	Name	Description
Control Inputs			
PL	2	Parallel Load	Input signal that, when high, enables D_0 - D_3; not edge-triggered. Ones catching.
$\overline{CPSI}$	8	Serial Input Clock	Edge-triggered input signal that activates on the falling edge.
$\overline{IES}$	9	Serial Input Enable	Input signal that, when low, enables serial and parallel input.
$\overline{TTS}$	10	Transfer-to-Stack	Input signal that, when low, initiates fall-through.
$\overline{MR}$	11	Master Reset	Active-low input signal.
$\overline{OES}$	15	Serial Output Enable	Input signal that, when low, enables serial and parallel output.
TOP	13	Transfer Out Parallel	Input signal that, when high, enables a word to be transferred from the stack to the output register; not edge-triggered. (The $\overline{TOS}$ signal must be low for the transfer to occur.)
$\overline{TOS}$	14	Transfer Out Serial	Input signal that, when low, enables a word to be transferred from the stack to the output register; not edge-triggered. (The TOP signal must be high for the transfer to occur.)
$\overline{CPSO}$	16	Serial Output Clock	Edge-triggered input signal that activates on the falling edge.
$\overline{EO}$	17	Output Enable	Active-low input signal that allows data to be output.
Data Inputs			
D_0-D_3	3 - 6	Parallel Data	Parallel data inputs
D_S	7	Serial Data	Serial data inputs
Data Outputs			
Q_0-Q_3	18 - 21	Parallel Data	Parallel data outputs
Q_S	22	Serial Data	Serial data output
Register Status			
$\overline{IRF}$	1	Input Register Full	Output signal that, when low, indicates that the input register is full.
$\overline{ORE}$	23	Output Register Empty	Output signal that, when high, indicates that the output register contains valid data.
Power			
V_{CC}	24	Power Supply	Nominal +5 V
GND	12	Ground	Common power and signal return

Figure 1 F9423 Block Diagram



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Functional Description

Input Register

The input register can receive data in either bit-serial or 4-bit parallel form. It stores this data until it is sent to the fall-through stack, and also generates the necessary status and control signals.

This 5-bit register (see figure 2) is initialized by setting flip-flop F3 and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is output as the Input Register Full ($\overline{IRF}$) signal. After initialization, this output is high.

Parallel Entry

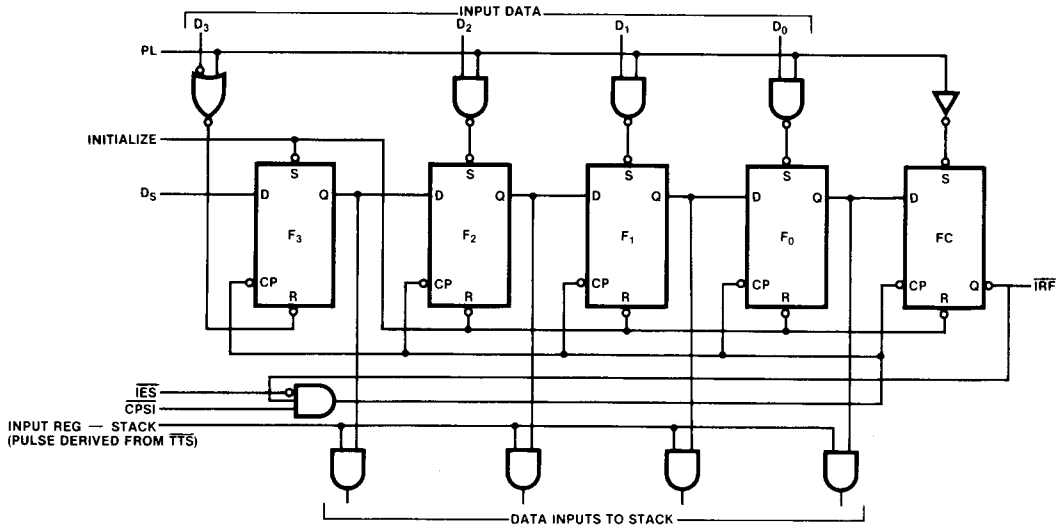
A high on the parallel load (PL) input loads the D_0 - D_3 inputs into the F_0 - F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output low, indicating that the input register is full. During parallel entry, the serial input clock ($\overline{CPSI}$) input must be low.

Serial Entry

Data on the serial data (D_S) input is serially entered into the shift register (F_3, F_2, F_1, F_0, FC) on each high-to-low transition of the $\overline{CPSI}$ input when the Serial Input Enable ($\overline{IES}$) signal is low. During serial entry, the PL input should be low.

After the fourth clock transition, the four data bits are located in flip-flops F_0 - F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output low and internally inhibiting $\overline{CPSI}$ pulses from effecting the register. Figure 3 illustrates the final positions in an F9423 resulting from a 256-bit serial bit train (B_0 is the first bit, B_{255} the last).

Figure 2 Input Register Conceptual Logic Diagram



Fall-Through Stack

The outputs of flip-flops F_0 - F_3 feed the stack. A low level on the transfer-to-stack ($\overline{TTS}$) input initiates a fall-through action; if the top location of the stack is empty, data is loaded into the stack and the input register is reinitialized. (Note that this initialization is delayed until PL is low.) Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS-type flip-flop (the initialization flip-flop) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack even though $\overline{IRF}$ and $\overline{TTS}$ may still be low; the initialization flip-flop is not cleared until PL goes low.

Once in the stack, data falls through automatically, pausing only when it is necessary to wait for an empty next location. In the F9423, the master reset ($\overline{MR}$) input only initializes the stack control section and does not clear the data.

Output Register

The output register (see figure 4) receives 4-bit data words from the bottom stack location, stores it, and outputs data on a 3-state, 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals.

Figure 3 Final Bit Positions Resulting from 256-Bit Serial Train

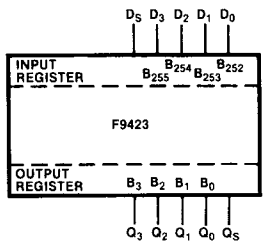
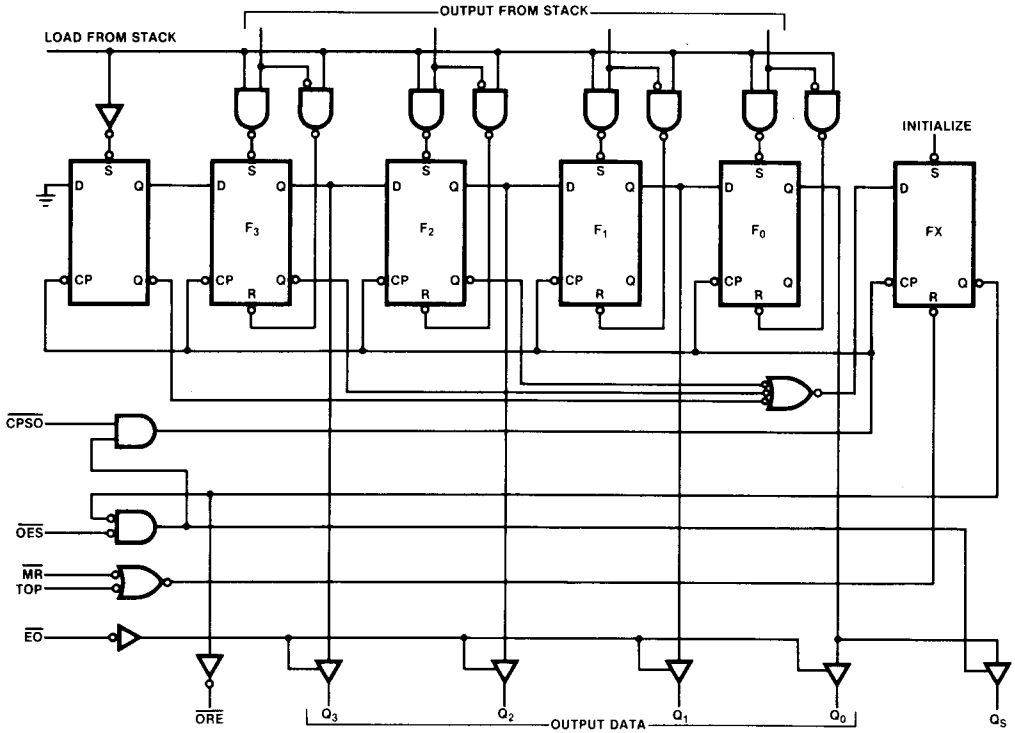


Figure 4 Output Register Conceptual Logic Diagram



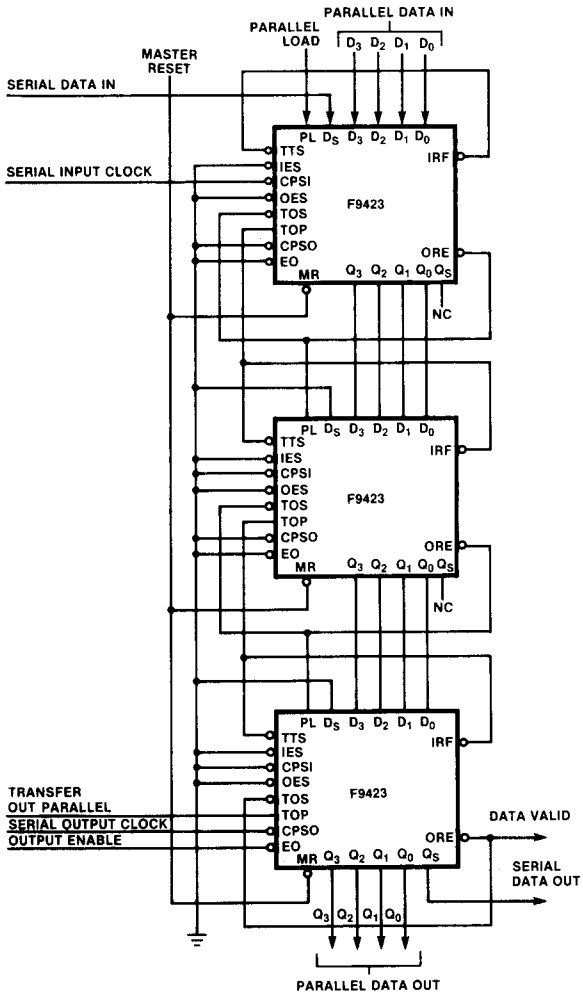
Parallel Extraction

When the FIFO is empty after a low pulse is applied to the $\overline{MR}$ input, the output register empty ($\overline{ORE}$) output is low. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the transfer out parallel ($\overline{TOP}$) input is high. As a result of the data transfer, $\overline{ORE}$ goes high, indicating valid data on the data outputs (provided that the 3-state buffer is enabled). The TOP input can then be used to clock out the next word.

When TOP goes low, $\overline{ORE}$ also goes low, indicating that the output data has been extracted; however, the data itself remains on the output bus until a high level on TOP permits the transfer of the next word (if available) into the output register. During parallel data extraction, the serial output clock ($\overline{CPSO}$) line should be low. The transfer out serial ($\overline{TOS}$) line should be grounded for single-slice operation or connected to the appropriate $\overline{ORE}$ line for expanded operation (refer to the "Expansion" section).

The TOP signal is not edge-triggered. Therefore, if TOP goes high before data is available from the stack but data becomes available before TOP again goes low, that data is transferred into the output register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes high and returns to low before data is available from the stack, $\overline{ORE}$ remains low, indicating that there is no valid data at the outputs.

Figure 5 190-Word x 4-Bit Vertical Expansion Scheme



Serial Extraction

When the FIFO is empty after a low is applied to the $\overline{MR}$ input, the $\overline{ORE}$ output is low. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the $\overline{TOS}$ input is low and TOP is high. As a result of the data transfer, $\overline{ORE}$ goes high, indicating that valid data is in the register.

The 3-state serial data output (Q_S) is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the high-to-low transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be low when the new word is being loaded into the output register. The fourth transition empties the shift register, forces $\overline{ORE}$ low, and disables the serial output, Q_S. For serial operation, the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

Expansion

Vertical Expansion

The F9423 may be vertically expanded, without external components, to store more words. The interconnections necessary to form a 190-word by 4-bit FIFO are shown in figure 5. Using the same technique, any FIFO of 63n + 1 words by 4 bits can be configured, where n is the number of devices. Note that expansion does not sacrifice any of the F9423 flexibility for serial/parallel input and output.

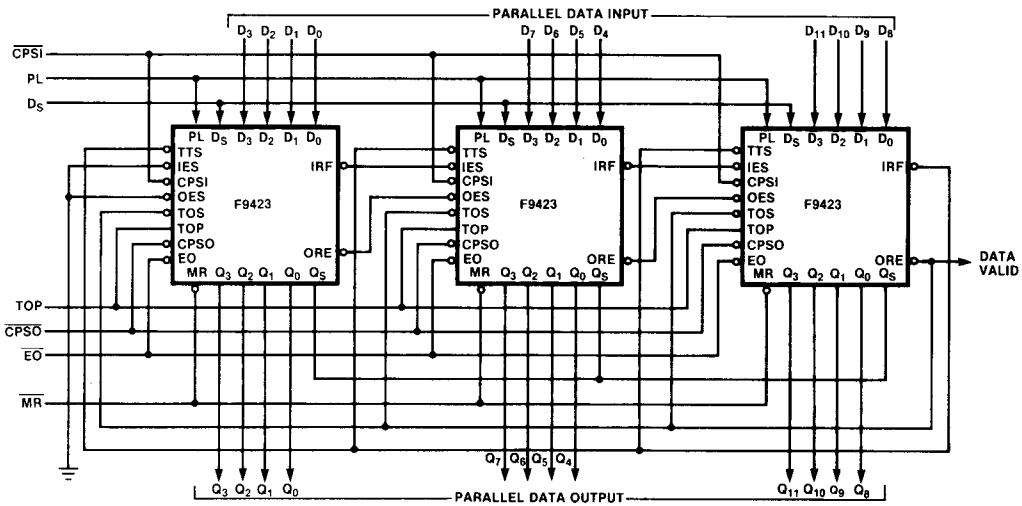
Horizontal Expansion

The F9423 can be horizontally expanded, without external logic, to store long words (in multiples of 4 bits). The interconnections necessary to form a 64-word by 12-bit FIFO are shown in figure 6. Using the same technique, any FIFO of 64 words by 4n bits can be constructed, where n is the number of devices.

The right-most (most significant) device is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the F9423 flexibility for serial/parallel input and output.

It should be noted that the horizontal expansion scheme shown in figure 6 exacts a penalty in speed.

Figure 6 64-Word x 12-Bit Horizontal Expansion Scheme



Horizontal and Vertical Expansion

The F9423 can be expanded in both the horizontal and vertical directions without any external components and without sacrificing any of its FIFO flexibility for serial/parallel input and output. The interconnections necessary to form a 127-word by 16-bit FIFO are shown in figure 7. Using the same technique, any FIFO of 63m + 1 words by 4n bits can be configured, where m is the number of devices in a column and n is the number of devices in a row. Figures 8 and 9 illustrate the timing diagrams for serial data entry and extraction for the FIFO shown in figure 7. Figure 10 illustrates the final positions of bits in an expanded F9423 FIFO resulting from a 2032-bit serial bit train.

Interlocking Circuitry

Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit-to-unit operating speed require external gating to ensure that all devices have completed an operation. The F9423 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the F9423 array of figure 7, devices 1 and 5 are the row masters; the other devices are slaves to the master in their rows. No slave in a given row initializes its input register until it has received a low on its $\overline{IES}$ input from a row master or a slave of higher priority.

Similarly, the $\overline{ORE}$ outputs of slaves do not go high until their inputs have gone high. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes high and that output data for the array may be extracted when the $\overline{ORE}$ output of the final slave in the output row goes high.

The row master is established by connecting its $\overline{IES}$ input to ground, while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next-higher priority device. When an array of F9423 FIFOs is initialized with a low on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices are high. Thus, only the row master receives a low on the $\overline{IES}$ input during initialization.

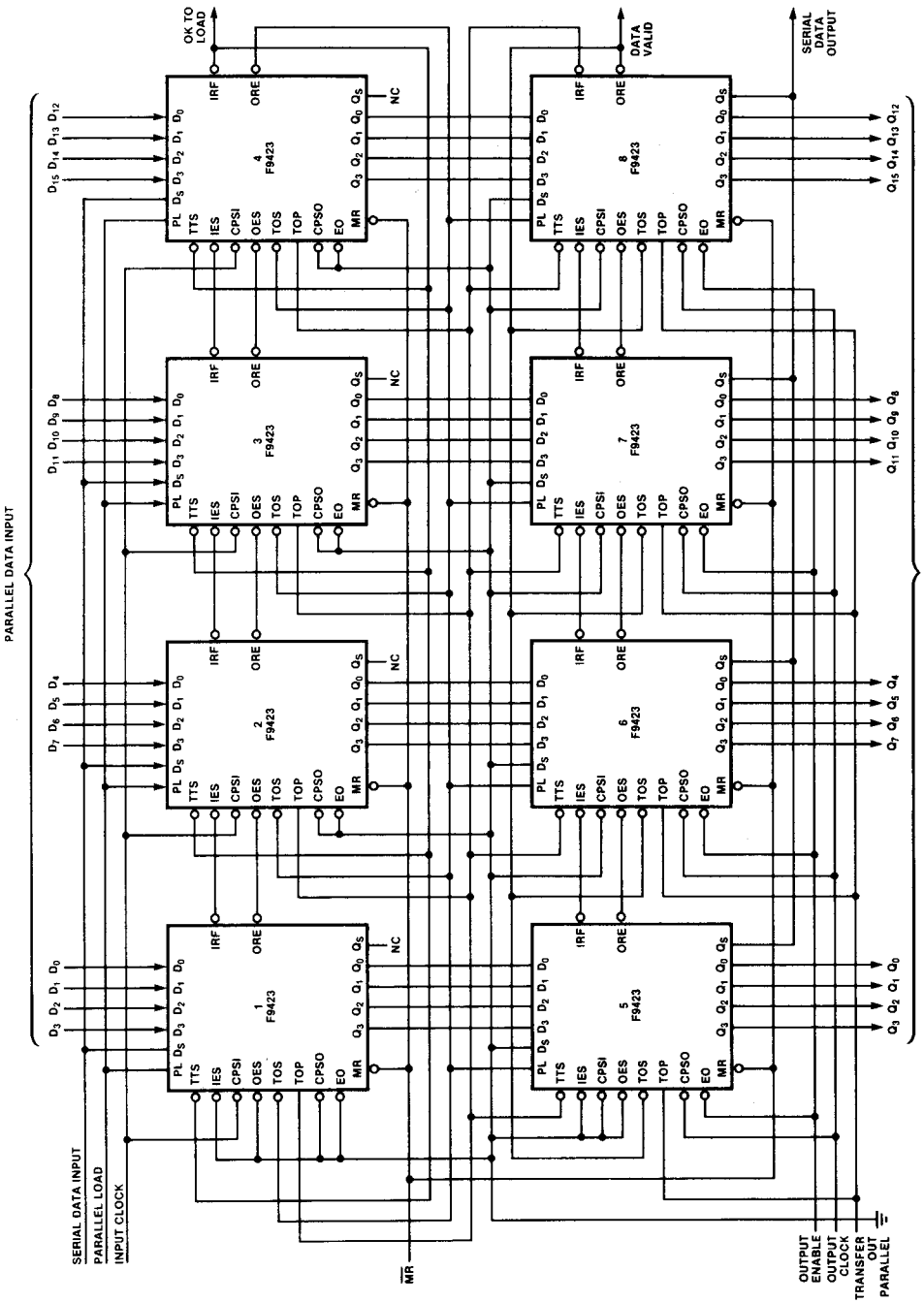


Figure 7 127-Word × 16-Bit FIFO Array

Figure 8 Serial Data Entry for 127 × 16 Array

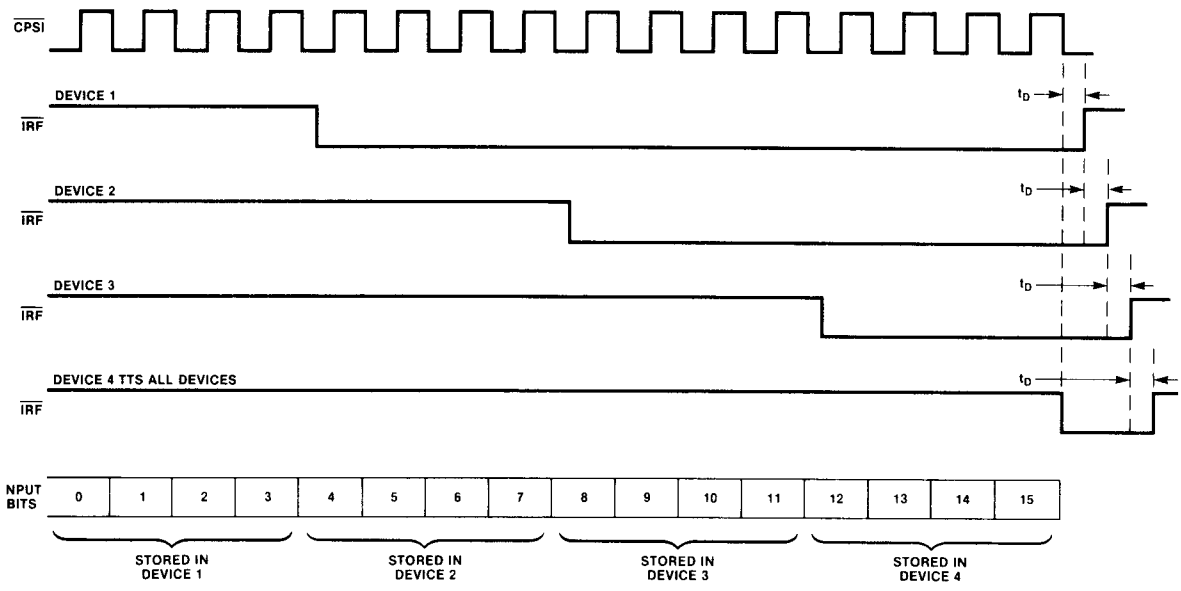


Figure 9 Serial Data Extraction for 127 × 16 Array

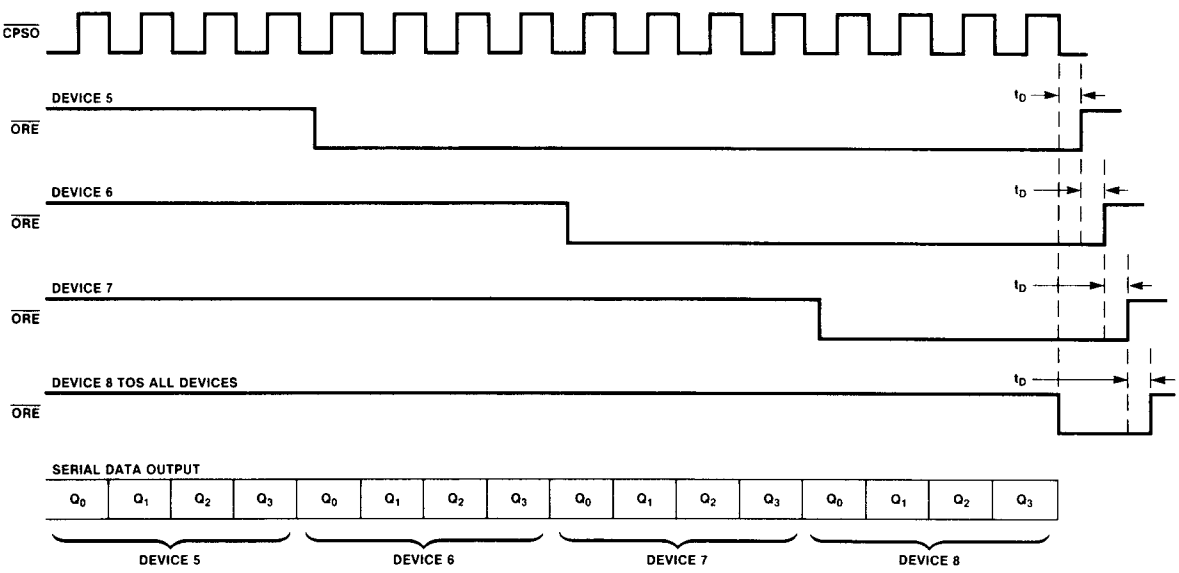


Figure 10 Final Position of 2032-Bit Serial Input

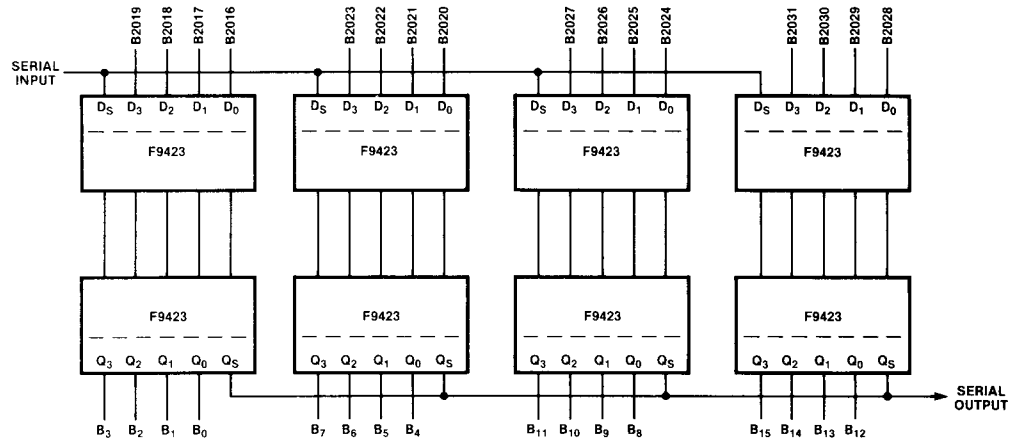


Figure 11 Interlocking Circuitry Conceptual Logic Diagram

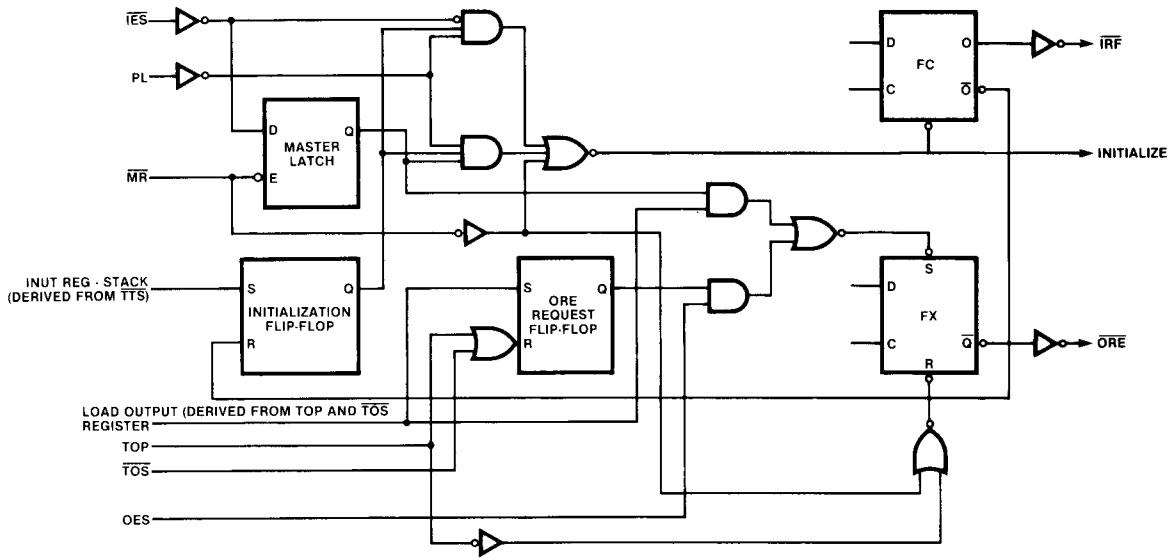


Figure 11 is a conceptual logic diagram of the internal circuitry that determines master/slave operation. When $\overline{MR}$ and $\overline{IES}$ are low, the master latch is set. When $\overline{TTS}$ goes low, the initialization flip-flop is set. If the master latch is high, the input register is immediately initialized and the initialization flip-flop reset. If the master latch is reset, the input register is not initialized until $\overline{IES}$ goes low. In array operaton, activating $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ request flip-flop. If the master latch is set, the last output register flip-flop is set and the $\overline{ORE}$ line goes high. If the master latch is reset, the $\overline{ORE}$ output is low until a serial output enable ($\overline{OES}$) input is received.

Timing Characteristics

Table 2 describes, and figures 12 through 19 illustrate, the F9423 timing characteristics.

Table 2 Timing Characteristics

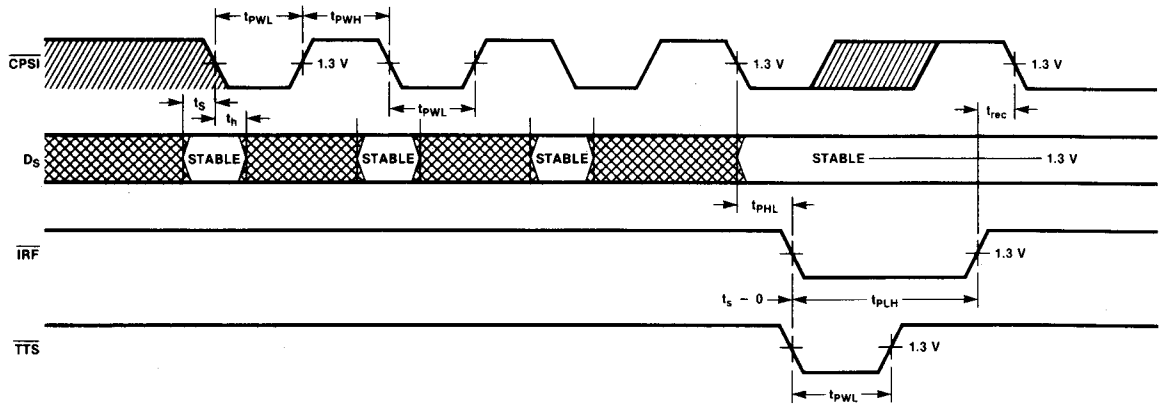
Symbol	Characteristic[1]	Limits			Units	Comments
		Min	Typ	Max		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output		30	40	ns	Stack not full, PL low (see figures 12 and 13).
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$		68	90	ns	
t_{PLH}	Propagation Delay, Negative-Going $\overline{CPSO}$ to Q_S Output		46	55	ns	$\overline{OES}$ low, TOP high (see figures 14 and 15).
t_{PHL}			30	40	ns	
t_{PLH}	Propagation Delay, Positive-Going TOP to Q_0-Q_3 Outputs		80	95	ns	$\overline{EO}$, $\overline{CPSO}$ low (see figure 16).
t_{PHL}			68	80	ns	
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$		29	50	ns	$\overline{OES}$ low, TOP high (see figures 14 and 15).
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$		39	60	ns	Parallel output, $\overline{EO}$, $\overline{CPSO}$ low (see figure 16).
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$		79	95	ns	
t_{DFT}	Fall-Through Time		3.6	4.3	μs	$\overline{TTS}$ connected to $\overline{IRF}$; $\overline{TOS}$ connected to $\overline{ORE}$; $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ low, TOP high (see figure 17).
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$		72	85	ns	Data in stack, TOP high (see figures 14 and 15).

Table 2 Timing Characteristics (Continued)

Symbol	Characteristics[1]	Limits			Units	Comments
		Min	Typ	Max		
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going $\overline{IRF}$		39	50	ns	Stack not full (see figures 18 and 19).
t_{PLH}	Propagation Delay, Negative-Going PL to Positive-Going $\overline{IRF}$		41	55	ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$		38	45	ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{IES}$ to Positive-Going $\overline{IRF}$		32	45	ns	See figure 19.
t_{PZL} t_{PZH}	Propagation Delay, $\overline{OE}$ to Q_0-Q_3		14	18	ns	Propagation delay out of the high-impedance state.
t_{PHZ} t_{PLZ}	Propagation delay, $\overline{OE}$ to Q_0-Q_3		16	20	ns	Propagation delay into the high-impedance state.
t_{PZL} t_{PZH}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S		14	20	ns	Propagation delay out of the high-impedance state.
t_{PLZ} t_{PHZ}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S		16	22	ns	Propagation delay into the high-impedance state.
t_{AP}	Parallel Appearance Time, $\overline{ORE}$ to Q_0-Q_3		4	6	ns	Time elapsed between $\overline{ORE}$ going high and valid data appearing at output. Negative number indicates data available before $\overline{ORE}$ goes high.
t_{AS}	Serial Appearance Time, $\overline{ORE}$ to Q_S		5	18	ns	

[1] V_{CC} = 5.0 V ±5%; C_L = 15 pF; T_A = 0°C to +75°C

Figure 12 Serial Input, Unexpanded or Master Operation



Conditions: Stack Not Full; $\overline{IES}$, PL Low

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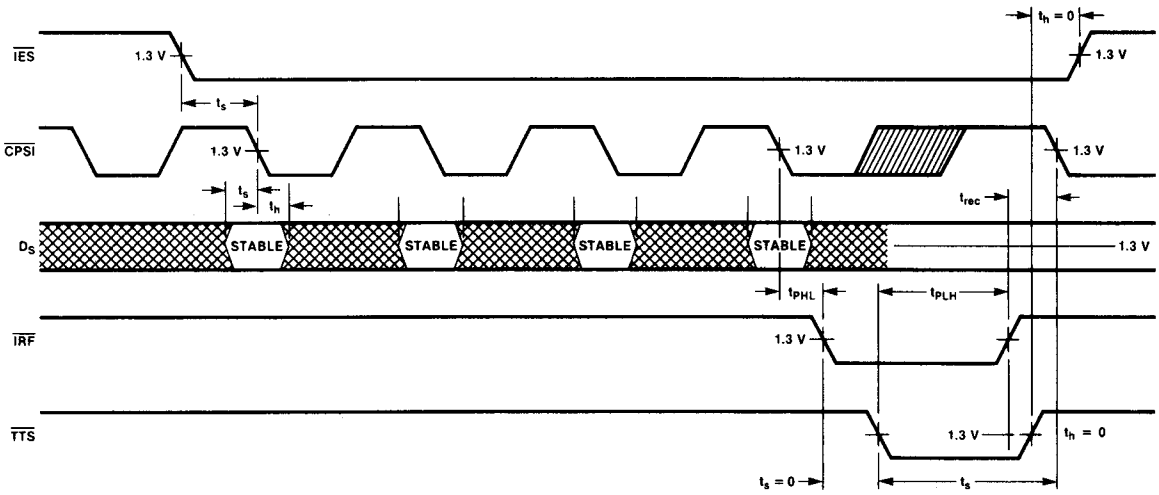
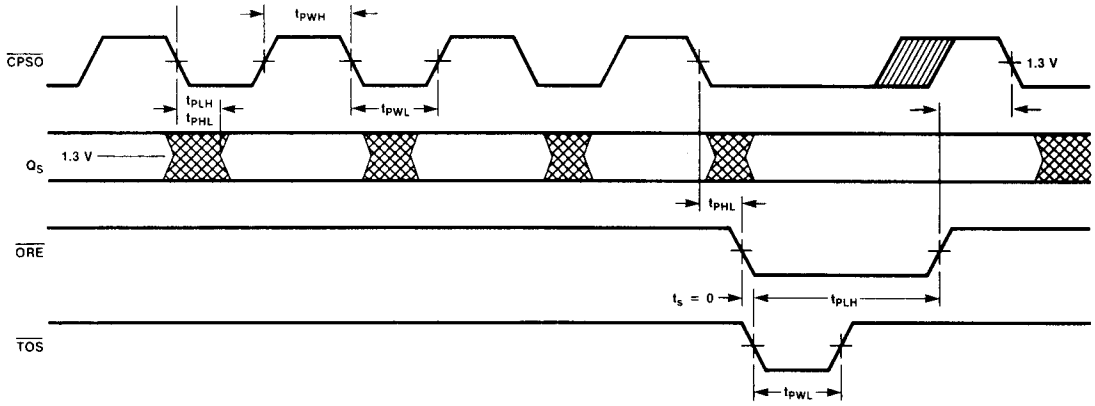
Figure 13 Serial Input, Expanded Slave Operation



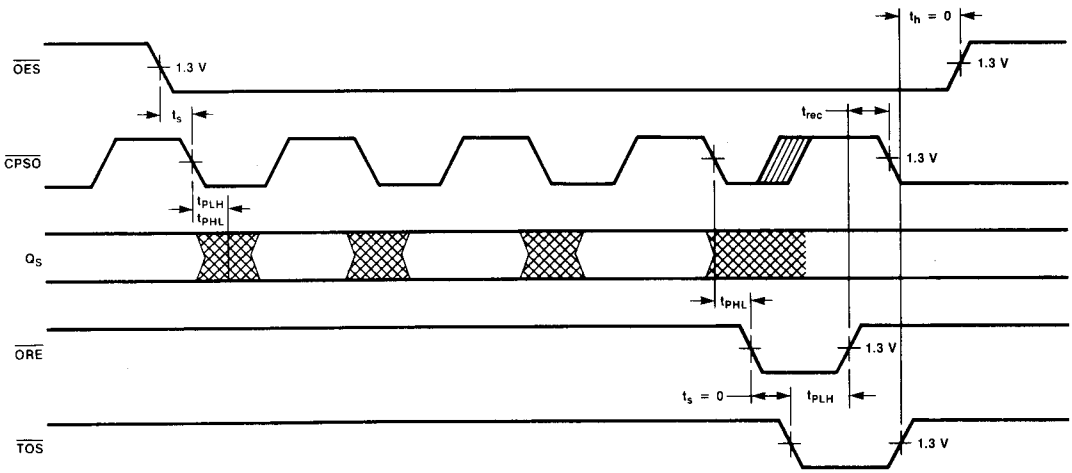
Conditions: Stack Not Full; $\overline{IES}$ High When Initiated; PL Low

Figure 14 Serial Output, Unexpanded or Master Operation



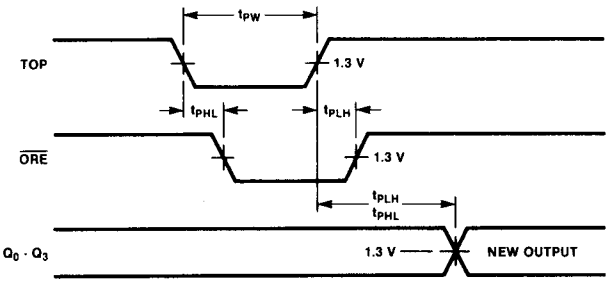
Conditions: Data in Stack; TOP High, $\overline{IES}$ Low When Initiated; $\overline{OES}$ Low

Figure 15 Serial Output, Slave Operation



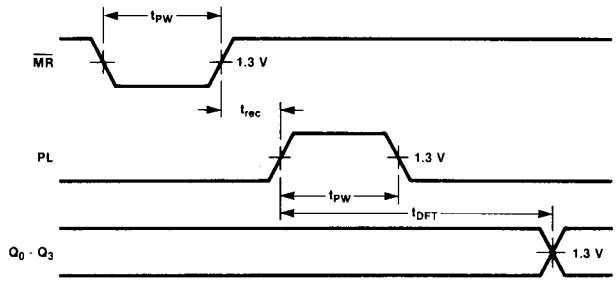
Conditions: Data In Stack; TOP High; $\overline{IES}$ High When Initiated

Figure 16 Parallel Output, 4-Bit Word or Master in Parallel in Expansion



Conditions: $\overline{IES}$ Low When Initiated; $\overline{EO}$, $\overline{CPSO}$ Low; Data Available In Stack

Figure 17 Fall-Through Time



Conditions: $\overline{TTS}$ Connected to $\overline{IRF}$; $\overline{TOS}$ Connected to $\overline{ORE}$; $\overline{IES}$, $\overline{OES}$, $\overline{CPSO}$ Low; TOP High

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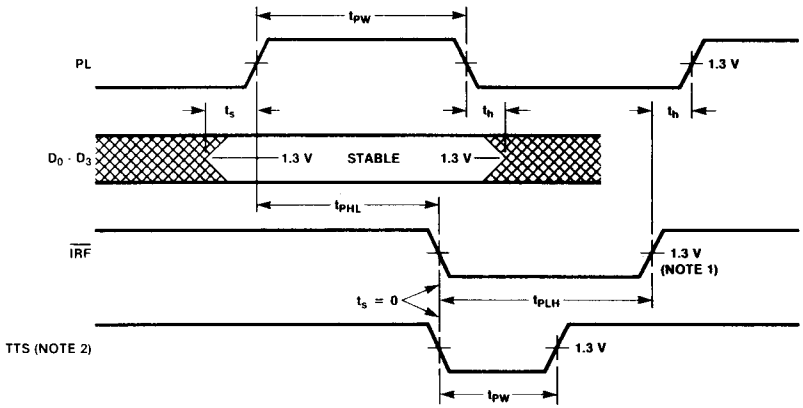
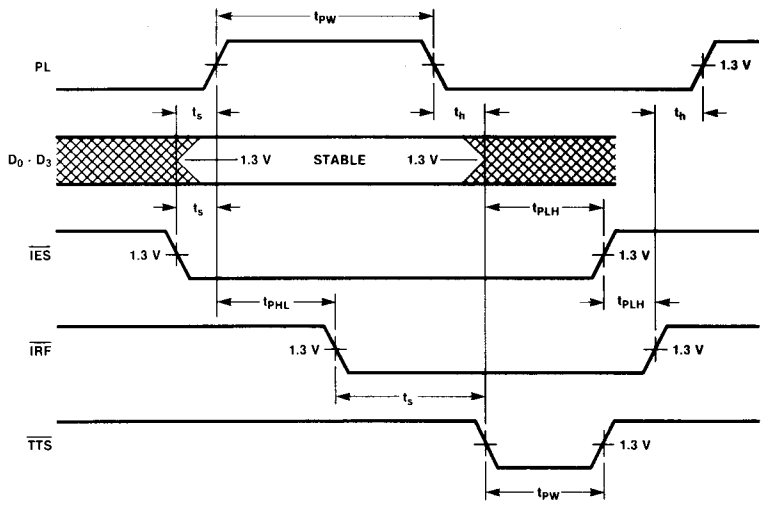
Figure 18 Parallel Load Mode, 4-Bit Word (Unexpanded) or Master in Parallel Expansion



NOTES:
[1] If stack is full, $\overline{IRF}$ stays low.
[2] $\overline{TTS}$ normally connected to $\overline{IRF}$.

Conditions: Stack Not Full; $\overline{IES}$ Low When Initialized

Figure 19 Parallel Load, Slave Mode



Conditions: Stack Not Full; Device Initialized With $\overline{IES}$ High;
Initialization Requires That a Master Reset Occur After
Power Is Applied

Timing Set-Up Requirements

Table 3 describes the F9423 timing set-up requirements.

Table 3 Timing Set-Up Requirements

Symbol	Characteristics[1]	Limits			Units	Comments
		Min	Typ	Max		
t_{PWH}	$\overline{CPSI}$ Pulse Width (High)	18	15		ns	Stack not full; PL low (see figures 12 and 13).
t_{PWL}	$\overline{CPSI}$ Pulse Width (Low)	22	15		ns	
t_{PWH}	PL Pulse Width (High)	11	10		ns	Stack not full (see figures 18 and 19).
t_{PWL}	$\overline{TTS}$ Pulse Width (Low) Serial or Parallel Mode	40	26		ns	Stack not full; (see figures 12, 13, 18, 19).
t_{PWL}	$\overline{MR}$ Pulse Width (Low)	35	22		ns	See figure 17.
t_{PWH}	TOP Pulse Width (High)	52	35		ns	$\overline{CPSO}$ low; data available in stack (see figure 16).
t_{PWL}	TOP Pulse Width (Low)	32	24		ns	
t_{PWH}	$\overline{CPSO}$ Pulse Width (High)	18	11		ns	TOP high; data in stack.
t_{PWL}	$\overline{CPSO}$ Pulse Width (Low)	25	17		ns	See figures 14 and 15.
t_s	Set-Up Time, D_S to Negative $\overline{CPSI}$	10	6		ns	PL low (see figures 12 and 13).
t_h	Hold Time, D_S to $\overline{CPSI}$	6	4		ns	PL low (see figures 12 and 13).
t_s	Set-Up Time, $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode	1	−17		ns	See figures 12, 13, 18, 19.
t_s	Set-Up Time, Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$	0	−26		ns	TOP high (see figures 14 and 15).
t_{rec}	Recovery Time, $\overline{MR}$ to Any Input	30	24		ns	See figure 17.
t_s	Set-Up Time, Negative-Going $\overline{IES}$ to $\overline{CPSI}$	18	15		ns	See figure 13.
t_s	Set-Up Time, Negative-Going $\overline{TTS}$ to $\overline{CPSI}$	110	83		ns	See figure 13.
t_s	Set-Up Time, Parallel Inputs to PL	0	−12		ns	Length of time parallel inputs must be applied prior to rising edge of PL.
t_h	Hold Time, Parallel Inputs to PL	20	10		ns	Length of time parallel inputs remain applied after falling edge of PL.

V_{CC} = 5.0 V; C_L = 15 pF; T_A = 25°C

DC Characteristics

Table 4 describes the F9423 dc characteristics.

Table 4 DC Characteristics

Symbol	Characteristic[1]	Limits[2]			Units	Test Conditions[3]
		Min	Typ	Max		
V_{IH}	Input High Voltage	2.0			V	Guaranteed input high voltage
V_{IL}	Input Low Voltage			0.8	V	Guaranteed input low voltage
V_{CD}	Input Clamp Diode Voltage		−0.9	−1.5	V	V_{CC} = Min; I_{IN} = −18 mA
V_{OH}	Output High Voltage, $\overline{ORE}$, $\overline{IRF}$	2.4	3.4		V	V_{CC} = Min; I_{OH} = −400 μA
V_{OH}	Output High Voltage, Q_0-Q_3, Q_S	2.4	3.1		V	V_{CC} = Min; I_{OH} = −5.7 mA
V_{OL}	Output Low Voltage, $\overline{ORE}$, $\overline{IRF}$		0.35	0.5	V	V_{CC} = Min; I_{OL} = 8.0 mA
V_{OL}	Output Low Voltage, Q_0-Q_3, Q_S		0.35	0.5	V	V_{CC} = Min; I_{OL} = 16 mA
I_{OZH}	Output Off High Current, Q_0-Q_3, Q_S			100	μA	V_{CC} = Max; V_{OUT} = 2.4 V; V_E = 2.0 V
I_{OZL}	Output Off Low Current, Q_0-Q_3, Q_s			−100	μA	V_{CC} = Max; V_{OUT} = 0.5 V; V_E = 2.0 V
I_{IH}	Input High Current		1.0	40	μA	V_{CC} = Max; V_{IN} = 2.7 V
				1.0	mA	V_{CC} = Max; V_{IN} = 5.5 V
I_{IL}	Input Low Current, Except $\overline{OES}$, $\overline{MR}$			−0.4	mA	V_{CC} = Max; V_{IN} = 0.4 V
	Input Low Current, $\overline{OES}$, $\overline{MR}$			−0.8	mA	
I_{OS}[4]	Output Short Circuit Current $\overline{ORE}$, $\overline{IRF}$	−15		−100	mA	V_{CC} = Max; V_{OUT} = 0 V
	Q_0-Q_3, Q_S	−30		−130	mA	
I_{CC}	Supply Current		140	180	mA	V_{CC} = Max; inputs open

Notes

1. Typical limits are at V_{CC} = 5.0 V ±5%, T_A = 0°C to +75°C, and Max loading. The temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (junction-to-ambient) at 400 fpm air flow = 50°C/W, ceramic DIP; 65° C/W, plastic DIP.
   θ_{JA} (junction-to-ambient) in still air = 90°C/W, ceramic DIP; 110°C/W, plastic DIP.
   θ_{JC} (junction-to-case) = 25°C/W, ceramic DIP; 25°C/W, plastic DIP.

2. The specified limits represent the worst-case values for the characteristic. Since these values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

3. Conditions for testing not shown in the table are chosen to guarantee operation under worst-case conditions.

4. Duration of short circuit should not exceed 1 second; not more than one output should be shorted at a time.

Absolute Maximum Ratings

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this document, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

Storage Temperature	−65 °C, +150 °C
Temperature (Ambient) Under Bias	−55 °C, +125 °C
V_{CC} Pin Potential to Ground Pin	−0.5 V, +6.0 V
*Input Voltage (DC)	−0.5V, +5.5 V
*Input Current (DC)	−12 mA, +5.0 mA
**Voltage Applied to Outputs (Output High)	−0.5V, +5.5V
Output Current (Output Low)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.
**Output current limit required.

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Typ	Max	
F9423XC	4.75 V	5.0 V	5.25 V	0 °C to +75 °C

X = package type (D for ceramic DIP, P for plastic DIP)

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