

74F413 64 x 4 First-In First-Out Buffer Memory with Parallel I/O

General Description

The F413 is an expandable fall-through type high-speed First-In First-Out (FIFO) buffer memory organized as 64 words by four bits. The 4-bit input and output registers record and transmit, respectively, asynchronous data in parallel form. Control pins on the input and output allow for handshaking and expansion. The 4-bit wide, 62-bit deep fall-through stack has self-contained control logic.

Features

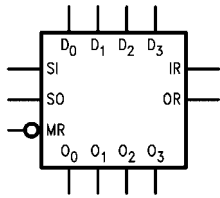
- Separate input and output clocks
- Parallel input and output
- Expandable without external logic
- 15 MHz data rate
- Supply current 160 mA max
- Available in SOIC, (300 mil only)

Ordering Code:

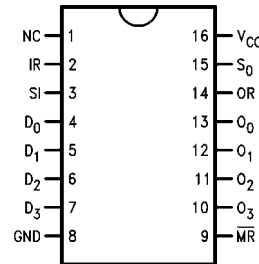
Order Number	Package Number	Package Description
74F413PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
D ₀ -D ₃	Data Inputs	1.0/0.667	20 μA/-0.4 mA
O ₀ -O ₃	Data Outputs	50/13.3	-1 mA/8 mA
IR	Input Ready	1.0/0.667	20 μA/-0.4 mA
SI	Shift In	1.0/0.667	20 μA/-0.4 mA
SO	Shift Out	1.0/0.667	20 μA/-0.4 mA
OR	Output Ready	1.0/0.667	20 μA/-0.4 mA
$\overline{\text{MR}}$	Master Reset	1.0/0.667	20 μA/-0.4 mA

Functional Description

Data Input— Data is entered into the FIFO on D_0 – D_3 inputs. To enter data the Input Ready (IR) should be HIGH, indicating that the first location is ready to accept data. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

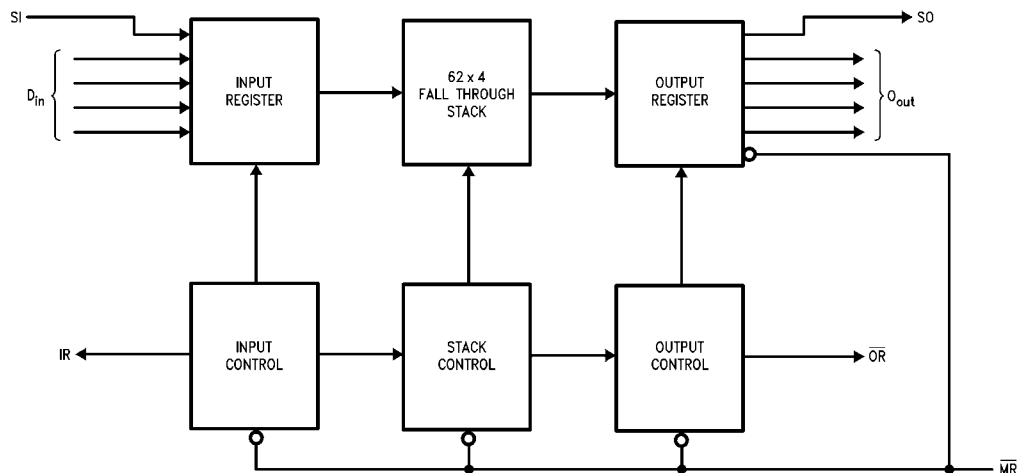
Data Transfer— Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will “bubble” to the front. The t_{PT} parameter

defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output— Data is read from the O_0 – O_3 outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW, the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_0 – O_3 remains as before, i.e., data does not change if FIFO is empty.

Input Ready and Output Ready— may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

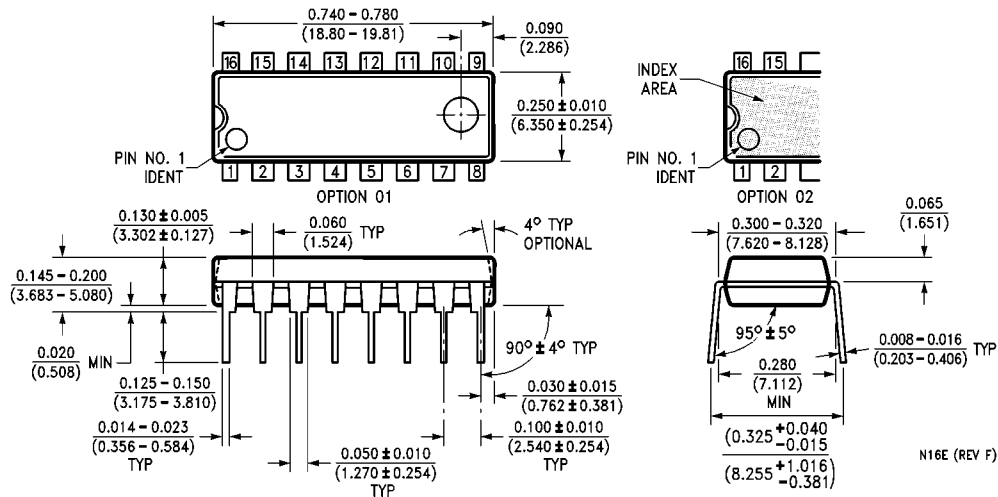
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.5	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.4 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 8 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.4	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-20		-130	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		115	160	mA	Max	V _O = HIGH

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{ to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Shift In Rate	10			8.0			10	MHz
f_{MAX}	Shift Out Rate	10			8.0			10	MHz
t_{PLH}	Propagation Delay	1.5		44.0	1.5	50.0	1.5	48.0	ns
t_{PHL}	Shift In to IR	1.5		31.0	1.5	37.0	1.5	35.0	ns
t_{PLH}	Propagation Delay	1.5		52.0	1.5	57.0	1.5	55.0	ns
t_{PHL}	Shift Out to OR	1.5		31.0	1.5	37.0	1.5	35.0	ns
t_{PLH}	Propagation Delay	1.5		46.0	1.5	52.0	1.5	50.0	ns
t_{PHL}	Output Data Delay	1.5		34.0	1.5	39.0	1.5	37.0	ns
t_{PLH}	Propagation Delay	1.5		27.0	1.5	33.0	1.5	31.0	ns
t_{PLH}	Master Reset to IR								ns
t_{PLH}	Propagation Delay	1.5		30.0	1.5	34.0	1.5	32.0	ns
t_{PLH}	Master Reset to OR								ns
AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{ to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	1.0		1.0		1.0		ns	
$t_S(L)$	D_n to SI	1.0		1.0		1.0		ns	
$t_H(H)$	Hold Time, HIGH or LOW	10.0		10.0		10.0		ns	
$t_H(L)$	D_n to SI	10.0		10.0		10.0		ns	
$t_W(H)$	Shift In Pulse Width	5.0		5.0		5.0		ns	
$t_W(L)$	HIGH or LOW	10.0		10.0		10.0		ns	
$t_W(H)$	Shift Out Pulse Width	7.5		8.5		7.5		ns	
$t_W(L)$	HIGH or LOW	10.0		10.0		10.0		ns	
$t_W(H)$	Input Ready Pulse Width, HIGH	7.5		8.5		7.5		ns	
$t_W(L)$	Output Ready Pulse Width, LOW	5.0		5.0		5.0		ns	
$t_W(L)$	Master Reset Pulse Width, LOW	10.0		10.0		10.0		ns	
t_{REC}	Recovery Time, MR to SI	32.0		35.0		35.0		ns	
t_{PT}	Data Throughput Time		0.9		1.0		1.0	μs	

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

N16E (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com