



# 67C401/13 67C402/23

First-In First-Out (FIFO) 64x4, 64x5 Memory  
10/15 MHz (Cascadable) CMOS

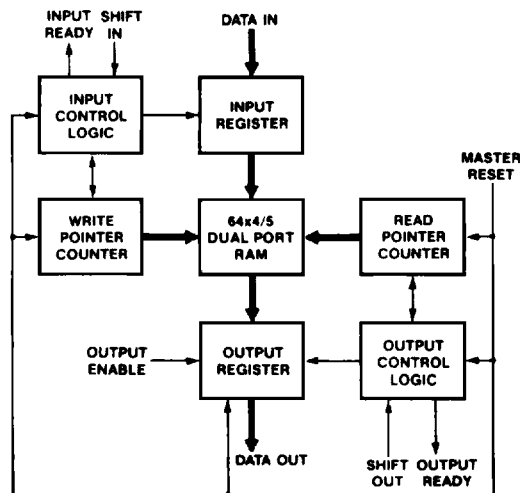
## Features

- Zero standby power
- High-speed 15-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- RAM-based architecture for short fall-through delay
- Full CMOS 8-transistor cell for maximum noise immunity
- Asynchronous operation
- Output Enable feature (67C4013/23)

## General Description

The 67C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out (FIFO) buffer memory products organized as 64 words by 4 or by 5 bits wide. These devices use Monolithic Memories' latest CMOS process technology and meet the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using both Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disc controllers, graphics, and communication network systems. The 550- $\mu$ watt standby power specification makes these devices ideal for ultra-low-power and battery-powered systems.

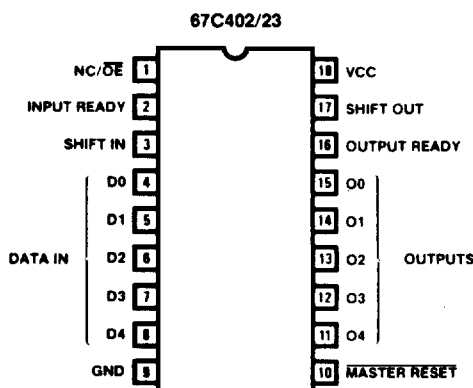
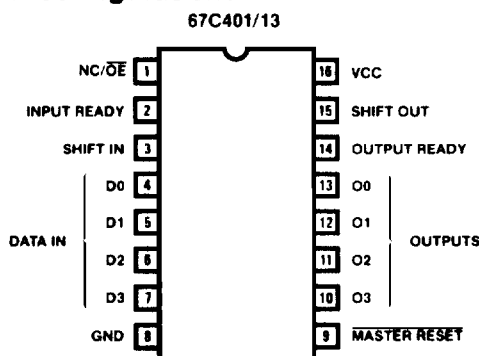
## Block Diagram



## Ordering Information

Part Number	Package	Temp	Output	Description
67401-10	CD 020, PD 020, PL 020	Com	Totem Pole	10 MHz 64x4
67401-15		Com	Totem Pole	15 MHz 64x4
674013-10		Com	3-State	10 MHz 64x4
674013-15		Com	3-State	15MHz 64x4
67C402-10		Com	Totem Pole	10MHz 64x5
67C402-15		Com	Totem Pole	15MHz 64x5
67C4023-10		Com	3-State	10MHz 64x5
67C4023-15		Com	3-State	15MHz 64x5

## Pin Configurations



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## Absolute Maximum Ratings

Supply voltage $V_{CC}$	-0.5 V to 7 V
Input voltage	-1.5 V to 7 V
Off-state output voltage	-0.5 V to $V_{CC} + 0.5$ V
Storage temperature	-65°C to +150°C
Power dissipation	1.0 W
Latch-up trigger current (all outputs)	140 mA

## Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$T_A$	Operating free-air temperature		0	70	0	70	°C
$f_{IN}$	Shift in rate	1		10		15	MHz
$t_{SIH}$	Shift in HIGH time	1.B	14		14		ns
$t_{SIL}$	Shift in LOW time	1	25		25		ns
$t_{IDS}$	Input data setup to SI (Shift In)	1	0		0		ns
$t_{IDH}$	Input data hold time from SI (Shift In)	1	40		40		ns
$t_{RIDS}$	Input data setup to IR (Input Ready)	3	0		0		ns
$t_{RIDH}$	Input data hold time from IR (Input Ready)	3	30		30		ns
$f_{OUT}$	Shift out rate	4		10		15	MHz
$t_{SOH}$	Shift out HIGH time	4.B	24		21		ns
$t_{SOL}$	Shift out LOW time	4	25		25		ns
$t_{MRW}^*$	Master Reset pulse	8	35		35		ns
$t_{MRS}$	Master Reset to SI	8	65		65		ns

\* See AC test and high-speed application note

## Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$V_{IL}^*$	Low-level input voltage			0.8		0.8	V
$V_{IH}^*$	High-level input voltage		2		2		V
$I_{IN}$	Input current	$V_{CC} = \text{MAX}$ $GND < V_{IN} < V_{CC}$	-1	1	-1	1	$\mu\text{A}$
$I_{OZ}$	Off-state output current	$V_{CC} = \text{MAX}$ $GND < V_{OUT} < V_{CC}$	-5	5	-5	5	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 20 \mu\text{A}$	0.1		0.1	V
			$I_{OL} = 8 \text{ mA}$	0.4		0.4	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -20 \mu\text{A}$	$V_{CC} - 0.1$		$V_{CC} - 0.1$	V
			$I_{OH} = -4 \text{ mA}$	2.4		2.4	
$I_{OS}^{**}$	Output short-circuit current	$V_{CC} = \text{MAX}$ $V_O = 0 \text{ V}$	-90	-20	-90	-20	mA
$I_{CC}$	Standby supply current	$V_{CC} = \text{MAX}$ $V_{IH} = V_{CC}$ $V_{IL} = GND$		100		100	$\mu\text{A}$
	Operating supply current	$I_{OUT} = 0$ $V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$ $f_{IN} = f_{OUT} = \text{MAX}$		35		45	mA

\* These are absolute voltages with respect to GND (Pin 9) and include all overshoots due to system and/or tester noise

\*\* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second

## Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{IRL}^*$	Shift In $\uparrow$ to Input Ready LOW	1		60		55	ns
$t_{IRH}^*$	Shift In $\downarrow$ to Input Ready HIGH			50		50	ns
$t_{ORL}^*$	Shift Out $\uparrow$ to Output Ready LOW	4		55		45	ns
$t_{ORH}^*$	Shift Out $\downarrow$ to Output Ready HIGH			50		41	ns
$t_{ODH}$	Output Data Hold (previous word)		5		5		ns
$t_{ODS}$	Output Data Shift (next word)			35		30	ns
$t_{PT}$	Data throughput	3,6		100		90	ns
$t_{MRORL}$	Master Reset $\downarrow$ to Output Ready LOW	8		100		100	ns
$t_{MRIRH}$	Master Reset $\downarrow$ to Input Ready HIGH			100		100	ns
$t_{MRO}$	Master Reset $\downarrow$ to Outputs LOW			35		35	ns
$t_{IPH}$	Input ready pulse HIGH	3,B	19		16		ns
$t_{OPH}$	Output ready pulse HIGH	6,B	14		14		ns
$t_{ORD}$	Output ready $\uparrow$ to Data Valid	4		-3		-3	ns
$t_{PHZ}$	Output Disable Delay	A		25		25	ns
$t_{PLZ}$				25		25	
$t_{PZL}$	Output Enable Delay			30		30	ns
$t_{PZH}$				30		30	

\* See AC test and high-speed application note.

## Capacitances\*

SYMBOL	PARAMETER	TEST CONDITION	67C40X/XX-10		67C40X/XX-15		UNIT
			MIN	MAX	MIN	MAX	
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ $V_{CC} = 4.5\text{ V}$		10		10	pF
$C_{OUT}$	Output capacitance			7		7	pF

\* Not tested in production.

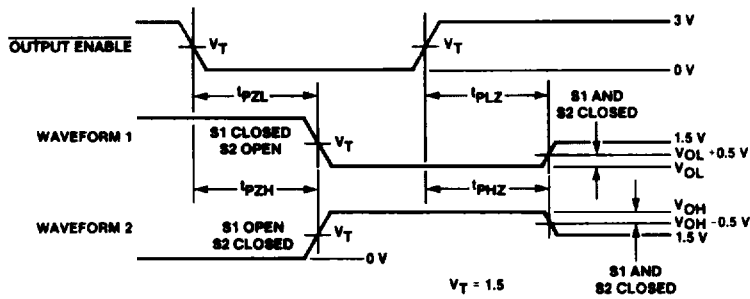
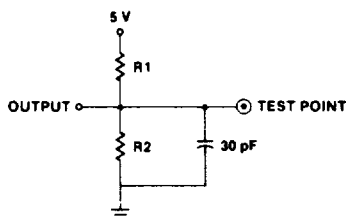


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

## Standard AC Test Load

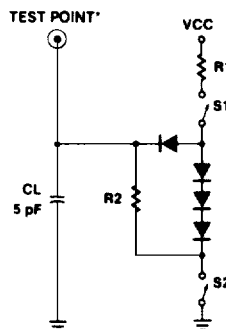


Input Pulse Amplitude = 3 V  
 Input Rise and Fall Time (10%-90%) = 2.5 ns  
 Measurements made at 1.5 V  
 All Diodes are 1N916 or 1N3064

## Resistor Values

I <sub>OL</sub>	R1	R2
8 mA	600 Ω	1200 Ω

## Three-State Test Load



## Functional Description

### Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D<sub>x</sub> inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

### Data Output

Data is read from the O<sub>x</sub> outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and O<sub>x</sub> remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T<sub>IDH</sub>) and the next activity of Input Ready (T<sub>IRL</sub>) to be extended relative to Shift-In going HIGH. This same type of problem is also related to T<sub>IRH</sub>, T<sub>ORL</sub>, and T<sub>ORH</sub> as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

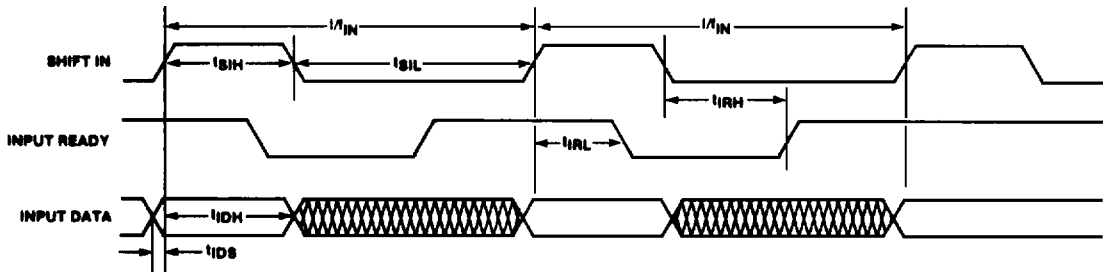


Figure 1. Input Timing

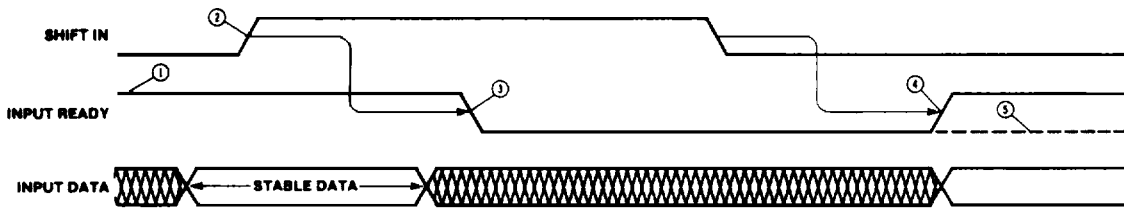


Figure 2. The Mechanism of Shifting Data into the FIFO

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- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first available memory location.
- ③ Input Ready goes LOW indicating this memory location is full.
- ④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
- ⑤ If the FIFO is already full then the Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

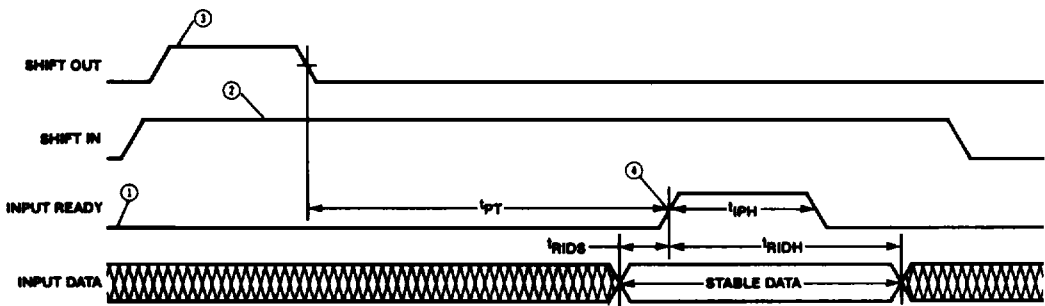


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- ① FIFO is initially full.
- ② Shift In is held HIGH.
- ③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
- ④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

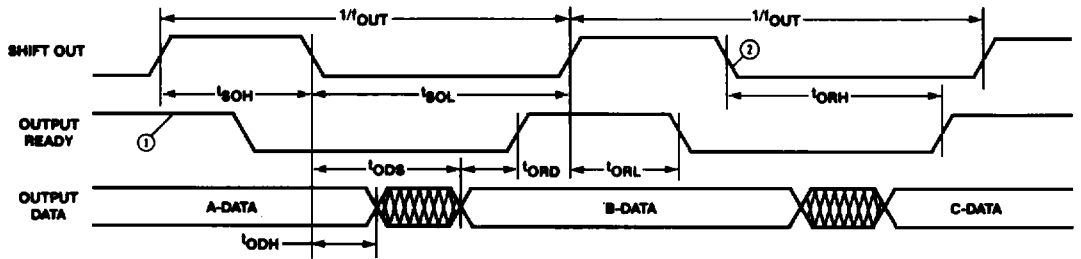


Figure 4. Output Timing

- ① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word)
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

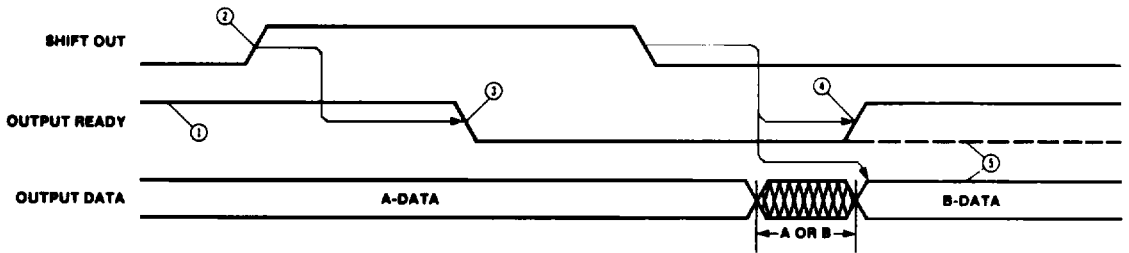


Figure 5. The Mechanism of Shifting Data Out of the FIFO

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
- ③ Output Ready goes LOW.
- ④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- ⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

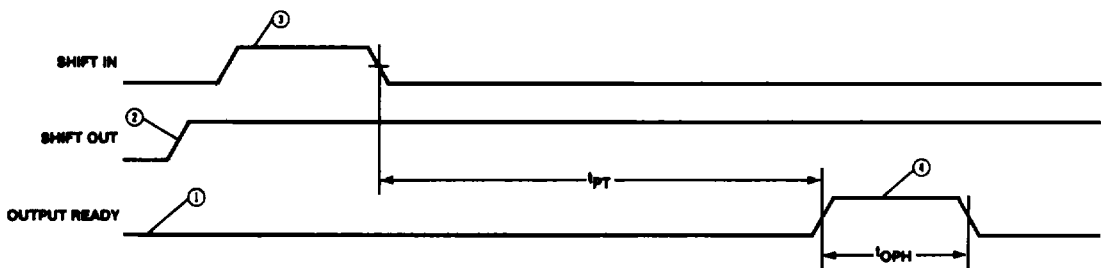


Figure 6.  $t_{PT}$  and  $t_{OPH}$  Specification

- ① FIFO initially empty.
- ② Shift-Out held HIGH.
- ③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
- ④ As soon as Output Ready becomes HIGH, the word is shifted out.

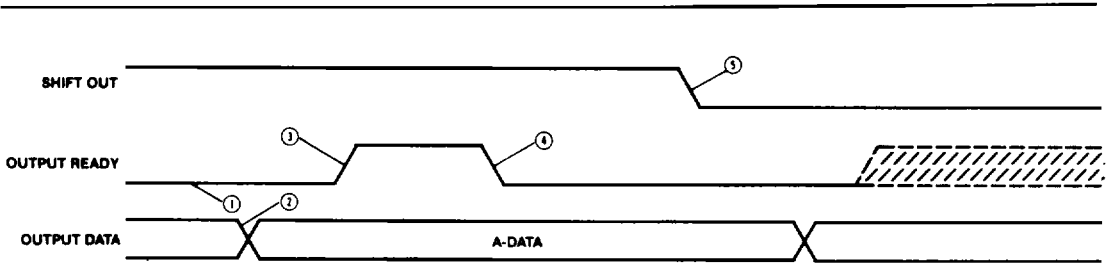


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

- ① The internal logic does not detect the presence of any words in the FIFO
- ① New data (A) arrives at the outputs
- ① Output Ready goes HIGH indicating arrival of the new data.
- ① Since Shift Out is held HIGH, Output Ready goes immediately LOW
- ① As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional words in the FIFO.

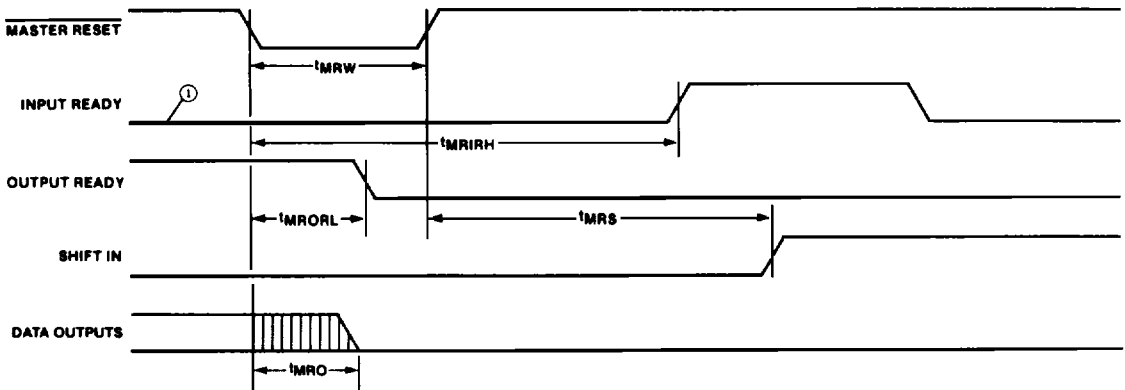
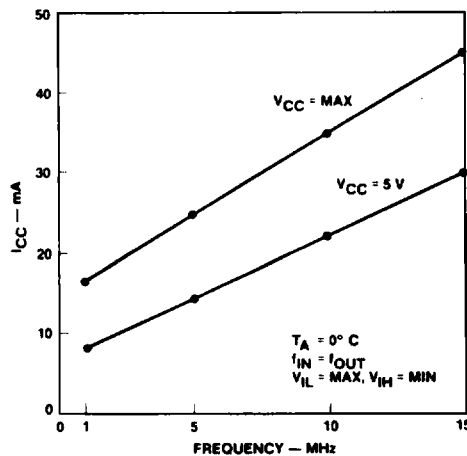


Figure 8. Master Reset Timing

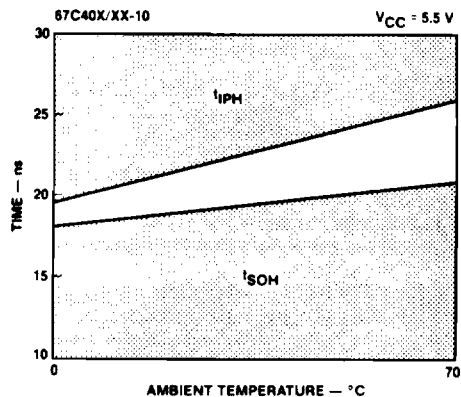
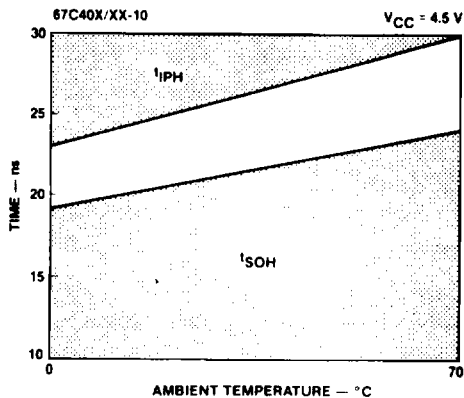
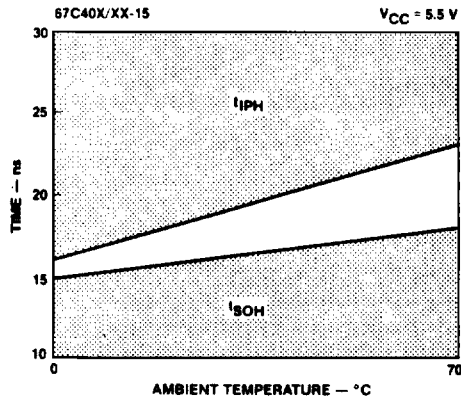
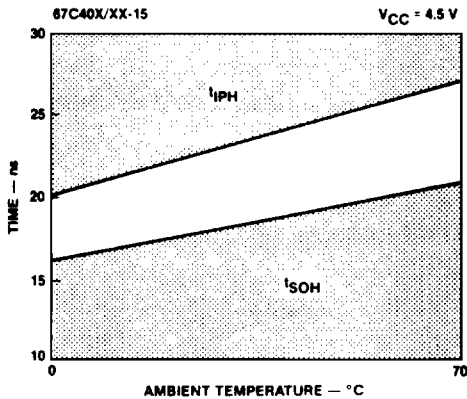
- ① FIFO is initially full

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## ICC vs. Frequency



Guaranteed Distribution of  $t_{1PH}$ ,  $t_{1SOH}$  vs. Temperature (For Cascadability Only)



Guaranteed Distribution of  $t_{0PH}$ ,  $t_{0SH}$  vs. Temperature (For Cascadability Only)

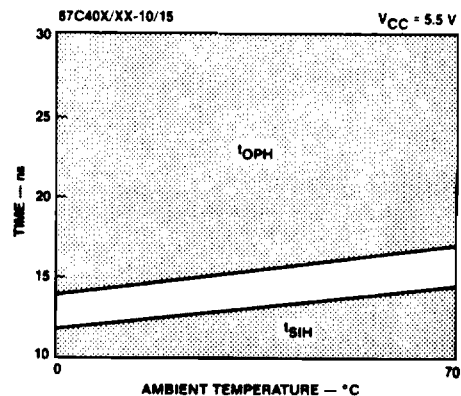
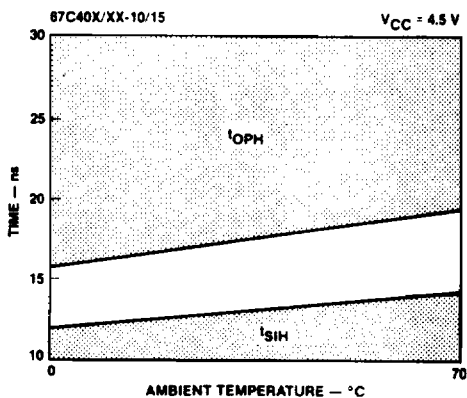


Figure B. Cascadability