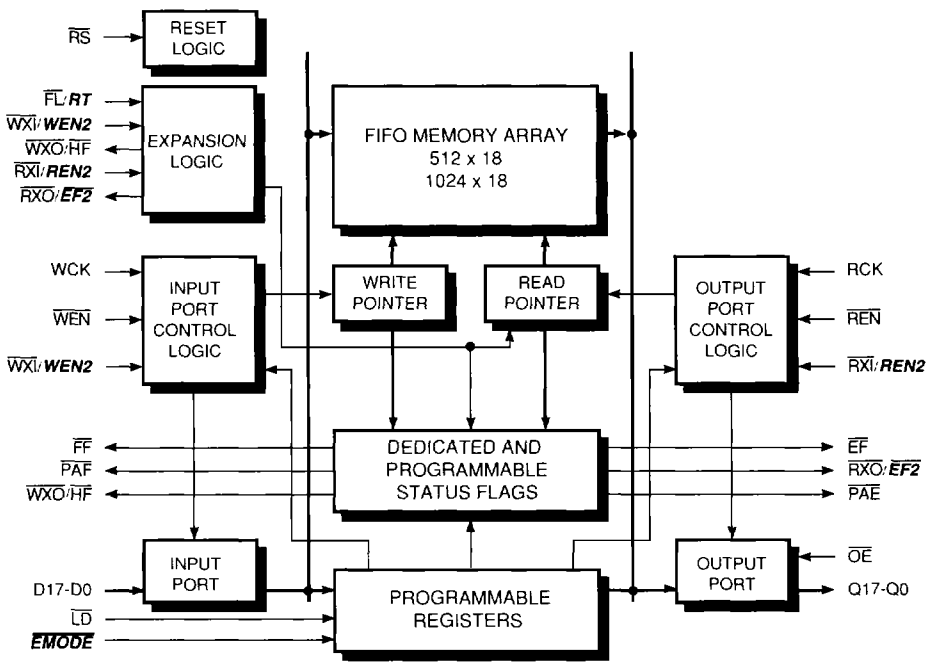
High-Speed CMOS 512 x 18, 1K x 18 Parallel Clocked FIFO

QS72215
QS72225

FEATURES

- CMOS dual-port SRAM technology, 512 x 18 or 1024 x 18
- Fast cycle times: 20/25/35 ns
- Choice of standard or enhanced operating mode
- Device comes up into one of two known default states at reset depending on the state of the ***EMODE*** control input
- I_{OL} = 16 mA, three-state outputs
- Independently synchronized operation of input port and output port
- May be cascaded for increased depth, or paralleled for increased width
- TTL/CMOS-compatible I/O
- Five status flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; Partial flags are programmable
- ***In enhanced operating mode (EMODE), Almost Full, Half-Full, and Almost-Empty flags can be made completely synchronous***
- ***In enhanced operating mode, duplicate enables for interlocked paralleled FIFO operation, for 36-bit data width***
- ***Data retransmit function***
- ***In enhanced operating mode, disabling three-state outputs may be made to suppress reading***
- Pin-compatible drop-in replacements for IDT72215LB/25LB FIFOs
- Space-saving 68-pin PLCC and 64-pin TQFP packages

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION

The QS72215/25 are FIFO (first-in, first-out) memory devices, based on fully static CMOS dual-port SRAM technology, capable of containing up to 512 or 1024 18-bit words, respectively. They can replace two or more byte-wide FIFOs in many applications for microprocessor-to-microprocessor or microprocessor-to-bus communication. Their architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports, respectively. However, these "clocks" also may be asynchronous signals. Almost all control input signals and status-output signals are synchronized to these clocks to simplify system design.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either totally full or totally empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flag offsets are programmable over the entire FIFO depth; but, during a reset operation, each of these is initialized to a default offset value of 63 (QS72215) or 127 (QS72225) FIFO-memory words, from the respective FIFO boundary. If this default offset value is satisfactory, no further programming is required.

After a reset operation during which the ***$\overline{EMODE}$*** control input was not asserted (was HIGH), these FIFOs operate in the standard operating mode. In this mode, each part is pin-compatible and functionally compatible with the IDT72215/25 part of similar depth and speed grade; and the ***control register*** is not even accessible or visible to the external-system logic, which is controlling the FIFO, although it still performs the same control functions.

However, assertion of the $\overline{EMODE}$ control input during a reset operation leaves control register bits 00-05 set, and causes the FIFO to operate in the enhanced operating mode. In essence, asserting $\overline{EMODE}$ chooses a different default state for the control register. The system optionally then may program the control register in any desired manner to activate or deactivate any or all of the enhanced operating mode features which it can control, including selectable-clock-edge flag synchronization and read inhibition when the data outputs are disabled.

Whenever $\overline{EMODE}$ is being asserted, interlocked operation paralleling also is available, by appropriate interconnection of the FIFO's expansion inputs.

The retransmit facility is available during standalone operation, in either standard operating mode or ***an enhanced operating mode*** (see Tables 1 and 2). It is inoperative if the $\overline{FL}$/RT input signal is grounded. It is not an IDT72215/25 feature. ***The retransmit control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer address may be read out repeatedly, an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may wrap around during this entire process, and that the retransmit facility is not available during depth-cascaded operation, either in standard operating mode or in enhanced operating mode (See Tables 1 and 2). Also, the flags behave differently for a short time after a retransmit operation. Otherwise, the retransmit facility is available during standalone operation, in either standard or enhanced operating mode.***

Programming the programmable-flag offsets, ***the timing synchronization of the various status flags, the optional read-suppression functionality of $\overline{OE}$,*** and the behavior of the pointers which access the offset-value registers and ***the control register*** may be individually controlled by asserting the signal $\overline{LD}$ without any reset operation. When $\overline{LD}$ is being asserted, and writing is being enabled by asserting $\overline{WEN}$, some portion of the input bus word D17-D0 is used at the next rising edge of WCLK to program one or more of the programmable registers on successive write clocks. Likewise, the values programmed into these programmable registers may be read out for verification by asserting $\overline{LD}$ and $\overline{REN}$, with the outputs Q17-Q0 enabled. Reading out these programmable registers should not be initiated while they are being written into. Table 3 defines the possible modes of operation for loading and reading out the contents of programmable registers.

In the enhanced operating mode, coordinated operation of two 18-bit FIFOs as one 36-bit FIFO may be ensured by interlocked cross coupling of the status flag outputs from one FIFO to the expansion inputs of the other one: that is, $\overline{FF}$ to $\overline{WXI}$/WEN2 and $\overline{EF}$ to $\overline{RXI}$/REN2, in both directions between two parallel FIFOs. This "interlocked" operation takes effect automatically if two paralleled FIFOs are cross connected in this manner, with the $\overline{EMODE}$ control input being asserted (LOW) (See Tables 1 and 2, also Figures 27 and 30). Standard operating mode depth cascading no longer is available when operating in this "interlocked-paralleled" mode; however, pipelined depth cascading remains available.

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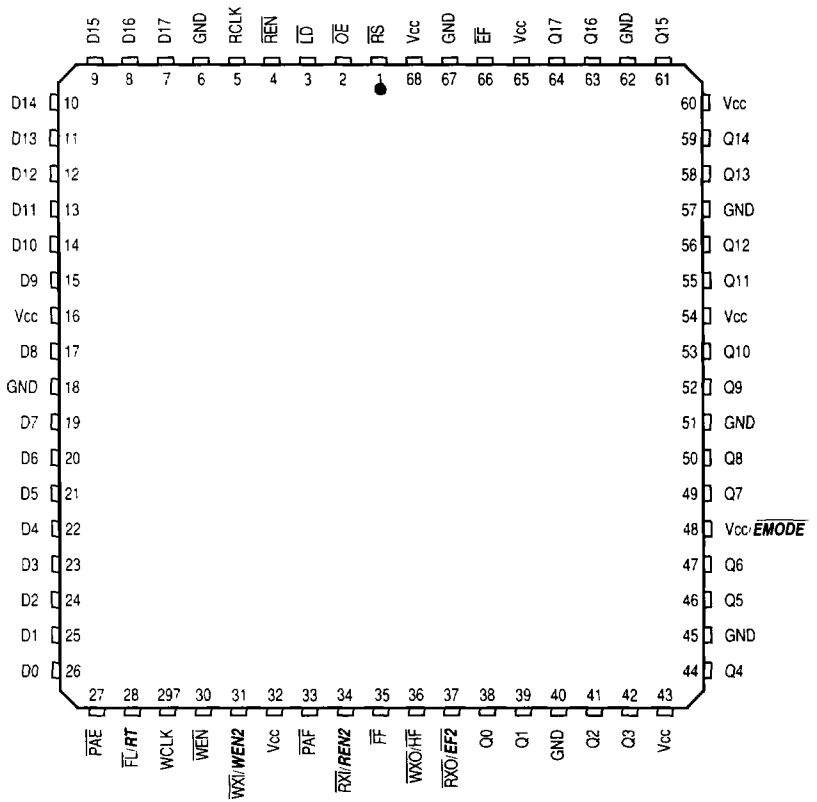
FIGURE 2. 68-PIN PLCC PACKAGE DESCRIPTIONS

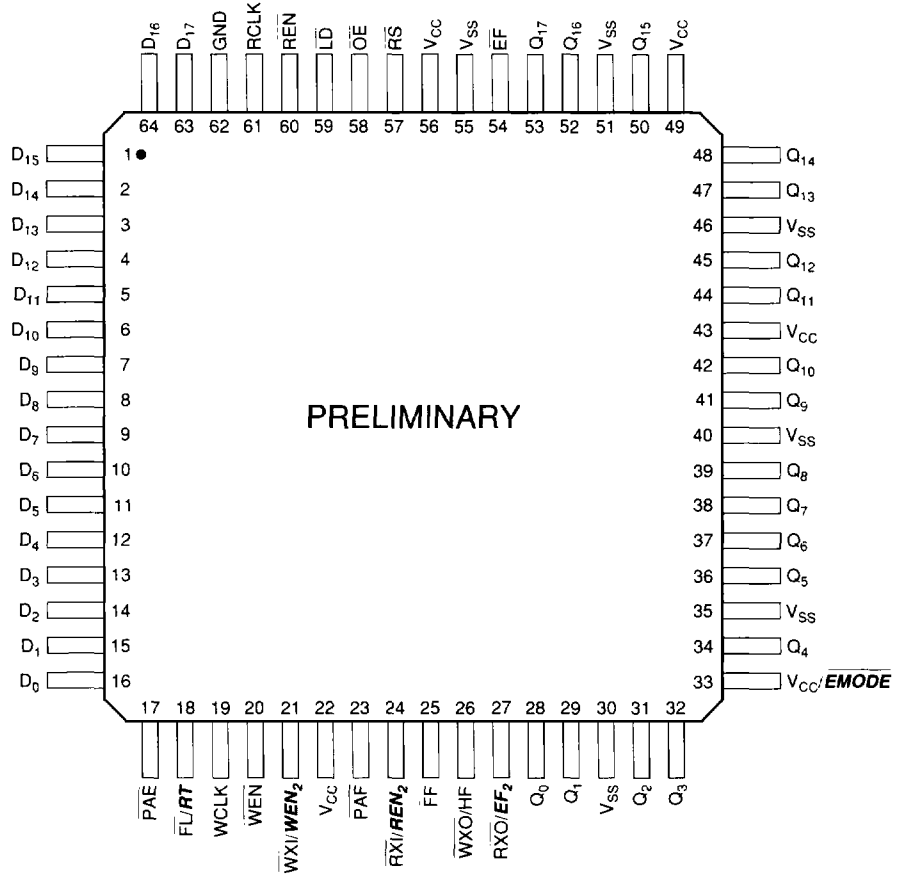


Name	I/O	Function
D17-D0	I	Data Inputs
$\overline{RS}$	I	Reset
$\overline{EMODE}$	I	***Enhanced Operating Mode***
WCLK	I	Write Clock
$\overline{WEN}$	I	Write Enable
RCLK	I	Read Clock
$\overline{REN}$	I	Read Enable
$\overline{OE}$	I	Output Enable
$\overline{LD}$	I	Load
$\overline{FL}$/***RT***	I	First Load/***Retransmit***
$\overline{WXI}$/***WEN2***	I	Write Expansion Input/ ***Write Enable 2***

Name	I/O	Function
$\overline{RXI}$/***REN2***	I	Read Expansion Input/ ***Read Enable 2***
$\overline{FF}$	O	Full Flag
$\overline{PAF}$	O	Programmable Almost-Full Flag
$\overline{WXO}$/$\overline{HF}$	O	Write Expansion Output/Half-Full Flag
$\overline{EF}$	O	Empty Flag
$\overline{PAE}$	O	Programmable Almost-Empty Flag
$\overline{RXO}$/***$\overline{EF2}$***	O	Read Expansion Output/***Empty Flag 2***
Q17-Q0	O	Data Outputs
Vcc		Power
Vss		Ground

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 3. 64-PIN TQFP PACKAGE DESCRIPTIONS



BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

PIN DESCRIPTIONS

Name	I/O[1]	Function	Description
D17-D0	I	Data Inputs	Data inputs from an 18-bit bus.
$\overline{RS}$	I	Reset	When $\overline{RS}$ is taken LOW, the FIFO's internal read and write pointers are set to address the first physical location of the RAM array; $\overline{FF}$, $\overline{PAF}$, and $\overline{HF}$ go HIGH; and $\overline{PAE}$ and $\overline{EF}$ go LOW. The programmable-flag-offset registers ***and the control register*** are set to their default values. (But see the description of ***$\overline{EMODE}$*** below.) A reset is required before initial read or write operation after power-up.
$\overline{EMODE}$	***I***	***Enhanced Operating Mode***	***When $\overline{EMODE}$ is tied LOW, the default setting for control register bits 00-05 after a reset operation changes to HIGH rather than LOW, thus enabling all control-register-controllable enhanced operating mode features, and allowing access to the control register for reprogramming or readback. (See Tables 1, 2, and 5.) If this behavior is desired, $\overline{EMODE}$ may be grounded; however, control-register bits 00-05 still may be individually programmed to selectively enable or disable certain of the enhanced mode features, even though those features associated with interlocked-paralleled operation always are enabled whenever $\overline{EMODE}$ is being asserted (see Table 2). Alternatively, $\overline{EMODE}$ may be tied to Vcc, so that the FIFO is functionally compatible, and the control register is not accessible or visible, and all of its bits remain LOW. Controlling $\overline{EMODE}$ dynamically during system operation is not recommended.***
WCLK	I	Write Clock	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ (write enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a programmable register rather than the internal FIFO memory is written into. ***In the enhanced operating mode, WEN2 is ANDed with $\overline{WEN}$ to produce an effective internal write-enable signal.***[2]
$\overline{WEN}$	I	Write Enable	When $\overline{WEN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO internal memory continues to hold the previous data (see Table 3). Data will not be written into the FIFO if $\overline{FF}$ is LOW. ***In the enhanced operating mode, WEN2 is ANDed with $\overline{WEN}$ to produce an effective internal write-enable signal.***[2]
RCLK	I	Read Clock	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK whenever $\overline{REN}$ (read enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a programmable register rather than the internal FIFO memory is read from. ***In the enhanced operating mode, REN2 is ANDed with $\overline{REN}$ (and whenever control register bit 05 is HIGH, also with $\overline{OE}$) to produce an effective internal read-enable signal.***[2]

(Continued)

Notes:
1 I = input, O = output, Z = high-impedance, V = power voltage level.
2 The ostensible differences in signal assertiveness are reconciled before ANDing.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

PIN DESCRIPTIONS *(Continued)*

Name	I/O[1]	Function	Description
$\overline{REN}$	I	Read Enable	When $\overline{REN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, and/or also when $\overline{EF}$ is LOW, the FIFO's output register continues to hold the previous data word, whether or not Q17-Q0 (the data outputs) are enabled (see Table 3). ***In the enhanced operating mode, REN2 is ANDed with $\overline{REN}$ (and whenever control register bit 05 is HIGH, also with $\overline{OE}$) to produce an effective internal read-enable signal.***[2]
$\overline{OE}$	I	Output Enable	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in a high-Z (high-impedance) state. ***In the enhanced operating mode, $\overline{OE}$ not only continues to control the outputs in this same manner, but also can function as an additional ANDing input to the combined effective read-enable signal, along with $\overline{REN}$ and REN2, whenever control register bit 05 is HIGH (see Table 5).***[2]
$\overline{LD}$	I	Load	When $\overline{LD}$ is LOW, the data word on D17-D0 (the data inputs) is written into a programmable-flag-offset register, ***or into the control register (when in the enhanced operating mode)***, on the LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ is LOW (see Table 3). Also, when $\overline{LD}$ is LOW, a word is read to Q17-Q0 (the data outputs) from the offset registers ***and/or the control register (when in the enhanced operating mode)***, on the LOW-to-HIGH transition of RCLK, whenever $\overline{REN}$ is LOW. (See again Table 3, and particularly the Notes following this table.) When $\overline{LD}$ is HIGH, normal FIFO write and read operations are enabled.
$\overline{FL}$/***RT***	I	First Load/ ***Retransmit***	In the standalone or paralleled configuration, $\overline{FL}$ /***RT*** should be LOW during a reset operation (see Tables 1 and 2). ***However, thereafter, in the standalone or paralleled configuration, if $\overline{FL}$ is taken HIGH, it functions instead as RT (retransmit), and resets the FIFO's internal read pointer to the first physical location of the RAM array. Note that although retransmit is an 'enhanced' feature, it is always available for a FIFO during standalone operation, whether the FIFO is in standard operating mode or in enhanced operating mode; it is not regulated by the control register or by $\overline{EMODE}$ control input.*** In standard operating mode cascaded configurations, $\overline{FL}$ has an entirely different function: it is grounded for the first FIFO device (the "master" device or the "first-load" device), and is set to HIGH for all other FIFO devices in the daisy chain. Thus, the ***retransmit*** feature is not available for FIFOs operating in a standard operating mode cascaded configuration.

(Continued)

Notes:
1. I = input, O = output, Z = high-impedance. V = power voltage level.
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BOLD ITALIC = ENHANCED OPERATING MODE
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PIN DESCRIPTIONS *(Continued)*

Name	I/O[1]	Function	Description
$\overline{WXI}$/ ***WEN2***	I	Write Expansion Input/***Write Enable 2***	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the three other control inputs $\overline{RXI}$/***REN2***, $\overline{FL}$/***RT***, and $\overline{EMODE}$ (see Tables 1 and 2). In the standalone or paralleled configuration, $\overline{WXI}$/***WEN2*** is grounded. In the cascaded configuration, $\overline{WXI}$/***WEN2*** is connected to $\overline{WXO}$ (write expansion output) of the previous device, and functions as $\overline{WXI}$. ***In the enhanced operating mode, $\overline{WXI}$/WEN2 functions as a second write-enable signal, WEN2, which is ANDed with WEN to produce an effective internal write-enable signal.***[2]
$\overline{RXI}$/ ***REN2***	I	Read Expansion Input/***Read Enable 2***	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the three other control inputs $\overline{WXI}$/***WEN2***, $\overline{FL}$/***RT***, and $\overline{EMODE}$. ***(see Tables 1 and 2).*** In the standalone or paralleled configuration, $\overline{RXI}$/***REN2*** is grounded. In the cascaded configuration, $\overline{RXI}$/***REN2*** is connected to $\overline{RXO}$ (read expansion output) of the previous device, and functions as $\overline{RXI}$. ***In the enhanced operating mode, $\overline{REN}$/REN2 functions as a second read-enable signal, REN2, which is ANDed with $\overline{REN}$ — and perhaps also with $\overline{OE}$, if control-register bit 05 is HIGH — to produce an effective internal read-enable signal.***[2]
$\overline{FF}$	O	Full Flag	When $\overline{FF}$ is LOW, the FIFO is full; further advancement of its internal write-address pointer and further data writes through its data inputs into its internal memory array are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAF}$	O	Programmable Almost-Full Flag	When $\overline{PAF}$ is LOW, the FIFO is "almost-full", based on the almost-full-offset value programmed into the FIFO's almost-full offset register. The default value of this offset at reset is one-eighth of the total number of words in the FIFO-memory array, minus one, measured from "full" (see Table 4). In the standard operating mode, $\overline{PAF}$ is asynchronous. ***In the enhanced operating mode, $\overline{PAF}$ is synchronized to WCLK after a reset operation, according to the state of control register bit 04 (see Table 5).***
$\overline{EF}$	O	Empty Flag	When $\overline{EF}$ is LOW, the FIFO is empty; further advancement of its internal read-address pointer and further readout of data words from its internal memory array to its data outputs, are inhibited. When the $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ synchronized to RCLK.

(Continued)

Notes:
1. I = input, O = output, Z = high-impedance, V = power voltage level.
2. The ostensible differences in signal assertiveness are reconciled before ANDing.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

PIN DESCRIPTIONS *(Continued)*

Name	I/O[1]	Function	Description
$\overline{PAE}$	O	Programmable Almost-Empty Flag	When $\overline{PAE}$ is LOW, the FIFO is "almost empty," based on the almost-empty-offset value programmed into the FIFO's almost-empty offset register. The default value of this offset at reset is one-eighth of the total number of words in the FIFO-memory array, minus one, measured from "empty" (see Table 4). In the standard operating mode, $\overline{PAE}$ is asynchronous. ***In the Enhanced Operating Mode, $\overline{PAE}$ is synchronized to RCLK after a reset operation, according to the state of control register bit 01. (See Table 5.)***
$\overline{WXO}$/ $\overline{HF}$	O	Write Expansion Output/ Half-Full Flag	This signal is dual-purpose: its functionality is determined during a reset operation, according to the states of the two control inputs $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** (see Tables 1 and 2). In the standalone or paralleled configuration, whenever $\overline{HF}$ is LOW, the device is more than half-full. In the standard operating mode, $\overline{HF}$ is asynchronous. ***In the enhanced operating mode, $\overline{HF}$ may be synchronized to WCLK or to RCLK after a reset operation, according to the state of control register bits 02 and 03 (see Table 5).*** In the standard operating mode cascaded configuration, a pulse is sent from $\overline{WXO}$ to the $\overline{WXI}$ input of the next FIFO in the daisy-chain cascade whenever the last location in the FIFO is written.
$\overline{RXO}$/ ***EF2***	O	Read Expansion Output	This signal is dual-purpose; its functionality is determined by the state of the $\overline{EMODE}$ control input during a reset operation (see Tables 1 and 2). In the standard operating mode, in a cascaded configuration, a pulse is sent from $\overline{RXO}$ to the $\overline{RXI}$ input of the next FIFO in the daisy-chain cascade, whenever the last location of the FIFO is read. ***In the enhanced operating mode, whenever $\overline{EMODE}$ is being asserted (LOW), $\overline{EF2}$ behaves as an exact duplicate of $\overline{EF}$, but delayed by one full cycle of RCLK with respect to $\overline{EF}$.***
Q17-Q0	O/Z	Data Outputs	Data outputs to an 18-bit Bus.
Vcc	V	Power	+5V power supply pins.
Vss	V	Ground	0V ground pins.

Notes:
1. I = input, O = output, Z = high-impedance, V = power voltage level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to GND Potential	−0.5V to +7.0V
Signal Pin Voltage to GND Potential	−0.5V to Vcc + 0.5V
DC Output Current Max Sink Current/Pin[1]	±75 mA
Maximum Power Dissipation	2.0 W
Temperature Range with Power Applied[2]	−55° to +125°C
TSTG Storage Temperature Range	−65° to +155°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional- or reliability-type failures.

Notes:
1. Only one output may be shorted at a time, for a period not exceeding 30 seconds.
2. Measured with clocks idle.

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CAPACITANCE

T_A = 25°C, f = 1.0 MHz

Name	Description[1]	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	—	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	pF

Notes:
1. Capacitance is guaranteed but not tested.

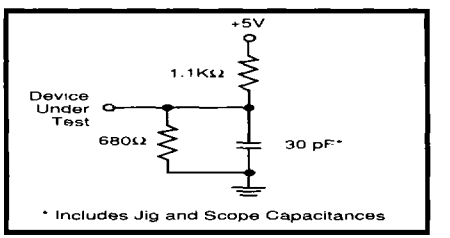
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	Vcc + 0.5	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –12.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 16.0 mA	—	0.4	V
I_{LO}	I/O Leakage	0V ≤ V_{OUT} ≤ Vcc, $\overline{OE}$ ≥ V_{IH}	–10	+10	µA
I_{IL}	Input Leakage	Vcc = 5.5V, V_{IN} = 0V to Vcc	–10	+10	µA

AC TEST CONDITIONS

Input Pulse Levels	GND to 3V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load R_1 (Top Resistor)	1.1k Ω
Output Load R_2 (Bottom Resistor)	680 Ω
Output Load C_L (Load Capacitance)	30 pF

FIGURE 4. OUTPUT LOAD CIRCUIT



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{CC}	Operating Current [1] Vcc = Max., I_{OUT} = 0 mA	—	190	mA
I_{CC2}	Standby Current All Inputs = V_{IHMIN} (Clocks Idle)	—	25	mA
I_{CC3}	Power Down Current All Inputs at Vcc – 0.2V (Clocks Idle)	—	1	mA

Note:
1 Output load is disconnected.

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AC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Speed (ns)						Units
		-20		-25		-35		
		Min	Max	Min	Max	Min	Max	
f_{CC}	Clock Cycle Frequency	—	50	—	40	—	28.6	MHz
t_A	Data Access Time	2	12	3	15	3	20	ns
t_{CLK}	Clock Cycle Time	20	—	25	—	35	—	ns
t_{CLKH}	Clock HIGH Time	8	—	10	—	14	—	ns
t_{CLKL}	Clock LOW Time	8	—	10	—	14	—	ns
t_{DS}	Data Setup Time	5	—	6	—	7	—	ns
t_{DH}	Data Hold Time	1	—	1	—	2	—	ns
t_{ENS}	Enable Setup Time	5	—	6	—	7	—	ns
t_{ENH}	Enable Hold Time	1	—	1	—	2	—	ns
t_{RS}	Reset Pulse Width[1]	20	—	25	—	35	—	ns
t_{RSS}	Reset Setup Time[2]	12	—	15	—	20	—	ns
t_{RSR}	Rest Recovery Time[2]	12	—	15	—	20	—	ns
t_{RSF}	Reset to Flag and Output Time	—	30	—	35	—	40	ns
t_{OE}	Output Enable to Output Valid	—	9	—	12	—	15	ns
t_{OLZ}	Output Enable to Output LOW-Z[2]	0	—	0	—	0	—	ns
t_{OHZ}	Output Enable to Output HIGH-Z[2]	1	9	1	12	1	15	ns
t_{WFF}	Write Clock to Full Flag	—	12	—	15	—	20	ns
t_{REF}	Read Clock to Empty Flag	—	12	—	15	—	20	ns
t_{PAF}	Clock to Programmable Almost-Full Flag (Standard Operating Mode)	—	14	—	17	—	23	ns
t_{PAE}	Clock to Programmable Almost-Empty Flag (Standard Operating Mode)	—	14	—	17	—	23	ns
t_{HF}	Clock to Half-Full Flag (Standard Operating Mode)	—	14	—	17	—	23	ns
t_{PAFS}	***Clock to Programmable Almost-Full Flag (Enhanced Operating Mode)***	—	***14***	—	***17***	—	***23***	***ns***
t_{PAES}	***Clock to Programmable Almost-Empty Flag (Enhanced Operating Mode)***	—	***14***	—	***17***	—	***23***	***ns***
t_{HFS}	***Clock to Half-Full Flag (Enhanced Operating Mode)***	—	***14***	—	***17***	—	***23***	***ns***
t_{XO}	Clock to Expansion-Out	—	12	—	15	—	20	ns
t_{XI}	Expansion-In Pulse Width	7	—	9	—	13	—	ns
t_{XIS}	Expansion-In Setup Time	7	—	9	—	14	—	ns
t_{SKEW1}	Skew Time between Read Clock and Read Clock for Full Flag[3]	9	—	11	—	16	—	ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag[4]	9	—	11	—	16	—	ns

Notes:
1. Pulse widths less than the stated minimum values may cause incorrect operation.
2. Values are generated by design, not currently tested.
3. These times also apply to the Programmable-Almost-Full and Half-Full flags when they are synchronized to WCLK.
4. These times also apply to the Half-Full and Programmable-Almost-Empty flags when they are synchronized to RCLK.

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SIGNAL AND OPERATING SEQUENCE DESCRIPTION

TABLE 1. GROUPING-MODE DETERMINATION DURING A RESET OPERATION

$\overline{EMODE}$	$\overline{WXI}$/WEN2	$\overline{RXI}$/REN2	$\overline{FL}$/RT	MODE	$\overline{WXO}$/ $\overline{HF}$ USAGE	$\overline{WXI}$/ *WEN2* USAGE	$\overline{RXI}$/ *REN2* USAGE	$\overline{FL}$/ *RT* USAGE	$\overline{RXO}$/ *EF2* USAGE
H[1]	H	H	H	Cascaded Slave[2]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$	$\overline{RXO}$
H[1]	H	H	L	Cascaded Master[2]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$	$\overline{RXO}$
H	H	L	X	(Reserved)	—	—	—	—	—
H	L	H	X	(Reserved)	—	—	—	—	—
H	L	L	H[3]	(Not Allowed)	(HF)	(none)	(none)	(***RT***)	(none)
H	L	L	L[3]	Standalone	HF	(none)	(none)	***RT***	(none)
L	***X***	***X***	***H***[3]	***(Not Allowed During Reset)***	***($\overline{HF}$)***	***(WEN2)***	***(REN2)***	***(RT)***	***($\overline{EF2}$)***
L	***X***	***X***	***L***[3]	***Interlocked Paralleled***[4]	***$\overline{HF}$***	***WEN2***	***REN2***	***RT***	***$\overline{EF2}$***

Notes:

1. A reset operation forces $\overline{WXO}$/$\overline{HF}$ and $\overline{RXO}$/***EF2*** HIGH for the nth FIFO, thus forcing $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** HIGH for the (n + 1)st FIFO.
2. The terms "master" and "slave" refer to the standard operating mode cascading. In pipeline cascading[3], there is no such distinction.
3. ***Once grouping mode has been determined during a reset operation, $\overline{FL}$/RT then may go HIGH to achieve a retransmit operation.***
4. ***$\overline{EMODE}$ must be asserted for access to the control register to be enabled. Also, FIFOs being used in pipelined-cascading configurations should be in interlocked paralleled mode.***
5. Setup time and recovery time specifications apply during a reset operation.
6. H = HIGH, L = LOW, X = don't care.

TABLE 2. EXPANSION-PIN USAGE ACCORDING TO GROUPING-MODE

		standard operating mode			*Enhanced Operating Mode*
I/O	Pin	Depth-Cascaded Master	Depth-Cascaded Slave	Standalone	*Interlocked Paralleled*
I	$\overline{WXI}$/***WEN2***	From $\overline{WXO}$ ([n – 1]st FIFO)	From $\overline{WXO}$ ([n – 1]st FIFO)	Grounded	***From $\overline{FF}$ (other FIFO)***
O	$\overline{WXO}$/$\overline{HF}$	To $\overline{WXI}$ ([n + 1]st FIFO)	To $\overline{WXI}$ ([n + 1]st FIFO)	Becomes $\overline{HF}$	***Becomes $\overline{HF}$***
I	$\overline{RXI}$/***REN2***	From $\overline{RXO}$ ([n – 1]st FIFO)	From $\overline{RXO}$ ([n – 1]st FIFO)	Grounded	***From $\overline{EF}$ (other FIFO)***
O	$\overline{RXO}$/***$\overline{EF2}$***	To $\overline{RXI}$ ([n + 1]st FIFO)	To $\overline{RXI}$ ([n + 1]st FIFO)	Unused	***Becomes $\overline{EF2}$***
I	$\overline{FL}$/***RT***	Grounded (Logic LOW)	Logic HIGH	Becomes RT[1]	***Becomes RT***[1]

Note:

1. $\overline{FL}$/***RT*** may be grounded if ***the retransmit facility*** is not being used.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

TABLE 3. SELECTION OF READ AND WRITE OPERATIONS

$\overline{LD}$	$\overline{WEN}$[3,4]	$\overline{REN}$[3,4]	WCLK	RCLK	Action
L	X	X	—	—	No operation.
L	L	H	↑	—	Write to a programmable register[1].
L	H	H	↑	—	Hold present value of programmable-register write counter, and do not write[2].
L	H	L	—	↑	Read from a programmable register[1].
L	H	H	—	↑	Hold present value of programmable-register read counter, and do not read[2].
L	X	X	↑	↑	Illegal combination, which will cause errors.
H	L	X	↑	X	Normal FIFO write operation.
H	X	L	X	↑	Normal FIFO read operation.
H	L	X	—	X	No write operation.
H	H	X	X	X	No write operation.
H	X	L	X	—	No read operation.
H	X	H	X	X	No read operation.
H	L	L	—	—	No operation.
H	H	H	X	X	No operation.

Key:
H = Logic HIGH, L = Logic LOW, X = Dont Care (Logic HIGH, Logic LOW, or any transition), ↑ = A LOW-to-HIGH transition; — = Any condition EXCEPT a LOW-to-HIGH transition.

Notes:

1. The selection of a programmable register to be written or read is controlled by two simple state machines. One state machine controls the selection for writing; the other state machine controls the selection for reading. These two state machines operate independently of each other. Both state machines are reset to point to word 0 by a reset operation. ***In the enhanced operating mode, if control register bit 00 is set, both state machines are also rest to point to word 0 bit de-assertion of $\overline{LD}$ after $\overline{LD}$ has been asserted (that is, by a rising edge of $\overline{LD}$), followed by a valid memory array write cycle for the writing-control state machine and/or by a valid memory-array read cycle for the reading-control state machine.***
2. The order of the two programmable registers which are accessible in standard operating mode, as selected by either state machine, is always:

   Word 0: Almost-empty offset register
   Word 1: Almost-full offset register
   Word 0: Almost-empty offset register
   ...
   (Repeats Indefinitely)
   ...

   The order of the three programmable registers which are accessible in enhanced operating mode, as selected by either state machine, is always:

   Word 0: Almost-empty offset register
   Word 1: Almost-full offset register
   Word 2: Control register
   Word 0: Almost-empty offset register
   ...
   (Repeats Indefinitely)
   ...

   Note that, in the standard operating mode, word 2 is not accessed, and words 0 and 1 alternate.
3. After normal FIFO operation has begun, writing new contents into either of the two offset registers should only be done when the FIFO is empty.
4. ***$\overline{WEN2}$, $\overline{REN2}$, and $\overline{OE}$ may be ANDed terms in the enabling of read and write operations, according to the state of the $\overline{EMODE}$ control input and of control register bit 05.***

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

TABLE 4. STATUS FLAGS

Number of Unread Data Words Present within FIFO[1,2]		Full Flag	Middle Flags			Empty Flags
512 x 18 FIFO	**1024 x 18 FIFO**	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	H	L	L
1 to q	1 to q	H	H	H	L	H
(q + 1) to 256	(q + 1) to 512	H	H	H	H	H
257 to [512 – (p + 1)]	513 to [1024 – (p + 1)]	H	H	L	H	H
(512 – p) to 511	(1024 – p) to 1023	H	L	L	H	H
512	1024	L	L	L	H	H

Notes:
1. q = Programmable-almost-empty offset values. (Default values: 512 x 18, q = 63; 1024 x 18, q = 127.)
2. p = Programmable-almost-full offset values. (Default values: 512 x 18, p = 63; 1024 x 18, p = 127.)
3. Only 9 (512 x 18) or 10 (1024 x 18) of the 12 offset-value-register bits should be programmed. The unneeded most-significant-end bits should be LOW (zero).
4. The flag output is delayed by one full clock cycle in enhanced operating mode, when synchronous operation is specified for intermediate flags.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

TABLE 5. CONTROL-REGISTER FORMAT

Command Register Bits	Code	Value after Reset EMODE = H	Value after Reset EMODE = L	Flag Affected, If Any	Description	Notes
00	L	L	H	—	De-assertion of $\overline{LD}$ does not reset the programmable-register write pointer and read pointer.	Standard Addressing of programmable registers.
00	H	L	H	—	De-assertion of $\overline{LD}$ resets the programmable-register write pointer and read pointer to address word 0, the programmable-almost-empty-flag-offset register. The change takes effect after a valid write operation or a valid read operation, respectively.	Non-ambiguous addressing of programmable registers.
01	L	L	H	$\overline{PAE}$	Set by ↑RCLK, reset by ↑WCLK.	Asynchronous flag clocking.
01	H	L	H	$\overline{PAE}$	Set and reset by ↑RCLK.	Synchronous flag clocking
02, 03	LL	LL	HH	$\overline{HF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
02, 03	LH	LL	HH	$\overline{HF}$	Set and reset by ↑RCLK.	Synchronous flag clocking at output port.
02, 03	HL,HH	LL	HH	$\overline{HF}$	Set and reset by ↑WCLK.	Synchronous flag clocking at input port.
04	L	L	H	$\overline{PAF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
04	H	L	H	$\overline{PAF}$	Set and reset by ↑WCLK.	Synchronous flag clocking.
05	L	L	H	—	OE has no effect on an internal operation, apart from disabling the outputs.	Allows the read-address pointer to advance even when Q17-Q0 are not driving the output bus.
05	H	L	H	—	$\overline{OE}$ inhibits a read operation whenever the data outputs Q17-Q0 are in the HIGH-Z state.	Inhibits the read-address pointer from advancing when Q17-Q0 are not driving the bus; thus, guards against data loss.
06	L	L	L	—	Reserved.	Future use to control depth cascading and interlocked paralleling.
06	H	L	L	—	Reserved.	
07-11	LLLLL	LLLLL	LLLLL	—	Reserved.	Reserved.

Notes:
1. When $\overline{EMODE}$ is HIGH, and ***control register bits 00-05 are LOW***, the FIFO behaves in a manner functionally equivalent to the IDT72215LB/25LB FIFO of similar depth and speed grade. Under these conditions, the ***control register*** is not visible or accessible to the external system which includes the FIFO.
2. If $\overline{EMODE}$ is not asserted (is HIGH), ***control register bits 00-05 remain LOW*** after a reset operation. ***However, if $\overline{EMODE}$ is asserted (is LOW) during a reset operation, control register bits 00-05 are forced HIGH, and remain HIGH until changed. Control register bits 06-11 are unaffected by $\overline{EMODE}$.***

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES

Data Inputs

DATA IN (D17-D0)

Data, programmable flag-offset values, and ***control register*** codes are input to the FIFO as 18-bit words on D17-D0. Unused bit positions in offset-value and ***control register*** words should be zero-filled.

Control Inputs

RESET ($\overline{RS}$)

The FIFO is reset whenever the asynchronous reset ($\overline{RS}$) input is taken to a LOW state. A reset operation is required after power-up, before the first write operation may occur. The state of the FIFO is fully defined after a reset operation. If the default values which are entered into the programmable flag-offset-value registers ***and the control register*** by a reset operation are acceptable, then no device programming is required. A reset operation initializes the FIFO's internal read-address and write-address pointers to the FIFO's first physical memory location. The five status flags, $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$ are updated to indicate that the FIFO is completely empty; thus, the first three of these are reset to HIGH, and the last two are reset to LOW. The flag-offset values for $\overline{PAF}$ and $\overline{PAE}$ each are initialized to one-eighth of the depth of a single FIFO, minus one; 63 for a 512-word FIFO, and 127 for a 102-word FIFO. If ***$\overline{EMODE}$*** is not being asserted (i.e., if ***$\overline{EMODE}$*** is HIGH), all the ***control register*** bits are initialized to configure the FIFO to operate in the standard operating mode. Until a write operation occurs, the data outputs D17-D0 all are LOW whenever $\overline{OE}$ is LOW.

ENHANCED OPERATING MODE ($\overline{EMODE}$)

Whenever $\overline{EMODE}$ is asserted during a reset operation, control register bits 00-05 remain HIGH rather than LOW after the completion of the reset operation. Thus, $\overline{EMODE}$ has the effect of activating enhanced-operating-mode features during a reset operation. Subsequently, they may be individually disabled or re-enabled by changing the setting of control register bits. The behavior of these enhanced-operating-mode features is described in Table 5. For permanent enhanced-operating-mode operation, $\overline{EMODE}$ must be grounded; dynamic control of $\overline{EMODE}$ during system operation is not recommended.

Asserting $\overline{EMODE}$ during a reset operation also causes $\overline{WXI}$/WEN2 to be configured as WEN2, and $\overline{RXI}$/REN2 to be configured as REN2, to support interlocked-paralleled operation of two FIFOs "side by side" (see Figure 27).

WRITE CLOCK (WCLK)

A rising edge (LOW-to-HIGH transition) of WCLK initiates a FIFO write cycle if $\overline{LD}$ is HIGH or a programmable-register write cycle if $\overline{LD}$ is LOW. The 18 data inputs, and all input-side synchronous control inputs, must meet setup and hold times with respect to the rising edge of WCLK. The input-side status flags are meaningful after specified time intervals, following a rising edge of WCLK.

Conceptually, the WCLK input receives a free-running, periodic "clock waveform", which is used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the WCLK waveform *must* be periodic. An "asynchronous" mode of operation is in fact possible, if $\overline{WEN}$ is continuously asserted (that is, is continuously held LOW), and WCLK receives aperiodic "clock" pulses of suitable duration. There likewise is no requirement that WCLK must have any particular synchronization relation to the read clock RCLK. These two clock inputs may in fact receive the same "clock" signal, or they may receive totally different signals, which are not synchronized to each other in any way.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

WRITE ENABLE ($\overline{WEN}$)

Whenever $\overline{WEN}$ is being asserted (is LOW) and $\overline{LD}$ is HIGH, and the FIFO is not full, an 18-bit data word is loaded into the effective input register for the memory array at every WCLK rising edge (LOW-to-HIGH transition). Data words are stored into the two-port memory array sequentially, regardless of any ongoing read operation. Whenever $\overline{WEN}$ is not being asserted (is HIGH), the input register retains whatever data word it contained previously, and no new data word gets loaded into the memory array.

To prevent overrunning the internal FIFO boundaries, further write operations are inhibited whenever the Full flag ($\overline{FF}$) is being asserted (is LOW). If a valid read operation then occurs, upon the completion of that read cycle, $\overline{FF}$ again goes HIGH after a time t_{WFF}, and another write operation is allowed to begin whenever WCLK makes another LOW-to-HIGH transition. Effectively, $\overline{WEN}$ is overridden by $\overline{FF}$; thus, during normal FIFO operation, $\overline{WEN}$ has no effect when the FIFO is full.

In the enhanced operating mode, whenever $\overline{EMODE}$ is being asserted (is LOW), $\overline{WXI}$/WEN2 functions as WEN2, an additional duplicate (albeit assertive-HIGH) write-enable input in order to provide an "Interlocking" mechanism for reliable synchronization of two paralleled FIFOs. To control writing, WEN2 is ANDed with $\overline{WEN}$; the logic-AND function ($\overline{WEN}$ • WEN2) then behaves like $\overline{WEN}$ in the foregoing description.

READ CLOCK (RCLK)

A rising edge (LOW-to-HIGH transition) of RCLK initiates a FIFO read cycle if $\overline{LD}$ is HIGH, or a programmable-register read cycle if $\overline{LD}$ is LOW. All output-side synchronous control inputs must meet setup and hold times with respect to the rising edge of RCLK. The 18 data outputs, and the output-side status flags, are meaningful after specified time intervals, following a rising edge of RCLK.

Conceptually, the RCLK input receives a free-running, periodic "clock" waveform, which is used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the RCLK waveform must be periodic. An "asynchronous" mode of operation is in fact possible, if $\overline{REN}$ is continuously asserted (that is, is continuously held LOW), and RCLK receives aperiodic "clock" pulses of suitable duration. There likewise is no requirement that RCLK must have any particular synchronization relation to the write clock WCLK. These two clock inputs may in fact receive the same "clock" signal; or they may receive totally different signals, which are not synchronized to each other in any way.

READ ENABLE ($\overline{REN}$)

Whenever $\overline{REN}$ is being asserted (is LOW), and the FIFO is not empty, an 18-bit data word is loaded into the output register from the memory array at every RCLK rising edge (LOW-to-HIGH transition). Data words are read from the two-port memory array sequentially, regardless of any ongoing write operation. Whenever $\overline{REN}$ is not being asserted (is HIGH), the output register retains whatever data word it contained previously, and no new data word gets loaded into it from the memory array.

To prevent overrunning the internal FIFO boundaries, further read operations are inhibited whenever the Empty flag ($\overline{EF}$) is being asserted (is LOW). If a valid write operation then occurs, upon the completion of that write cycle $\overline{EF}$ again goes HIGH after a time t_{REF}, and another read operation is allowed to begin whenever RCLK makes another LOW-to-HIGH transition. Effectively, $\overline{REN}$ is overridden by $\overline{EF}$; thus, during normal FIFO operation, $\overline{REN}$ has no effect when the FIFO is empty.

In the enhanced operating mode, one (or, sometimes two) additional read-enable inputs may be ANDed with $\overline{REN}$ to control reading, depending on the state of the control register bit 05. The additional read-enable input(s) are REN2 (and $\overline{OE}$).

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

Whenever $\overline{EMODE}$ is being asserted (is LOW) $\overline{RXI}$/REN2 functions as REN2, an additional duplicate (albeit assertive-HIGH) read-enable input, in order to provide an "interlocking" mechanism for reliable synchronization of two paralleled FIFOs.

Also, if control register bit 05 has been set, $\overline{OE}$ takes on the extra role of serving as yet another duplicate read-enable input, in addition to its usual function of controlling the FIFO's data outputs, in order to inhibit further read operations whenever the FIFO's data outputs are disabled, and thereby to prevent data loss under some circumstances.

OUTPUT ENABLE ($\overline{OE}$)

$\overline{OE}$ is an assertive-LOW, asynchronous, output enable. In the standard operating mode, $\overline{OE}$ has only the effect of enabling or disabling the data outputs Q17-Q0. That is, disabling Q17-Q0 does not inhibit a read operation for data being transmitted to the output register; the same data will remain available later, when the outputs are again enabled, unless subsequently overwritten. When Q17-Q0 are enabled, each of these 18 data outputs is in a normal HIGH or LOW state, according to the bit pattern of the data word in the output register. When Q17-Q0 are disabled, each of these outputs is in the HIGH-Z (high-impedance) state.

In the enhanced operating mode, if control register bit 05 has been set, $\overline{OE}$ behaves as an additional read-enable control input, as well as enabling and disabling the data outputs Q17- Q0. Under these circumstances, incrementing the read-address pointer is inhibited whenever Q17-Q0 are in the HIGH-Z state. Thus, "reading" successive words which fail to reach the outputs is prevented, as a safeguard against data loss.

LOAD ($\overline{LD}$)

The QS72215/25 FIFOs contain ***three*** 18-bit programmable registers. The contents of these three registers may be loaded with data from the data inputs D17-D0, or read out onto the data outputs Q17-Q0. The first two registers are the programmable flag-offset value registers, for the Programmable Almost-Empty flag ($\overline{PAE}$) and the Programmable Almost-Full flag ($\overline{PAF}$), respectively. ***The third register is the control register, which includes several configuration-control bits for enhanced-operating-mode features.***

None of these three registers makes use of all of its available 18 bits. Figure 5 shows which bit positions of each register are operational. The two programmable flag-offset-value registers each contain an offset value in bits 0-8 (QS72215) or 0-9 (QS72225); bits 9-17 (QS72215) or 10-17 (QS72225) are unused. The default values for both offsets are one-eighth of the total number of words in the FIFO memory array minus one: 63 for a 512 x 18 FIFO, and 127 for a 1024 x 18 FIFO.

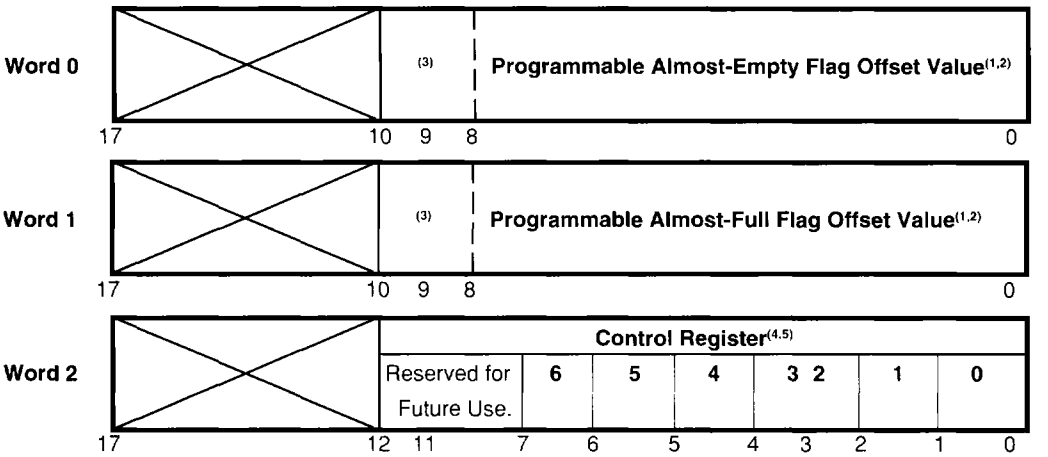
The ***control register*** configuration is shown in Figure 5 and in Table 5. For the ***control register***, in the standard operating mode, with ***$\overline{EMODE}$*** de-asserted (HIGH), the default value for any operational bit which has not been programmed is zero (LOW). ***In the enhanced operating mode, with $\overline{EMODE}$ asserted (LOW), the default value for bits 00-05 is HIGH, and the default value for bits 06-11 is LOW.***

Whenever $\overline{LD}$ and $\overline{WEN}$ are simultaneously being asserted (are both LOW), the 18-bit data word from the data inputs D17-D0 is written into the programmable almost-empty flag-offset-value register at the first rising edge (LOW-to-HIGH transition) of the write clock (WCLK) (see Table 3). If $\overline{LD}$ and $\overline{WEN}$ continue to be simultaneously asserted, another 18-bit data word from the data inputs D17-D0 is written into the programmable almost-full flag-offset-value register at the second rising edge of WCLK.

What happens next is determined by the state of the ***$\overline{EMODE}$*** control input. If it is de-asserted (HIGH), the next 18-bit word from the data inputs D17-D0 is written back into the programmable almost-empty flag-offset-value register again.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 5. PROGRAMMABLE REGISTERS



Control-Register Bits

6 Future use to control depth cascading and interlocking paralleling.
5 Enables suppressing reading whenever data outputs are enabled.
4 Makes $\overline{PAF}$ synchronous.
3 2 Makes $\overline{HF}$ synchronous. (See the control-register format table for the encoding of bits 02-03.)
1 Makes $\overline{PAE}$ synchronous.
0 Selects reinitialized addressing of the programmable registers.

Notes:

1. Default offset values are $63_{10} = 3F_{16}$ (QS72215) or $127_{10} = 7F_{16}$ (QS72225).
2. Bits 17-9 (QS72215) or 17-10 (QS72225) of both offset-value registers should in all cases be programmed LOW (zero).
3. This bit position is used for offset values in the QS72225 only. In the QS72215, it should always be programmed LOW.
4. ***See the control register format table for the default states of the control register, for $\overline{EMODE}$ = HIGH (standard operating mode) and for $\overline{EMODE}$ = LOW (enhanced operating mode). The control register is not accessible in standard operating mode.***
5. ***The assertion of $\overline{EMODE}$ (LOW) forces control register bits 00-05 HIGH during a reset operation. After that, these bits may be programmed at will.***

 = reserved. Do not load with non-zero information.

But, if $\overline{EMODE}$ is asserted (LOW), then still another 18-bit data word from the data inputs D17-D0 is written into the control register at the third rising edge of WCLK. At the fourth rising edge of WCLK, writing again occurs to the programmable almost-empty flag-offset-value register; and the same three-step writing sequence gets repeated on subsequent WCLK rising edges.

The lower nine bits of these offset-value words are made use of by the 512-word QS72215, and the lower ten bits by the 1024-word QS72225. ***Five active bits are used for the control register by both the QS72215 and the QS72225.*** There is no restriction on the values which may occur in these offset value and control-register fields. However, reserved bit positions must be encoded LOW in order to maintain forward compatibility.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

Writing contents to these two ***or three*** programmable registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{WEN}$ is not being asserted (is HIGH), the FIFO's internal programmable-register write-address pointer maintains its present value, without any writing actually taking place at each rising edge of WCLK (see Table 3). Thus, for instance, one or two programmable registers may be written, after which the FIFO may be returned to normal FIFO-array-read/write operation by de-asserting $\overline{LD}$ (to HIGH).

Likewise, whenever $\overline{LD}$ and $\overline{REN}$ are simultaneously being asserted (are both LOW) the 18-bit data word (zero-filled as necessary) from the Programmable Almost-Empty flag-offset-value register is read to the data outputs Q17-Q0 at the first rising edge (LOW-to-HIGH transition) of the read clock (RCLK) (see Table 3). If $\overline{LD}$ and $\overline{REN}$ continue to be simultaneously asserted, another 18-bit data word from the programmable almost-full flag-offset-value register is read to the data outputs Q17-Q0 at the second rising edge of RCLK.

What happens next is determined by the state of the ***EMODE*** control input. If it is de-asserted (HIGH), the next 18-bit word again comes from the programmable Almost-Empty flag-offset-value register; it is read to the data outputs Q17-Q0.

But, if $\overline{EMODE}$ is asserted (LOW), then the next 18-bit data word instead comes from the control register; it is read to the data outputs Q17-Q0 at the third rising edge of RCLK. At the fourth rising edge of RCLK, reading again occurs from the programmable Almost-Empty flag-offset-value register and the same three-step reading sequence gets repeated on subsequent RCLK rising edges.

Reading contents from these two or ***three*** programmable registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{REN}$ is not being asserted (is HIGH), the FIFO's internal programmable register-read-address pointer maintains its present value, without any reading actually taking place at each rising edge of RCLK (see Table 3). Thus, for instance, one or two programmable registers may be read, after which the FIFO may be returned to normal FIFO-array-read/write operation by de-asserting $\overline{LD}$ (to HIGH).

To ensure correct operation, rising edges of WCLK and RCLK should not both be occurring at the same time while $\overline{LD}$ is being asserted.

FIRST LOAD/*RETRANSMIT* ($\overline{FL}$/*RT*)

$\overline{FL}$/RT is a dual-purpose signal. It is one of four input signals which select the grouping mode in which the FIFO operates after being reset; the other three of these input signals are ***$\overline{WXI}$/WEN2, $\overline{RXI}$/REN2, and $\overline{EMODE}$***. ***There are four*** possible grouping modes: standalone, ***interlocked paralleled***, cascaded "master" or "first-load," and cascaded "slave." The designations "master" and "slave" pertain to standard depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone or paralleled operation, the $\overline{FL}$/*RT* pin should be grounded for strict standard operating mode operation. ***However, if it is taken HIGH, regardless of the state of the $\overline{EMODE}$ control input, the FIFO's internal read-address pointer is reset to address the FIFO's first physical memory location, without the other usual reset actions being taken, in particular the FIFO's internal write-address pointer is unaffected. Subsequent read operations may then again read out the same block of data, delimited by the FIFO's first physical memory location and the current value of the write pointer, as was read out previously. There is no limit on the number of times that a block of data may be retransmitted. The only restrictions are that neither the read-address pointer nor the write-address pointer may "wraparound" and address the FIFO's first physical memory location a second time during the retransmission process, and that*** the retransmit facility is unavailable during cascaded operation.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

In standard cascaded operation, $\overline{FL}$/***RT*** is grounded to distinguish the "master" or "first-load" FIFO from the other "slave" FIFO's in the cascade, which must all have their $\overline{FL}$/***RT*** inputs HIGH during a reset operation. (See again Tables 1 and 2.) The cascade will not operate correctly either without any "master" FIFO, or with more than one "master" FIFO.

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES

WRITE EXPANSION INPUT/*WRITE ENABLE2 (*$\overline{WXI}$/*WEN2)*

$\overline{WXI}$/***WEN2*** is a dual-purpose signal. It is one of four input signals which select the grouping mode in which the FIFO operates after being reset; the other three of these input signals are $\overline{FL}$/***RT*** and $\overline{RXI}$/***REN2 and*** $\overline{EMODE}$. There are ***four*** possible grouping modes: standalone, ***interlocked paralleled,*** cascaded "master or "first-load," and cascaded "slave." The designations "master" and "slave" pertain to standard depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. ***In interlocked paralleled operation,*** $\overline{WXI}$***/WEN2 is tied to*** $\overline{FF}$ ***of the other paralleled FIFO, and*** $\overline{RXI}$***/REN2 is tied to*** $\overline{EF}$ ***of that same other FIFO. This interconnection scheme ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews***

In cascaded operation, $\overline{WXI}$/***WEN2*** is connected to the $\overline{WXO}$ (write expansion output; actually $\overline{WXO}$/$\overline{HF}$) output of the previous FIFO in the cascade. $\overline{RXI}$/***REN2*** is likewise connected to the $\overline{RXO}$ (read expansion output; actually $\overline{RXO}$/$\overline{EF2}$) output of that previous FIFO. A reset operation forces $\overline{WXO}$/$\overline{HF}$ and $\overline{RXO}$/$\overline{EF2}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** inputs thus connected come up in one of the two cascaded grouping modes, according to whether their $\overline{FL}$/***RT*** inputs are grounded or tied HIGH (see again Tables 1 and 2).

READ EXPANSION INPUT/*READ ENABLE 2 (*$\overline{RXI}$/*REN2)*

$\overline{RXI}$/***REN2*** is a dual-purpose signal. It is one of four input signals which select the grouping mode in which the FIFO operates after being reset; the other three of these input signals are $\overline{FL}$/***RT*** and $\overline{WXI}$/***WEN2 and*** $\overline{EMODE}$. There are four possible grouping modes: standalone, ***interlocked paralleled***, cascaded "master" or "first-load," and cascaded "slave." The designations "master" and "slave" pertain to standard depth cascading. Tables 1 and 2 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. ***In interlocked paralleled operation,*** $\overline{WXI}$***/WEN2 is tied to*** $\overline{FF}$ ***of the other paralleled FIFO, and*** $\overline{RXI}$***/REN2 is tied to*** $\overline{EF}$ ***of that same other FIFO. This interconnection scheme ensures that both FIFOs will operate together and remain coordinated, regardless of timing skews.***

In cascaded operation, $\overline{RXI}$/***REN2*** is connected to $\overline{RXO}$ (read expansion output; actually RXO/***EF2***) of the previous FIFO in the cascade. $\overline{WXI}$/***WEN2*** is likewise connected to $\overline{WXO}$ (write expansion output; actually $\overline{WXO}$/$\overline{HF}$) output of that previous FIFO. A reset operation forces $\overline{RXO}$/$\overline{EF2}$ and $\overline{WXO}$/$\overline{HF}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{RXI}$/***REN2*** and $\overline{WXI}$/***WEN2*** inputs thus connected come up in one of the two standard cascaded grouping modes, according to whether their $\overline{FL}$/***RT*** inputs are grounded or tied HIGH (see again Tables 1 and 2).

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

Data Outputs

DATA OUT (Q17-Q0)

Data, programmable flag-offset values, and ***control register*** codes are output from the FIFO as 18-bit words on Q17-Q0. Unused bit positions in offset-value words and ***control-register*** words are zero-filled.

Control/Status Outputs

FULL FLAG ($\overline{FF}$)

$\overline{FF}$ goes LOW whenever the FIFO is completely full. That is, whenever the FIFO's internal write pointer has completely caught up with its internal read pointer; so that, if another word were to be written, it would have to overwrite the unread word which is now in position for reading out by the next requested read operation. Under these conditions, the FIFO is filled to its nominal capacity, which is 512 18-bit words for the QS72215 or 1024 18-bit words for the QS72225. Write operations are inhibited whenever $\overline{FF}$ is LOW, regardless of the assertion or de-assertion of Write Enable ($\overline{WEN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), $\overline{FF}$ initially is HIGH. But, whenever no read operations have been performed since the completion of the reset operation, $\overline{FF}$ goes LOW after 512 write operations for the QS72215, or after 1024 write operations for the QS72225 (see Table 4).

$\overline{FF}$ gets updated after a LOW-to-HIGH transition of the write clock (WCLK).

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

$\overline{PAF}$ goes LOW whenever the FIFO is "almost" full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than the value of the programmable almost-full flag offset "p." The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the QS72215 or 1024 for the QS72225.

The default value of "p" after the completion of a reset operation is one-eighth of the total number of words in the FIFO-memory array, minus one: 63 for the QS72215 or 127 for the QS72225. However, "p" may be set to any value which does not exceed this total nominal number of words for the device, as explained in the description of load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no read operations have been performed since the completion of the reset operation, $\overline{PAF}$ goes LOW after 512 – p write operations for the QS72215, or after 1024–p write operations for the QS72225 (see Table 4).

If "p" is still at its default value, $\overline{PAF}$ is LOW whenever the FIFO is from seven-eighths full to completely full.

In the standard operating mode, $\overline{PAF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the read clock RCLK. Thus, in this operating mode, $\overline{PAF}$ behaves as an "asynchronous flag."

In the enhanced operating mode, on the other hand, $\overline{PAF}$ gets updated only after a LOW-to-HIGH transition of the write clock WCLK, and thus behaves as a "synchronous flag" whenever control register bit 04 is HIGH (see Table 5).

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

$\overline{WXO}/\overline{HF}$ is a dual-purpose signal. In "standalone" operation, it behaves as a Half-Full flag ($\overline{HF}$), in accordance with Table 4. In standard "cascaded" operation, it behaves as a write expansion output ($\overline{WXO}$) signal to coordinate writing operations with the next FIFO in the cascade. Under these same conditions, also, the dual-purpose $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** inputs behave as write expansion input ($\overline{WXI}$) and read expansion input ($\overline{RXI}$) signals, respectively.

When two or more QS72215 or QS72225 FIFOs are "cascaded" to operate as a deeper "effective FIFO," in a "daisy chain" ring configuration, the write expansion input ($\overline{WXI}$) of each FIFO is connected to $\overline{WXO}$ of the previous FIFO in the ring, with $\overline{WXI}$ of the "first-load" or "master" FIFO being connected to $\overline{WXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{WXO}$-to-$\overline{WXI}$ connections, for read expansion input ($\overline{RXI}$) and read expansion output ($\overline{RXO}$/***EF2***, when it is behaving as $\overline{RXO}$).

When the last physical location has been written in a FIFO operating in cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{WXO}$ output, and the FIFO is deactivated for writing at the next valid WCLK; and the next FIFO in the ring is simultaneously activated for writing. Otherwise, $\overline{WXO}$ remains constantly HIGH whenever the FIFO is operating in cascaded mode. This LOW-going $\overline{WXO}$ pulse serves as a write token" in the "token-passing" FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{WXI}$ input. When this next FIFO receives the write token, it is activated for writing at the next valid WCLK.

The foregoing description applies both to the "first-load" or "master" FIFO in the ring, and to any and all "slave" FIFOs in the ring. However, $\overline{WXO}$ has no necessary function for FIFO's operating in the "standalone" mode. Consequently, in that mode, the same output pin is used for $\overline{HF}$; it follows that $\overline{HF}$ is not available as an output from any FIFO which is operating in the standard cascaded mode. A FIFO is initialized into "cascaded master" mode, into "cascaded slave" mode, ***into interlocked paralleled*** mode, or into standalone mode according to the state of its $\overline{WXI}$/***WEN2***, $\overline{RXI}$/***REN2***, and $\overline{FL}$/***RT*** control inputs during a reset operation, ***and of $\overline{EMODE}$*** (see Table 1, Table 2, and Table 5).

In standalone ***or interlocked paralleled*** operation, $\overline{HF}$ goes LOW whenever the FIFO is more than half full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than half of the total nominal number of 18-bit words in the FIFO's physical memory, which is 256 for the QS72215 or 512 for the QS72225 (see Table 4). The subtraction is performed using modular arithmetic, this total nominal number of words, which is 512 for the QS72215 or 1024 for the QS72225.

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and it is operating in standalone mode or in ***interlocked paralleled*** mode, and no read operations have been performed since the completion of the reset operation, $\overline{HF}$ goes LOW after 257 write operations for the QS72215, or after 513 write operations for the QS72225 (see again Table 4).

In the standard operating mode, $\overline{HF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the write clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the read clock RCLK. Thus, in this operating mode, $\overline{HF}$ behaves as an "asynchronous flag."

In the enhanced operating mode, on the other hand. $\overline{HF}$ gets updated only after a LOW-to-HIGH transition of the read clock RCLK, or else after a LOW-to-HIGH transition of the write clock WCLK, according to the setting of bits 03 and 02 of the control register (see Table 5). Thus, in this mode, $\overline{HF}$ behaves as a "synchronous flag," and may be synchronized either to the input side of the FIFO (i.e., to WCLK), or to the output side of the FIFO (i.e., to RCLK).

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

$\overline{PAE}$ goes LOW whenever the FIFO is "almost empty"; that is, whenever subtracting the value of the FIFO's internal write pointer from the value of its internal read pointer yields a difference which is less than q + 1, where "q" is the value of the programmable almost-empty flag offset. The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the QS72215 or 1024 for the QS72225.

The default value of "q" after the completion of a reset operation is one-eighth of the total number of words in the FIFO-memory array, minus one; 63 for the QS72215 or 127 for the QS72225. However, "q" may be set to any value which does not exceed this total nominal number of words for the device, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{PAE}$ is LOW (see Table 4). If "q" is still at its default value, $\overline{PAE}$ is LOW whenever the FIFO is from one-eighth full to completely empty.

In the standard operating mode, $\overline{PAE}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the read clock RCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the write clock WCLK. Thus, in this operating mode, $\overline{PAE}$ behaves as an "asynchronous flag."

In the enhanced operating mode, on the other hand, $\overline{PAE}$ gets updated only after a LOW-to-HIGH transition of the read clock RCLK, and thus behaves as a "synchronous flag" whenever control register bit 01 is HIGH (see Table 5).

EMPTY FLAG ($\overline{EF}$)

$\overline{EF}$ goes LOW whenever the FIFO is completely empty, that is, whenever the FIFO's internal read pointer has completely caught up with its internal write pointer; so that, if another word were to be read out, it would have to come from the physical memory location which is now in position to be written into by the next requested write operation. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the assertion or de-assertion of read enable ($\overline{REN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{EF}$ is LOW (see Table 4). $\overline{EF}$ gets updated after a LOW-to-HIGH transition of the read clock RCLK.

READ EXPANSION OUT/*EMPTY FLAG 2* ($\overline{RXO}$/*$\overline{EF2}$*)

When two or more QS72215 or QS72225 FIFOs are operating in standard "cascaded" mode as a deeper "effective FIFO," the dual-purpose $\overline{RXI}$/***REN2*** and $\overline{WXI}$/**WEN2** inputs behave as read expansion input ($\overline{RXI}$) and write expansion input ($\overline{WXI}$) signals respectively. A cascade of these FIFO devices has a "daisy-chain" ring configuration; the read expansion input ($\overline{RXI}$) of each FIFO is connected to $\overline{RXO}$/***EF2*** behaving as $\overline{RXO}$) of the previous FIFO in the ring, with $\overline{RXI}$ of the "first-load" or "master" FIFO being connected to $\overline{RXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{RXO}$-to-$\overline{RXI}$ connections, for write expansion input ($\overline{WXI}$) and write expansion output ($\overline{WXO}$).

When the last physical location has been read in a FIFO operating in standard-style cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{RXO}$ output; otherwise, $\overline{RXO}$ remains constantly HIGH. This LOW-going $\overline{RXO}$ pulse serves as a "read token" in the token-passing FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{RXI}$ input. When this next FIFO receives the token, it is activated for reading at the next valid RCLK.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES *(Continued)*

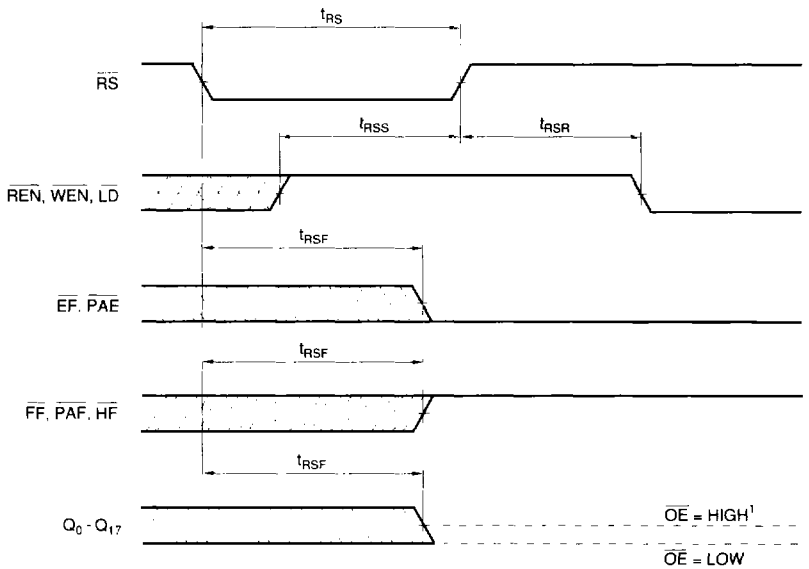
After a FIFO emits an $\overline{RXO}$ pulse, the FIFO is deactivated for reading at the next valid RCLK. Also, its data outputs go into HIGH-Z state, regardless of the assertion or deassertion of its output enable ($\overline{OE}$) control input, until it again receives the token. Simultaneously, the next FIFO in the ring is activated for reading.

The foregoing description applies both to the "first-load" or "master" FIFO in the ring, and to any and all "slave" FIFOs in the ring. However, $\overline{RXO}$ has no necessary function for a FIFO which is operating in "standalone" mode. Consequently, in that mode, $\overline{RXO}$ is never asserted, and remains constantly HIGH. A FIFO is initialized into "standalone" mode, into "cascaded master" mode, or into "cascaded slave" mode according to the state of its $\overline{WXI}$/***WEN2***, $\overline{RXI}$/***REN2***, and $\overline{FL}$/***RT*** control inputs during a reset operation. ***It also may be forced into interlocked paralleled mode by $\overline{EMODE}$ (see Table 1, Table 2, and Table 5).***

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

TIMING DIAGRAMS

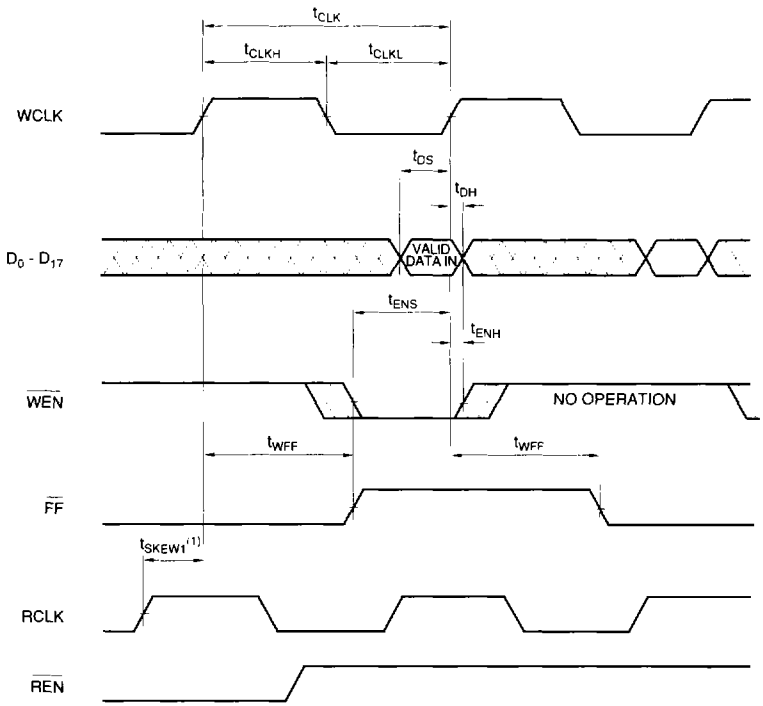
FIGURE 6. RESET TIMING



Notes:
1. After reset, the outputs will be LOW if $\overline{OE}$ = LOW, and in a high-impedance state if $\overline{OE}$ = HIGH.
2. The clocks (RCLK, WCLK) may be free running during a reset operation.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 7. SYNCHRONOUS WRITE OPERATION

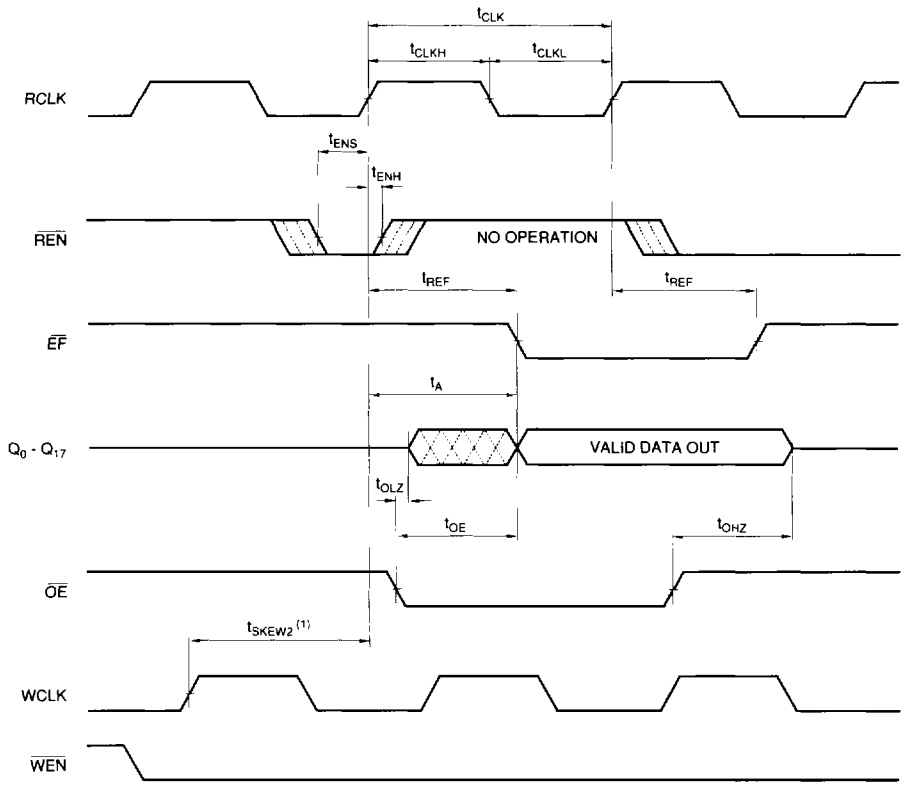


Note:

1. t_{SKEW1} *is the minimum time between a rising RCLK edge and a* rising WCLK edge for FF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that FF will change state until the next following WCLK edge.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 8. SYNCHRONOUS WRITE OPERATION

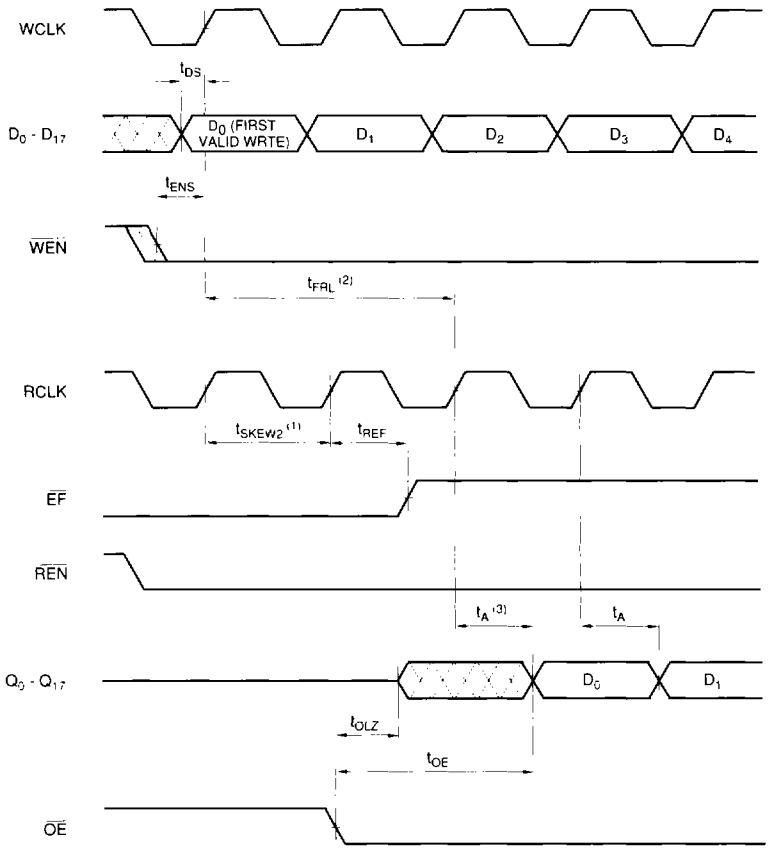


Note:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{EF}$ will change state until the next following RCLK edge.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 9. LATENCY FOR THE FIRST DATA WORD AFTER A RESET OPERATION, WITH SIMULTANEOUS READ AND WRITE



Notes:

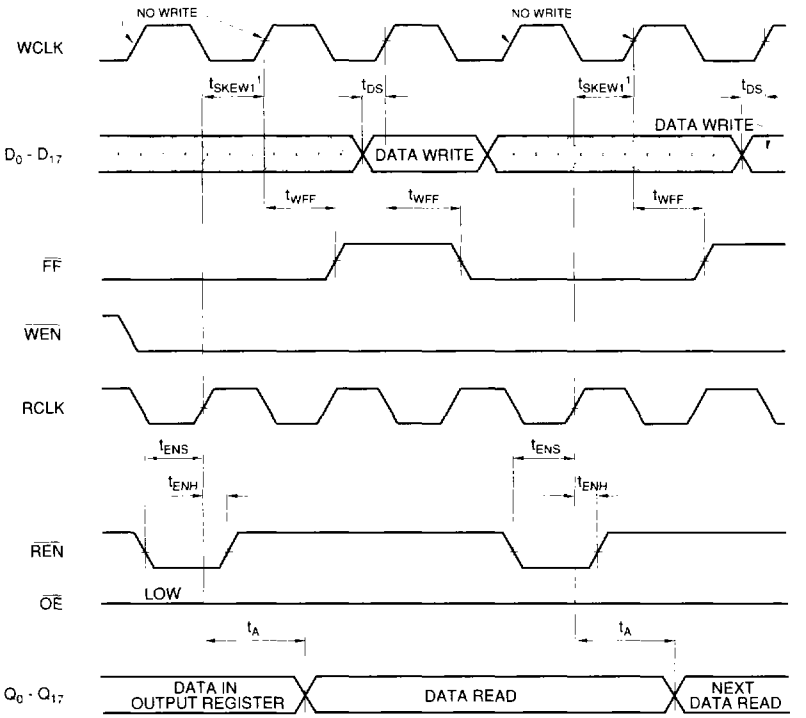
1. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then it is not guaranteed that FF will change state until the next following WCLK edge.

2. t_{FRL} (first-read latency) is the minimum time between a rising WCLK edge and a rising RCLK edge to assure a correct readout of the first data word D_0 in response to the next RCLK edge. Thus, $t_{FRL} = t_{CLK} + t_{SKEW2}$. If t_{FRL} is not met, D_0 may be available either at $t_{CLK} + t_{SKEW2}$, or after one more clock cycle delay at $2\ t_{CLK} + t_{SKEW2}$. The first-read latency timing restrictions apply only when the FIFO has been empty ($\overline{EF}$ = LOW).

3. $\overline{EF}$ may be used to determine when the first data word D_0 may be read. D_0 always is available on the next cycle after $\overline{EF}$ has gone HIGH.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 10. FULL FLAG TIMING

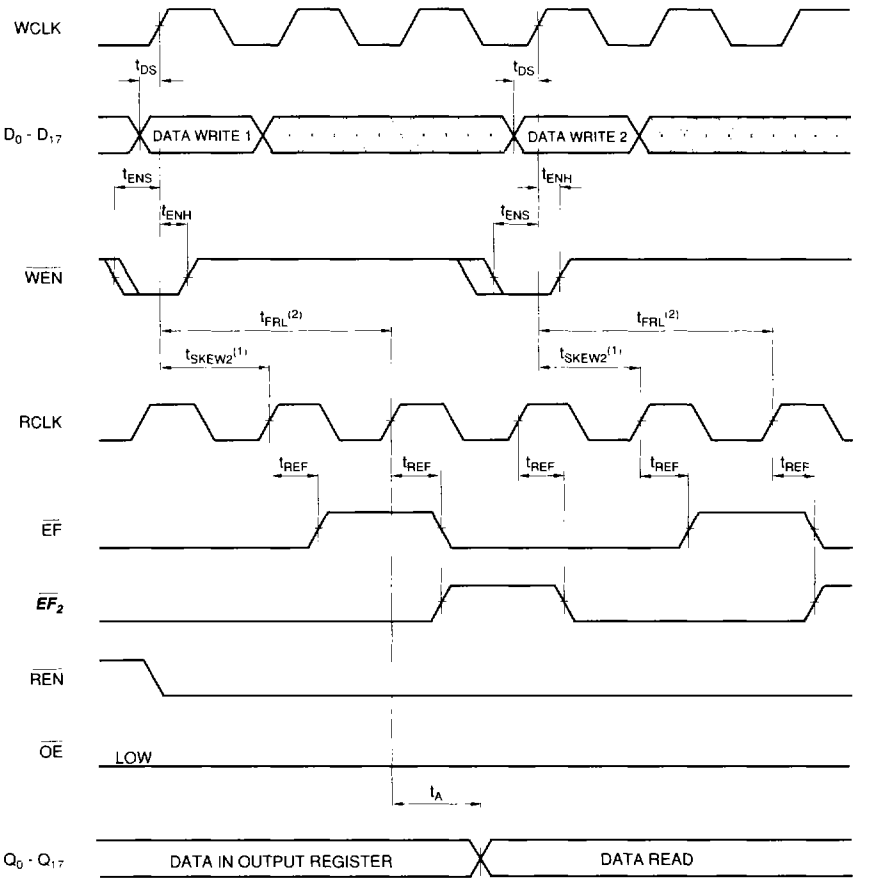


Note:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that FF will change state until the next following WCLK edge.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 11. EMPTY FLAG TIMING



Notes:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that $\overline{EF}$ will change state until the next following RCLK edge.

2. t_{FRL} *(first-read latency) is the minimum time between a rising* WCLK edge and a rising RCLK edge to assure a correct readout of the first data word D_0 in response to the next RCLK edge. Thus, $t_{FRL} = t_{CLK} + t_{SKEW2}$. *If* t_{FRL} *is not met,* D_0 *may be available either at* $t_{CLK} + t_{SKEW2}$, *or after* one more clock cycle delay at $2\ t_{CLK} + t_{SKEW2}$. The first-read latency timing restrictions apply only when the FIFO has been empty ($\overline{EF}$ = LOW).

3. $\overline{EF}$ may be used to determine when the first data word D_0 may be read. D_0 always is available on the next cycle after $\overline{EF}$ has gone HIGH.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 12. PROGRAMMABLE-REGISTER WRITE OPERATION

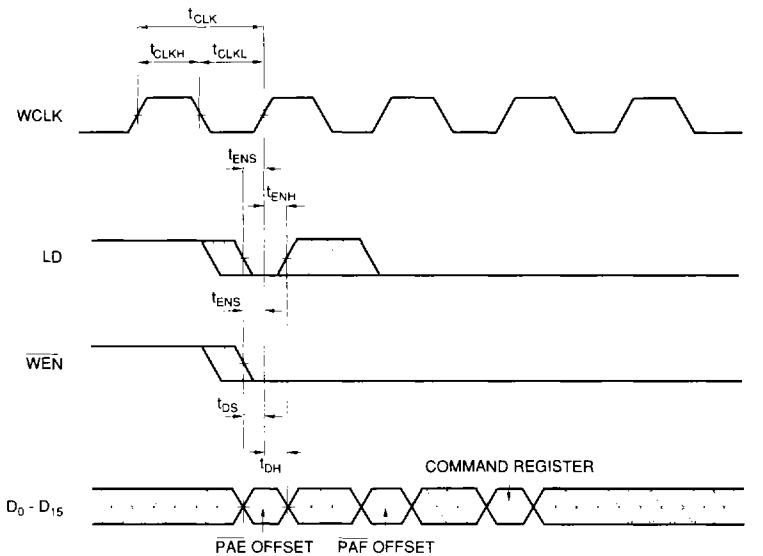
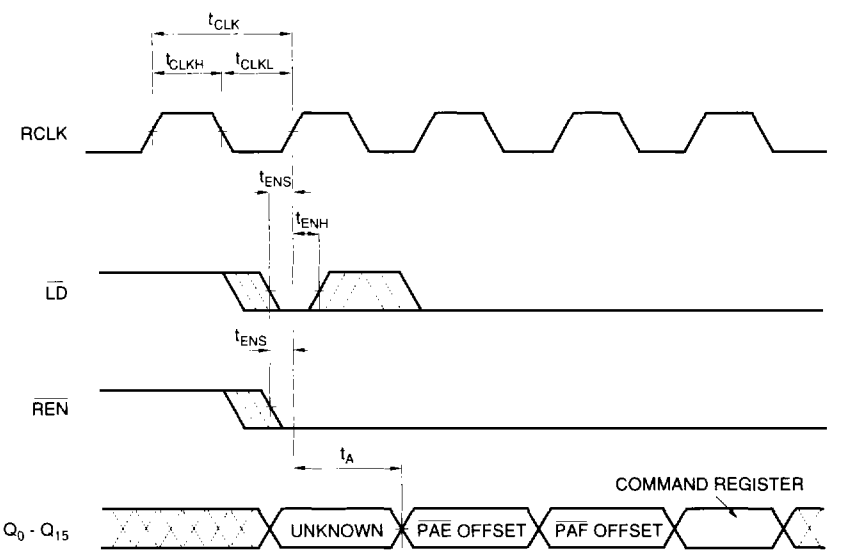
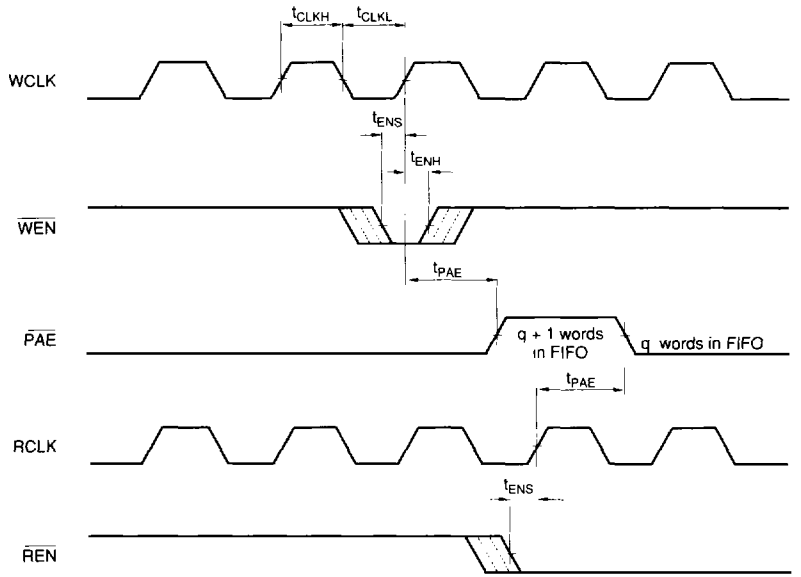


FIGURE 13. PROGRAMMABLE-REGISTER READ OPERATION



BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 14. PROGRAMMABLE ALMOST-EMPTY FLAG TIMING (Standard operating mode)

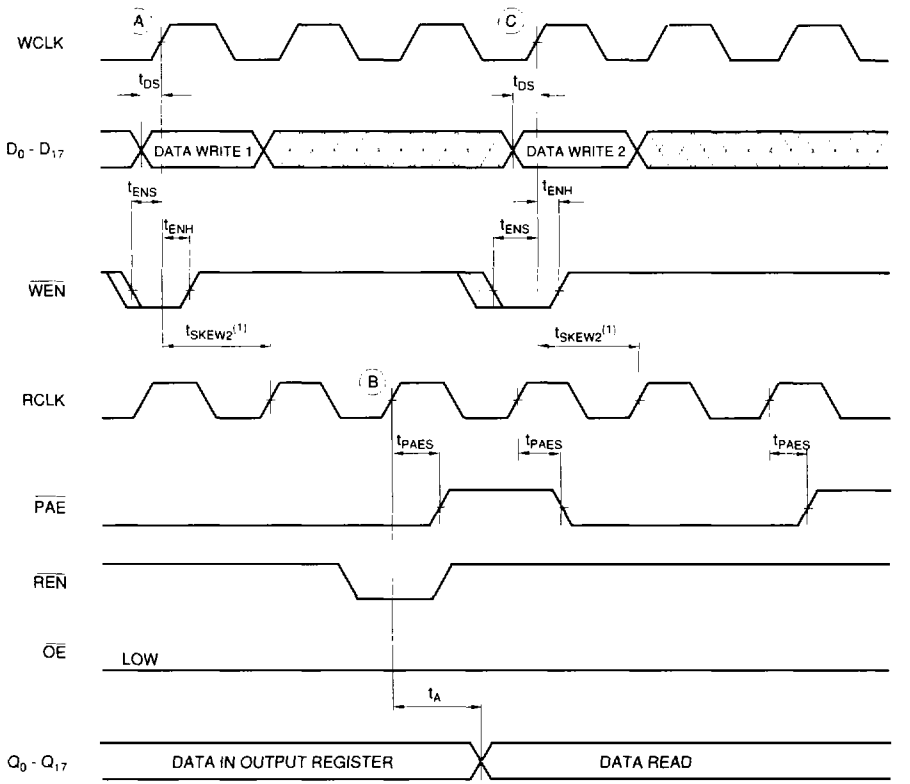


Note:
1. $\overline{PAE}$ offset = q. Also, number of data words written into FIFO already = q.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 15. PROGRAMMABLE-ALMOST-EMPTY FLAG TIMING When Synchronous (Enhanced operating mode)

Enhanced Operating Mode Timing Diagram



Notes:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for PAE to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that PAE will change state until the next following RCLK edge.

2. PAE offset = q. Also, number of data words written into FIFO already = q.

3. The internal state of the FIFO:

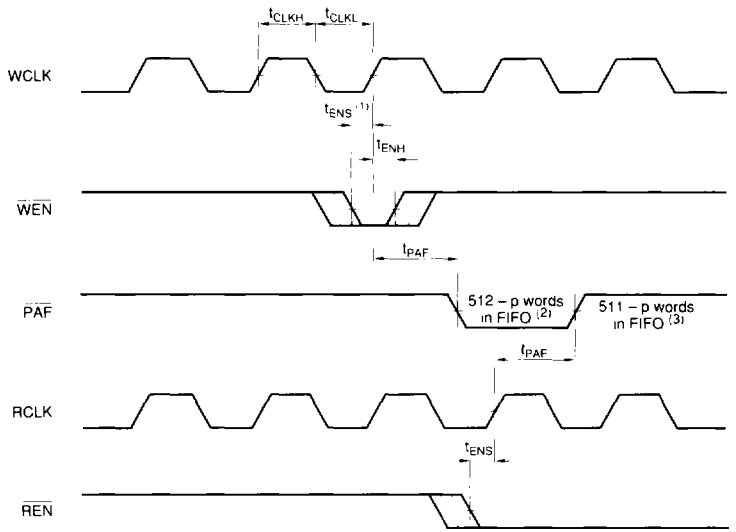
   At (A), q + 1 words.

   At (B), q words.

   At (C), q + 1 words again.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 16. PROGRAMMABLE ALMOST-FULL FLAG TIMING (Standard operating mode)

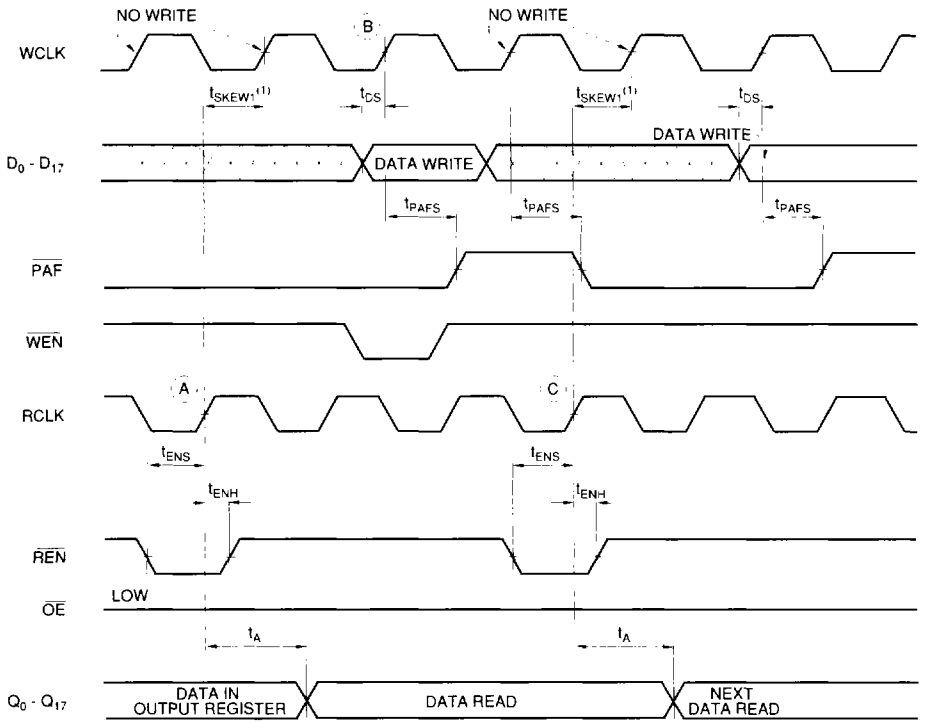


Notes:
1. $\overline{PAF}$ offset = p. Number of data words written into FIFO already = 511 – p for the QS72215 and 1023 – p for the QS72225.
2. 512 – p words in FIFO for QS72215. 1024 – p words in FIFO for QS72225
3. 511 – p words in FIFO for QS72215. 1023 – p words in FIFO for QS72225.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 17. PROGRAMMABLE ALMOST-FULL FLAG TIMING WHEN SYNCHRONOUS (Enhanced operating mode)

Enhanced Operating Mode Timing Diagram



Notes:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for PAF to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that PAF will change state until the next following WCLK edge.
2. PAF offset = p. Number of data words written into FIFO already = 511 – p for the QS72215 and 1023 – p for the QS72225
3. 512 – p words in FIFO for QS72215. 1024 – p words in FIFO for QS72225.
4. 511 – p words in FIFO for QS72215. 1023 – p words in FIFO for QS72225.
5. The internal state of the FIFO.

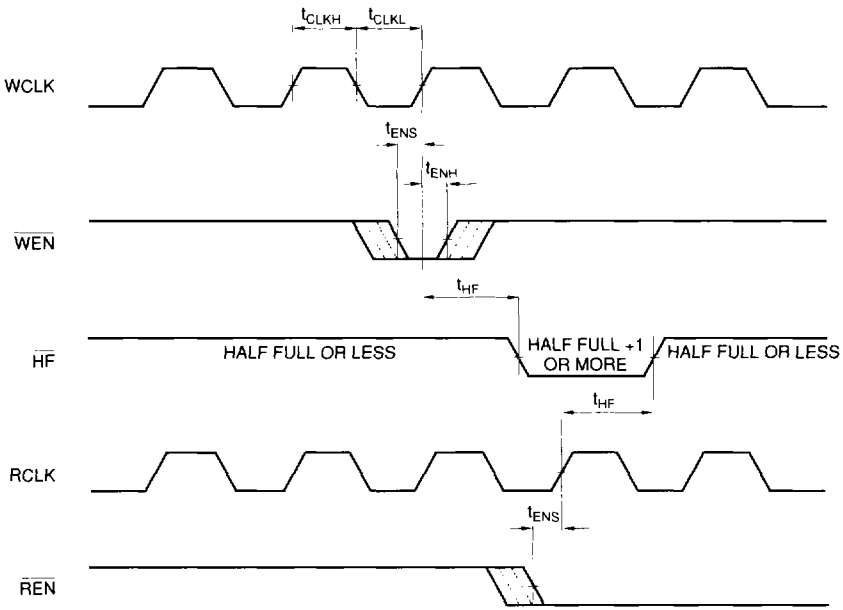
   At A, 511 – p words.

   At B, 512 – p words.

   At C, 511 – p words again.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

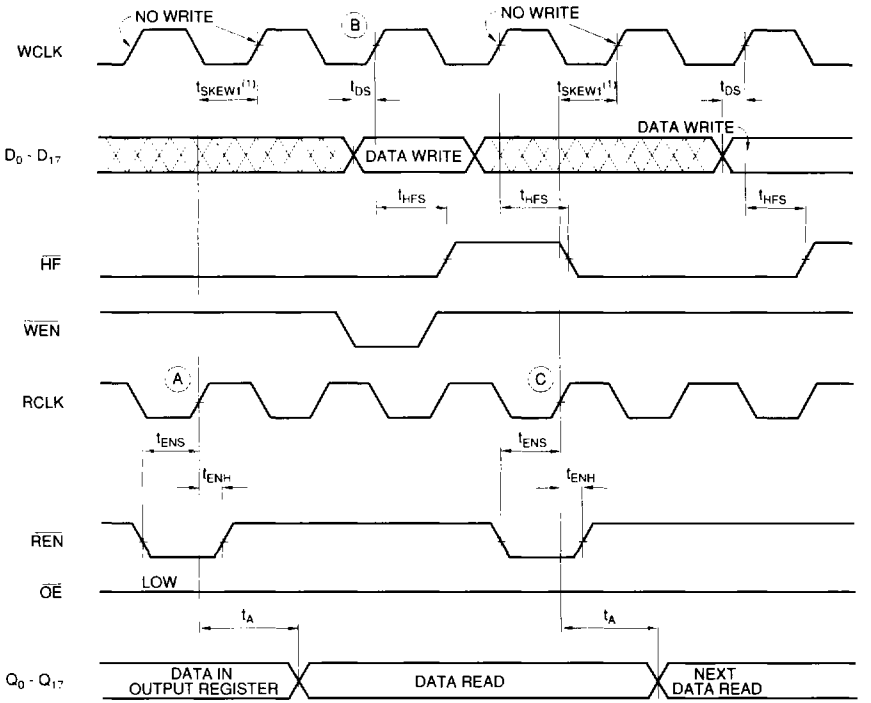
FIGURE 18. HALF-FULL FLAG TIMING (Standard operating mode)



BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = *IDT*-Compatible

FIGURE 19. HALF-FULL FLAG TIMING, WHEN SYNCHRONIZED TO INPUT PORT (Enhanced operating mode)

Enhanced Operating Mode Timing Diagram



Notes:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{HF}$ to change predictably during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then it is not guaranteed that $\overline{HF}$ will change state until the next following WCLK edge.

2. The internal state of the FIFO:

   At (A), exactly half full.

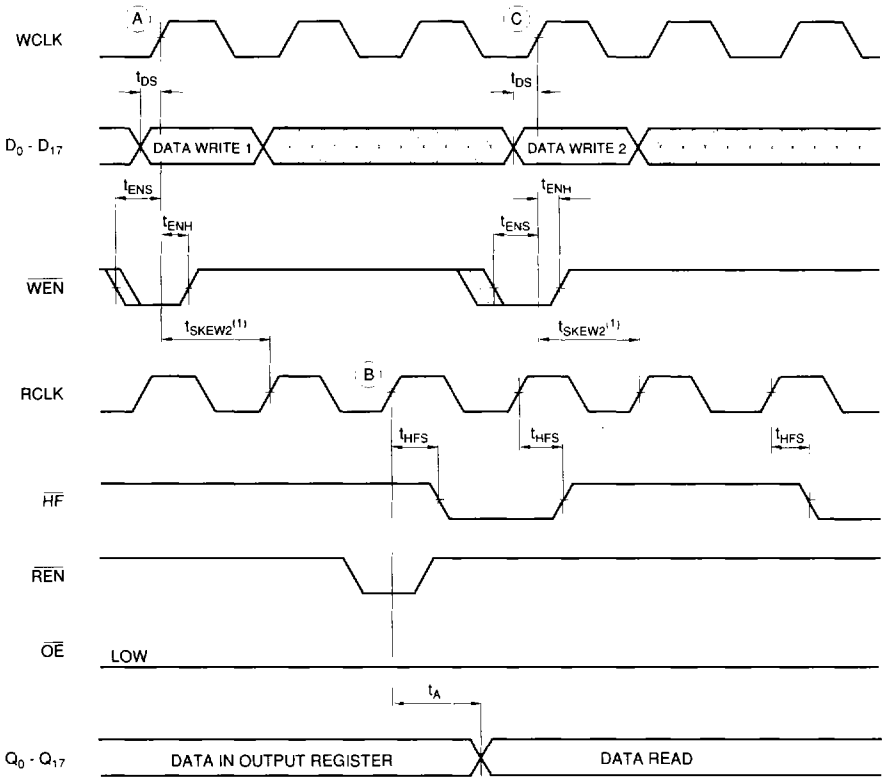
   At (B), half+1 words.

   At (C), exactly half full again.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 20. HALF-FULL FLAG TIMING, WHEN SYNCHRONIZED TO OUTPUT PORT (Enhanced operating mode)

Enhanced Operating Mode Timing Diagram



Notes:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for HF to change predictably during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then it is not guaranteed that HF will change state until the next following RCLK edge.

2. The internal state of the FIFO:

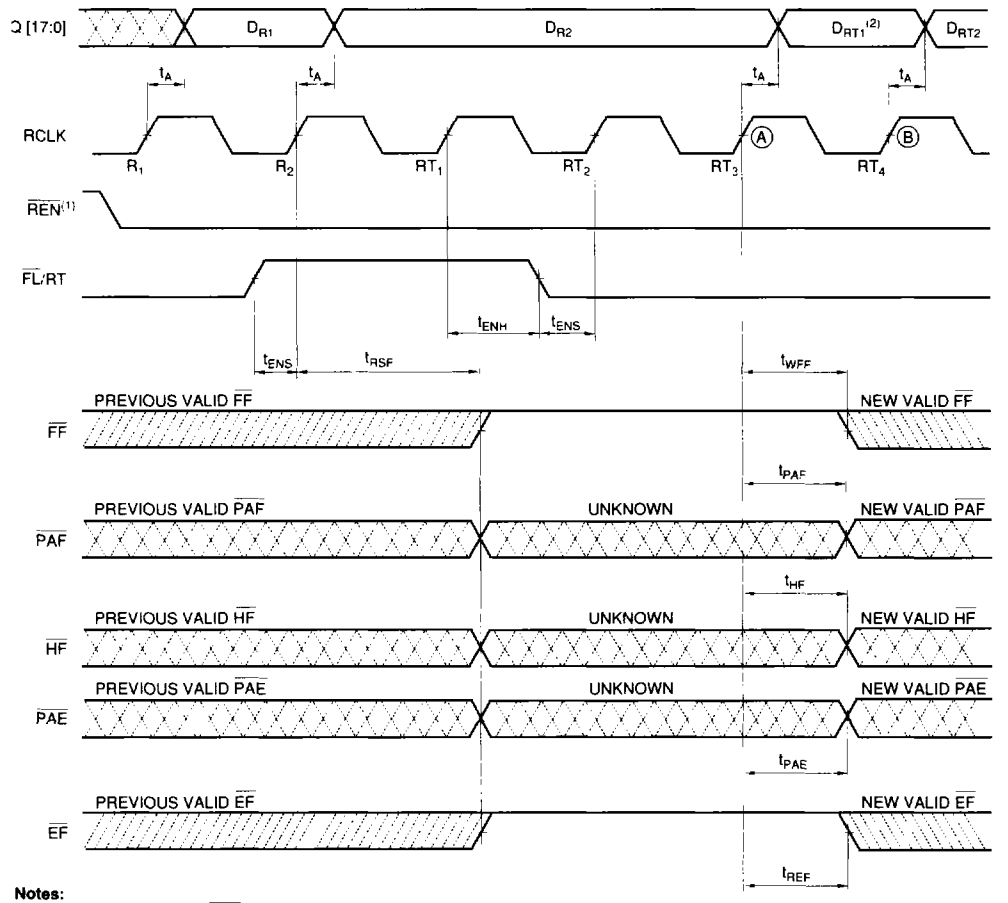
   At (A), half+1 words.

   At (B), exactly half full.

   At (C), half+1 words again.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 21. RETRANSMIT TIMING (Standard operating mode)

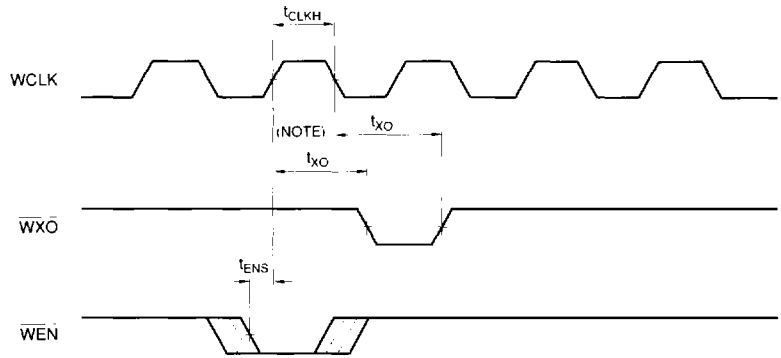


Notes:

1. It is not necessary for $\overline{REN}$ to be LOW for the device to recognize a retransmit request.
2. In order to actually read data words from the memory array, in IDT-compatible operating mode, REN = LOW; in enhanced operating mode, also $\overline{REN}_2$ = HIGH (and $\overline{OE}$ = LOW, if control register bit 05 = HIGH). In any case, LD = HIGH.
3. D_{RT1} is the data item in physical location zero of the FIFO memory array.
4. The asynchronous intermediate flags (corresponding to LOW control-register bits) will show correct status three RCLK cycles after a retransmit operation, as is shown above. (RT_3, in the above RCLK waveform.)
5. The intermediate flags which have been synchronized to RCLK by setting the appropriate control-register bits to HIGH will show correct status after Ⓑ, four RCLK cycles after a *retransmit operation. (RT_4, in the above RCLK waveform.)*
6. The intermediate flags which have been synchronized to WCLK, by setting the appropriate control-register bits HIGH, will show correct status on the second WCLK rising edge after Ⓐ, assuming that t_{SKEW1} was satisfied at Ⓐ; otherwise the flags will become valid on the third WCLK rising edge after Ⓐ.
7. Immediately after a reset operation, before any write operations have taken place, a retransmit operation is a "no-op," and does not change the state of any FIFO registers or flags.
8. In the special case that the FIFO memory array contains **only one** valid data item, the status of HF and PAF should be ignored on a retransmit.

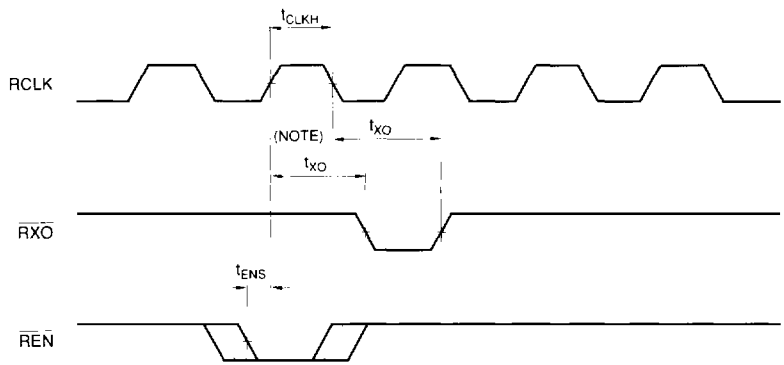
BOLD ITALIC = ENHANCED OPERATING MODE
S andard Operating Mode = IDT-Compatible

FIGURE 22. WRITE-EXPANSION-OUT TIMING (Standard operating mode)



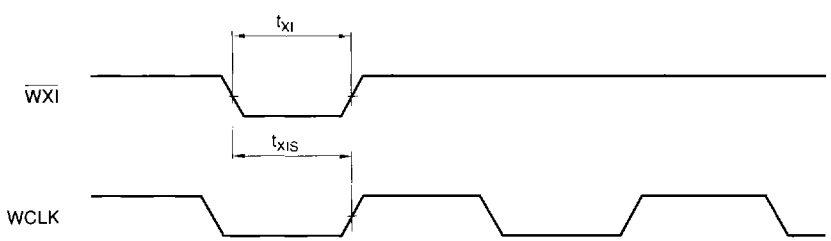
Note: Write to last physical location.

FIGURE 23. READ-EXPANSION-OUT TIMING (Standard operating mode)



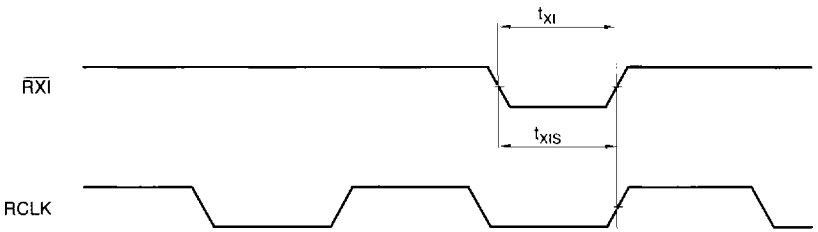
Note: Read from last physical location.

FIGURE 24. WRITE-EXPANSION-IN TIMING (Standard operating mode)



BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 25. READ-EXPANSION-IN TIMING (Standard operating mode)



APPLICATIONS INFORMATION

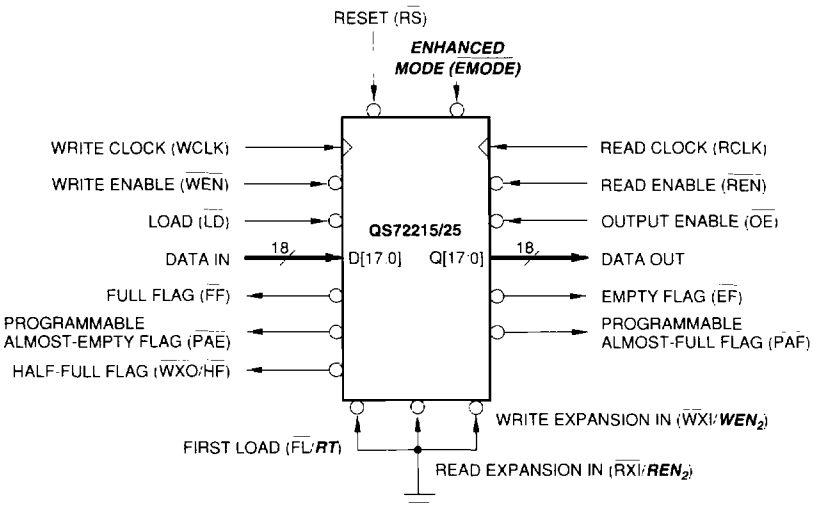
Standalone Configuration

When depth cascading is not required for a given application, the QS72215/25 is placed in standalone mode by tying the two expansion in pins $\overline{WXI}$/***WEN2*** and $\overline{RXI}$/***REN2*** to ground, while also holding the first load/ retransmit pin $\overline{FL}$/***RT*** LOW for the duration of any reset operation (see Table 1). Subsequently, $\overline{FL}$/***RT*** may be taken HIGH at will, whenever a retransmit operation is desired. If not being used, $\overline{FL}$/***RT*** also may be tied to ground, as shown in Figure 26.

Width Expansion

Word-width expansion is implemented by placing multiple QS72215/25 devices in parallel. Each device should be configured for standalone mode, unless the depth of one single FIFO is not adequate for the application. In this event, word-width expansion may in principle be used with either of the two depth-cascading schemes supported by the QS72215/25 architecture. In practice, the reliability benefits of interlocked-paralleled operation are available only with the pipelining scheme, making it the preferred alternative. (Refer to discussion in a later section).

FIGURE 26. STANDARD FIFO (512 x 18/1024 x 18)



BOLD ITALIC = Enhanced Operating Mode.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

When standalone-mode QS72215/25 devices are paralleled, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive "composite" flag values using external logic, since there may be minor speed variations between different actual devices. After writing or reading have been in a disabled state, the process of re-enabling should be gated by the slowest FIFO.

For m paralleled FIFOs, the form of this external composite-flag logic may be an OR gate with m assertive-LOW inputs and an assertive-LOW output. In keeping with deMorgan's theorem, such a gate may be implemented as an AND gate with m assertive-HIGH inputs and an assertive-HIGH output. Figure 27 illustrates the case m = 2.

The QS72215/25 architecture supports two very different methods of depth cascading:

- Token passing, which follows the scheme used in the pin-compatible and functionally-compatible Integrated Device Technology IDT72205/15/25/35/45 FIFOs, which the QS72215/25 can directly replace.
- Pipelining, which follows the scheme used in the Texas Instruments SN74ACT7801/11/81 FIFOs, and also in the Sharp LH543620 1024 x 36 FIFO. The SN74ACT7801/11/81 pinout closely resembles the pinout for the QS72215/25, but is not identical.

Depth Cascading Using Token Passing

Using the token-passing approach, depth cascading is implemented by configuring the required number of QS72215/25's in a circular "ring" fashion, with the expansion out outputs ($\overline{WXO}/\overline{HF}$ and $\overline{RXO}/\overline{\textbf{\textit{EF2}}}$) of each device tied to the expansion in inputs ($\overline{WXI}/\textbf{\textit{WEN2}}$ and $\overline{RXI}/\textbf{\textit{REN2}}$) of the next device (see Figure 28). Because a reset operation forces the $\overline{WXO}/\overline{HF}$ and $\overline{RXO}/\overline{\textbf{\textit{EF2}}}$ outputs HIGH for each device, the $\overline{WXI}/\textbf{\textit{WEN2}}$ and $\overline{RXI}/\textbf{\textit{REN2}}$ inputs for the next device are HIGH during the reset operation; thus, these two inputs are HIGH for all devices in the ring (see Tables 1 and 2, and also Figure 28). All devices in the cascade must be in the standard operating mode; thus, their $\overline{\textbf{\textit{EMODE}}}$ inputs must be tied to Vcc.

One FIFO in the cascade must be designated as the "first-load" device, by tying its first load input ($\overline{FL}/\textbf{\textit{RT}}$) to ground. All other devices must have their $\overline{FL}/\textbf{\textit{RT}}$ inputs tied HIGH. Under these circumstances, the retransmit function is not available for use.

In this mode, the control inputs which govern writing (WCLK and WEN) and the control inputs which govern reading (RCLK and REN) are shared by all devices, while logic within each QS72215/25 governs the steering of data. The common data inputs of all devices are tied together; but only one QS72215/25 is enabled during any given write cycle. Likewise, the common three-state data outputs of all devices are wire-ORed together; but only one QS72215/25 is enabled, including its three-state outputs, during any given read cycle. A data word is handled by only one device as it passes through the cascade of FIFOs, regardless of how many FIFOs are being cascaded together.

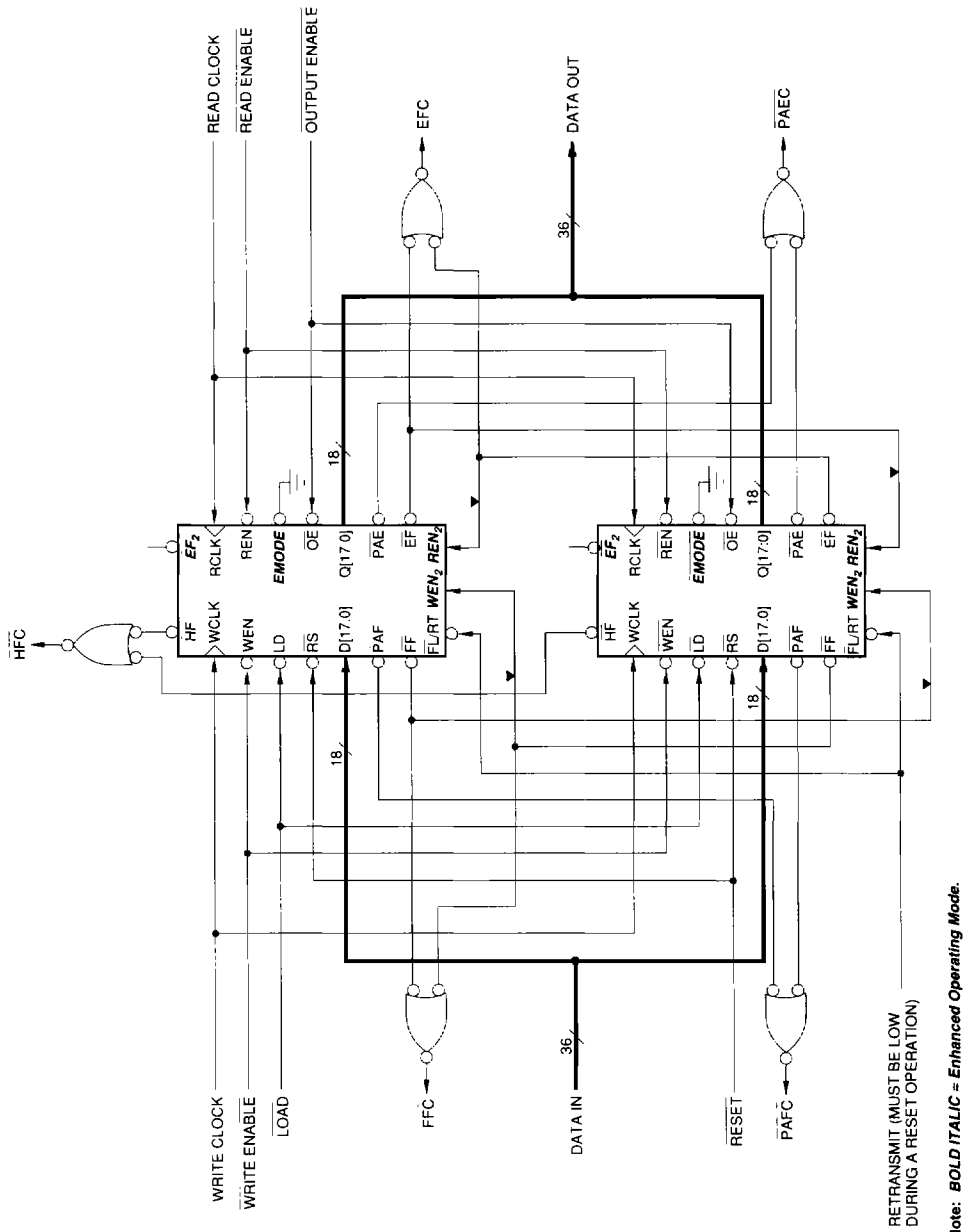
In the token-passing depth-cascaded mode, external logic should be used to generate a composite Full flag and a composite Empty flag, by ANDing the $\overline{FF}$ outputs of all QS72215/25 devices together and by ANDing the $\overline{EF}$ outputs of all devices together, using AND gates with assertive-LOW inputs and an assertive-LOW output. Here, the meaning of these composite flags is direct: the cascade of FIFOs is full, if and only if all k-FIFOs belonging to the cascade are individually full; and similarly for empty. In keeping with deMorgan's theorem, these k-input assertive-LOW AND gates are implemented physically as k-input assertive-HIGH OR gates. Figure 28 illustrates the case k = 3.

Similar external logic also may be used to generate a composite Programmable Almost-Full flag and a composite Programmable Almost-Empty flag, by ANDing the $\overline{PAF}$ outputs of all QS72215/25 devices together and by ANDing the $\overline{PAE}$ outputs of all devices together. Here, however, some careful analysis is required to determine exactly what the resulting composite flags mean. Their significance may vary widely, depending on the number of FIFOs in the cascade, and on the "offset" values which are present in the offset registers for these FIFOs. More complex logical combinations of $\overline{PAF}$ outputs with $\overline{FF}$ outputs, and of $\overline{PAE}$ outputs with $\overline{EF}$ outputs, may be found useful in particular applications.

In any case, the Half-Full flag and the retransmit function are not available for devices being used in token-passing depth-cascaded mode.

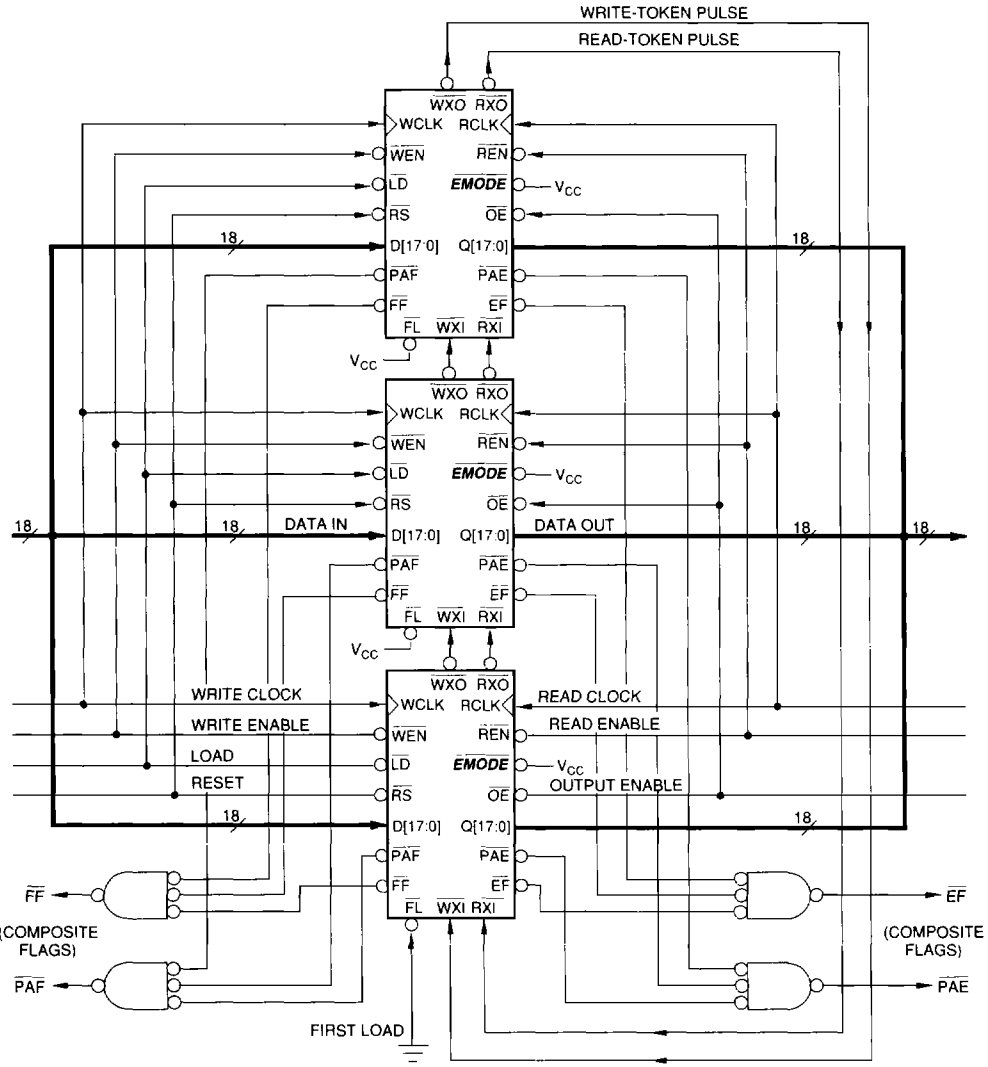
BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 27. INTERLOCKED-PARALLELED WORD-WIDTH EXPANSION



BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

FIGURE 28. SYNCHRONOUS-FIFO DEPTH-CASCADING USING STANDARD OPERATING MODE "TOKEN-PASSING" SCHEME



Notes :
Grounding $\overline{FL}$ designates the "first-load" FIFO ("master" FIFO). The remaining FIFOs are "slave" FIFOs.
BOLD ITALIC = Enhanced Operating Mode.

Depth Cascading Using Pipelining

Using the pipelining approach, depth cascading is implemented by connecting the required number of QS72215/25s in series. Within the cascade, the data outputs of each device are connected to the data inputs of the next device (see Figure 29a). All devices in the cascade must be in ***the enhanced operating mode***; thus, their ***$\overline{EMODE}$*** inputs must be grounded.

Successive devices in the cascade are crosscoupled; they control each other, using a "handclasp" scheme for crossconnecting their control inputs and their status outputs (see again Figure 29a). The input side of the first device, and the output side of the last device are not crosscoupled to other devices. Their control/status and clock pins are connected to the external system.

For the FIFO devices within the cascade, transferring data from each device to the next device is governed by a clock. Preferably, the same clock should be used at every FIFO-to-FIFO data-transfer interface boundary within the cascade. This "transfer clock" may be either the external write clock or the external read clock. If both of these two clocks are periodic and free-running, the faster of the two is the obvious choice for the "transfer clock." Of course, in principle, the "transfer clock" may even be some other, totally different clock.

The Empty flag of each device is used to govern writing into the next device, and the Full flag of each device is used to govern reading from the preceding device. Since the standard Empty flag $\overline{EF}$ occurs one RCLK cycle too early to properly enable/disable the next device, ***the duplicate Empt flag ($\overline{EF2}$) is used instead; $\overline{EF2}$ is an exact copy of $\overline{EF}$, except that it is delayed by one full RCLK cycle with respect to EF.***

Also, since the usual enable signals $\overline{WEN}$ and $\overline{REN}$ have the wrong polarity to function properly in this "handclasp" mode, they are grounded for all devices within the cascade. ***The duplicate but inverted signals WEN2 and REN2 are used instead.***

$\overline{EF2}$, WEN2, and REN2 are available only in enhanced operating mode. They share the same pins which in standard operating mode are used respectively for $\overline{RXO}$, $\overline{WXI}$, and $\overline{RXI}$. Hence, for pipelined operation, all devices in the cascade must be in the enhanced operating mode; their $\overline{EMODE}$ control inputs must be grounded.

When all of the foregoing conditions have been met in the interconnection of the pipelined array, then: At each device-to-device interface boundary within the array, a data word is transferred from the upstream device to the downstream device after ***every*** transfer-clock rising edge, as long as the upstream device is not empty and the downstream device is not full.

There is one possible anomalous behavior, which can occur if at any time the device upstream from a FIFO-to-FIFO boundary ("device n – 1") becomes totally empty, at the same time as the downstream device ("device n") becomes totally full. Under these relatively infrequent conditions, one extra copy of the last word transferred out of device n – 1, which remains still available at the outputs of that device, gets introduced into the data stream. The simple circuit illustrated in Figure 29b avoids introducing this extra word and does not slow down the operation of the pipeline if it is implemented with logic which is sufficiently fast. Table 6 indicates the speed requirements for this circuit which correspond to the various speed grades of QS72215/25. If the infrequent introduction of such an extra word is not of concern for a given cascaded-QS72215/25 application, the circuit of Figure 29b may safely be omitted.

Two PLDs (programmable logic devices) suffice to implement the circuit of Figure 29b ten times, which allows for the cascading of QS72215/25s eleven deep. The choice of a GAL20RA10B-10 PLD to implement the flip-flop and the two AND gates at its inputs, and a GAL22V10C-5 PLD to implement the simple AND gate which follows the flip-flop, provides a sufficiently fast circuit to allow a cascade of QS72215/25-20 devices (the fastest speed grade presently offered by QSI) to operate with no speed degradation. Designers experienced in using PLDs may recognize other implementations.

The GAL20RA10B and GAL22V10C PLDs each provide ten macrocells. One macrocell may be configured to operate as a simple inverting or non-inverting buffer, a simple NAND or AND gate, an AND-OR gate, or a flip-flop with an AND-OR input structure. The GAL20RA10B macrocell architecture in particular supports the implementation of an asynchronous-set/reset clocked D flip-flop like the one shown in Figure 29b, except for some polarity differences at certain points within the logic diagram. If a slower implementation of the final AND gate can be tolerated in a given application, a single GAL20RA10B may be used to implement the circuit of

TABLE 6. REQUIRED EXTERNAL-LOGIC SPEEDS FOR PIPELINED DEPTH-CASCADING OPERATION AT MAXIMUM RATE OF SPEED GRADE.

	SPEED GRADE (Cycle Time)		
	20 ns	**25 ns**	**35 ns**
T_A[1]	≤ 8 ns	≤ 10 ns	≤ 15 ns
T_B[2]	≤ 15 ns	≤ 19 ns	≤ 28 ns

Notes:

1. T_A is the setup time for the signal "$\overline{FF}$ (Device n)," including the delay of the assertive-LOW AND gate, with respect to the clock.
2. T_B is the clock-to-output time for the signal "WEN2 (Device n)." including the delay of the assertive-HIGH AND gate.

Figure 29b five times, thus allowing for a cascade six FIFOs deep, with no second PLD being necessary. The GAL20RA10B and GAL22V10C PLDs are manufactured by Lattice Semiconductor Corporation, 5555 Northeast Moore Court, Hillsboro, OR 97124, USA.

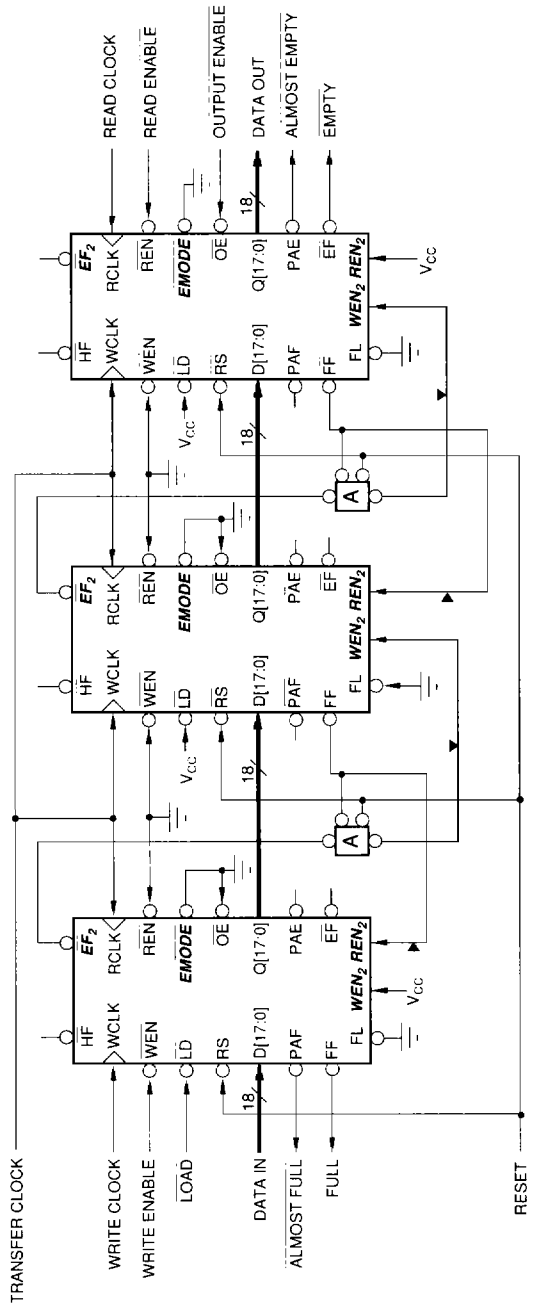
Width Expansion Along with Depth Cascading

In principle, width expansion may be used with either of the two possible depth-cascading schemes.

However, when using the token-passing depth-cascading scheme, width expansion reduces simply to placing two or more cascades in parallel. In this mode of interconnection, no architectural support is available for interlocked-paralleled operation. Composite-flag logic may, of course, be designed to fit any complete array configuration, to determine meaningful full and empty indications for the entire array. This logic may, for instance, OR the $\overline{FF}$ and $\overline{EF}$ signals from the devices at the same relative position in each of the paralleled cascades, and then AND all of the rank-$\overline{FF}$ signals together: and likewise for all of the rank-$\overline{EF}$ **signals. Then, the entire array is indicated to be full, if all ranks of devices (across the paralleled cascades) are individually full; and, similarly for empty.**

When using the pipelined depth-cascading scheme, on the other hand, the first rank of devices (the one which receives input data words from the external system) and the last rank of devices (the one which provides output data words to the external system) may be operated in an interlocked-paralleled manner. Figure 30 shows a suggested interconnection scheme for two paralleled cascades, each three devices deep. The entire array of Figure 30 would comprise a 3072 x 36 "effective FIFO," if implemented with 1024 x 18 QS72225 devices. Whenever the number of paralleled cascades exceeds two, a small amount of external logic is necessary to implement the interlocking.

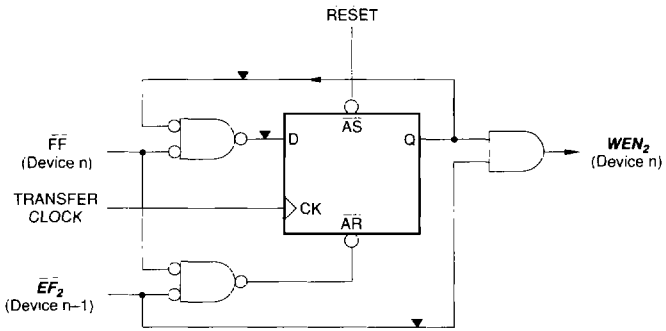
FIGURE 29a. TI-STYLE PIPELINED DEPTH-CASCADING



Notes:
1. The transfer clock may be any free-running clock. However, it is recommended that the faster of the write clock and the read clock be used, if both of these are free-running clocks.
2. Block "A" contains the circuit shown in Figure 29b.
BOLD ITALIC = Enhanced Operating Mode.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

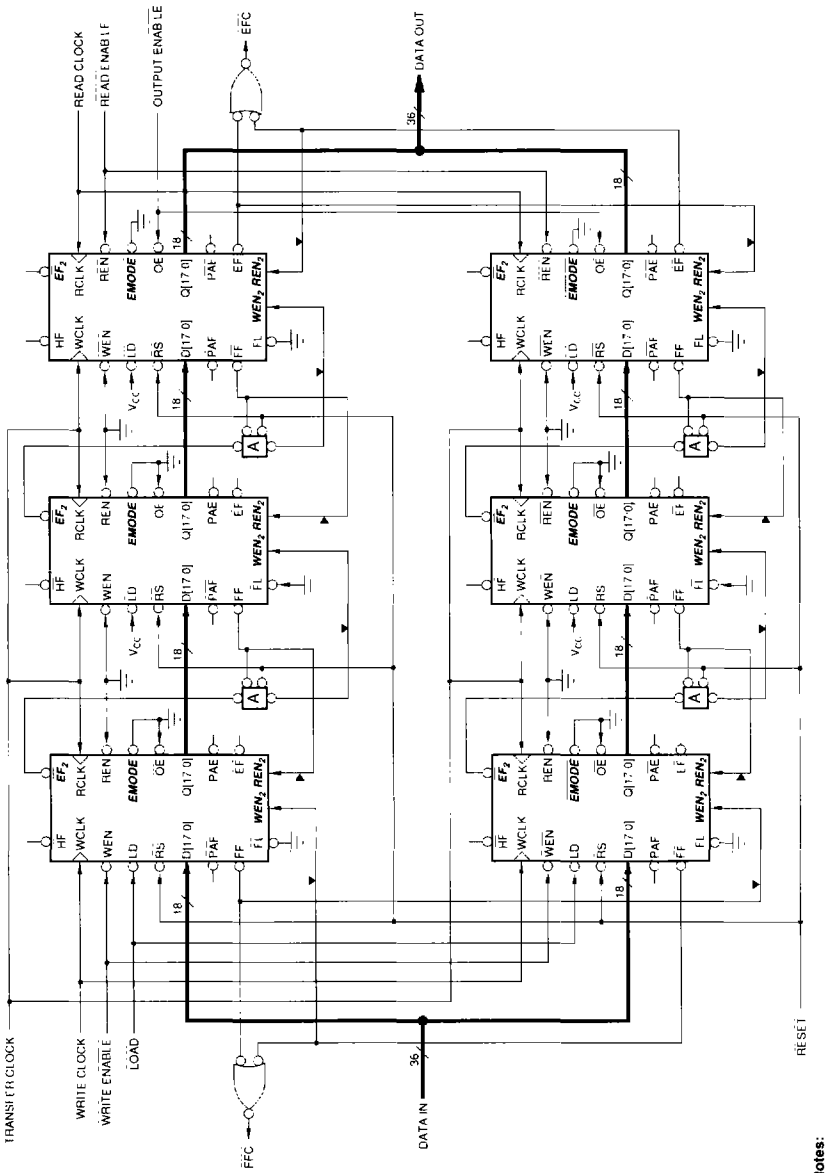
FIGURE 29b. EXTERNAL LOGIC NEEDED FOR TI-STYLE PIPELINED DEPTH-CASCADING



Notes:
1. $\overline{AS}$ sets Q=1 regardless of CK or D. (Asynchronous Set)
   $\overline{AR}$ sets Q=0 regardless of CK or D. (Asynchronous Reset)
2. Q=0 occurs if and only if device n–1 goes completely empty and device n goes completely full. Q=0 is maintained as long as these conditions persist.
3. This circuit is used as block "A" in Figure 29a and in Figure 30.

BOLD ITALIC = Enhanced Operating Mode.

FIGURE 30. INTERLOCKED PARALLELING USED TOGETHER WITH PIPELINED DEPTH-CASCADING



Notes:
1. The transfer clock may be any free-running clock. However, it is recommended that the faster of the write clock and the read clock 2 be used. If both of these are free running clocks.
2. Block "A" contains the circuit shown in Figure 29b

BOLD ITALIC = Enhanced Operating Mode.

BOLD ITALIC = ENHANCED OPERATING MODE
Standard Operating Mode = IDT-Compatible

ORDERING INFORMATION

Example: