High-Speed CMOS 2K x 36, 4K x 36 Clocked FIFO

QS723651
QS723661

FEATURES

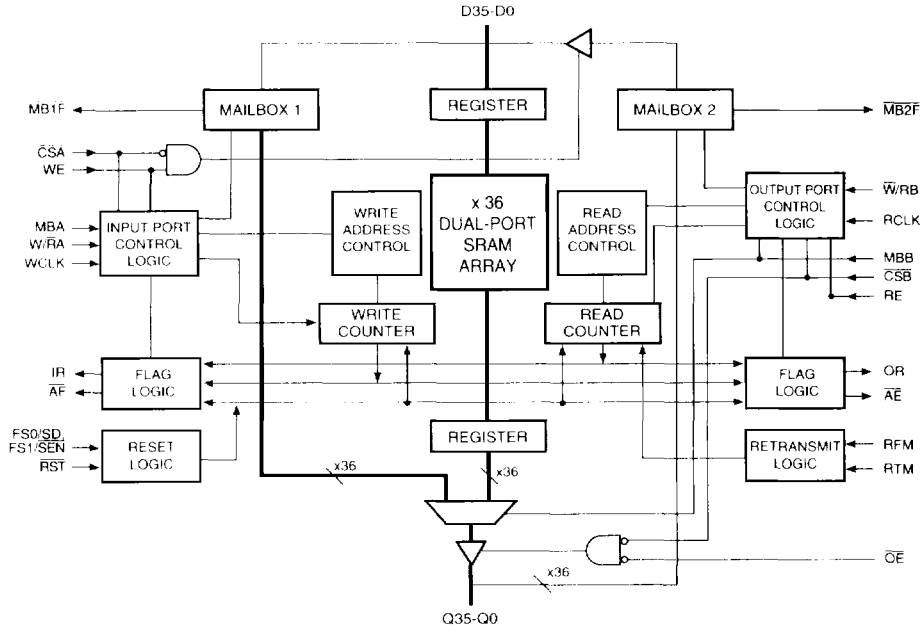
- Clocked interface 2K/4K x 36 FIFO
- Programmable Almost-Full and Empty flags
- Bi-directional mailbox registers
- Adjustable retransmit
- 8T cell for temperature and soft-error stability
- Fall-through architecture
- 40-MHz operating frequency
- Fast access times of 12 ns
- Metastable error-resistant flag logic
- Width expansion without additional logic
- Register-like outputs show current word in FIFO
- Available in 120-pin TQFP, 132-pin PQFP

DESCRIPTION

This 36-bit wide FIFO family is based on a high-performance 36-bit dual-ported memory core, and is the ideal solution for data-buffering needs, including data acquisition, multiprocessor interfaces, and digital communications buffering. The clocked interface allows direct interface to system clock signals without the need for complex wave shaping and external timing logic. Flag outputs are provided to indicate full, almost-full, almost-empty and empty status. The partial flags are programmable to any offset value. Other flags are provided to indicate when data is available in the bi-directional mailbox registers. Special care was taken in design to reduce the risk of metastability-induced flag errors. The QS7236x1 family uses multiple power and ground pins, output waveform control and input noise filters to dramatically reduce noise susceptibility and ground bounce. It is manufactured in the QCMOS™ process which features eight transistor memory cells for higher speed, lower power, radiation tolerance, soft-error resistance, process stability and performance linearity over a range of temperatures.

5

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

FIGURE 2. 120-PIN THIN QUAD FLAT PACK (TQFP) PINOUT

Counter-clockwise orientation, top view, 14mm square, 0.4mm pitch

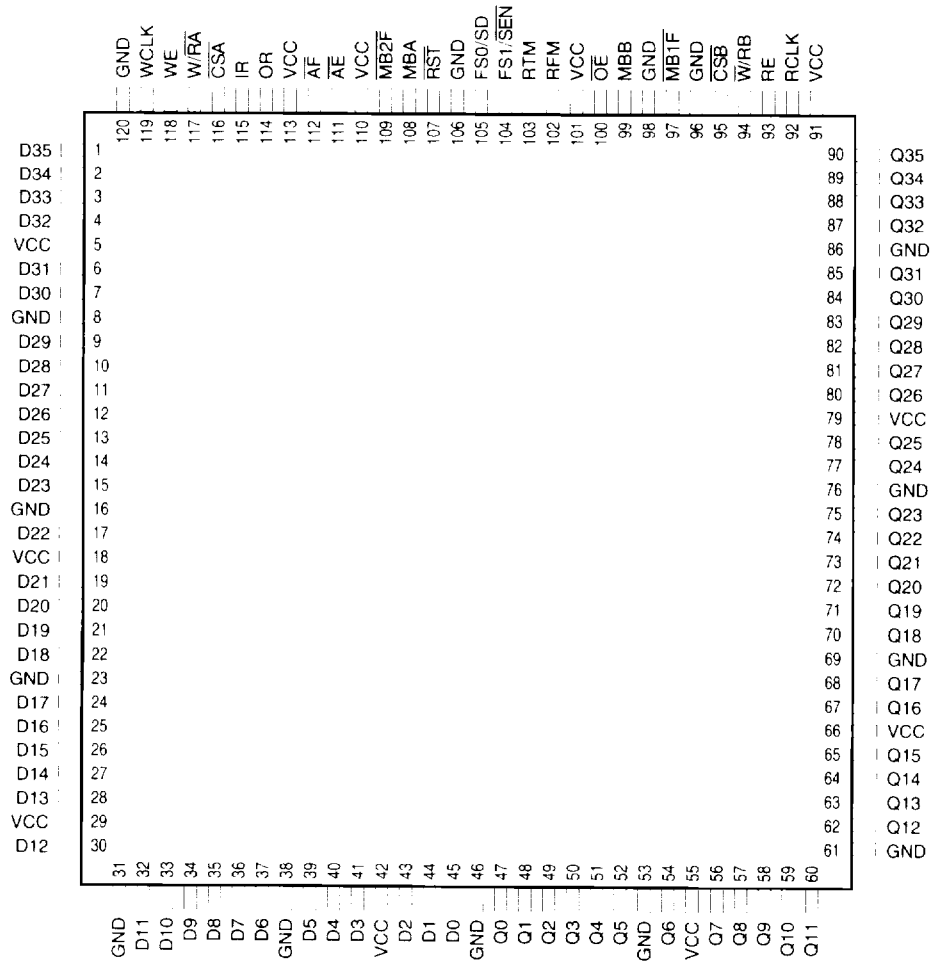
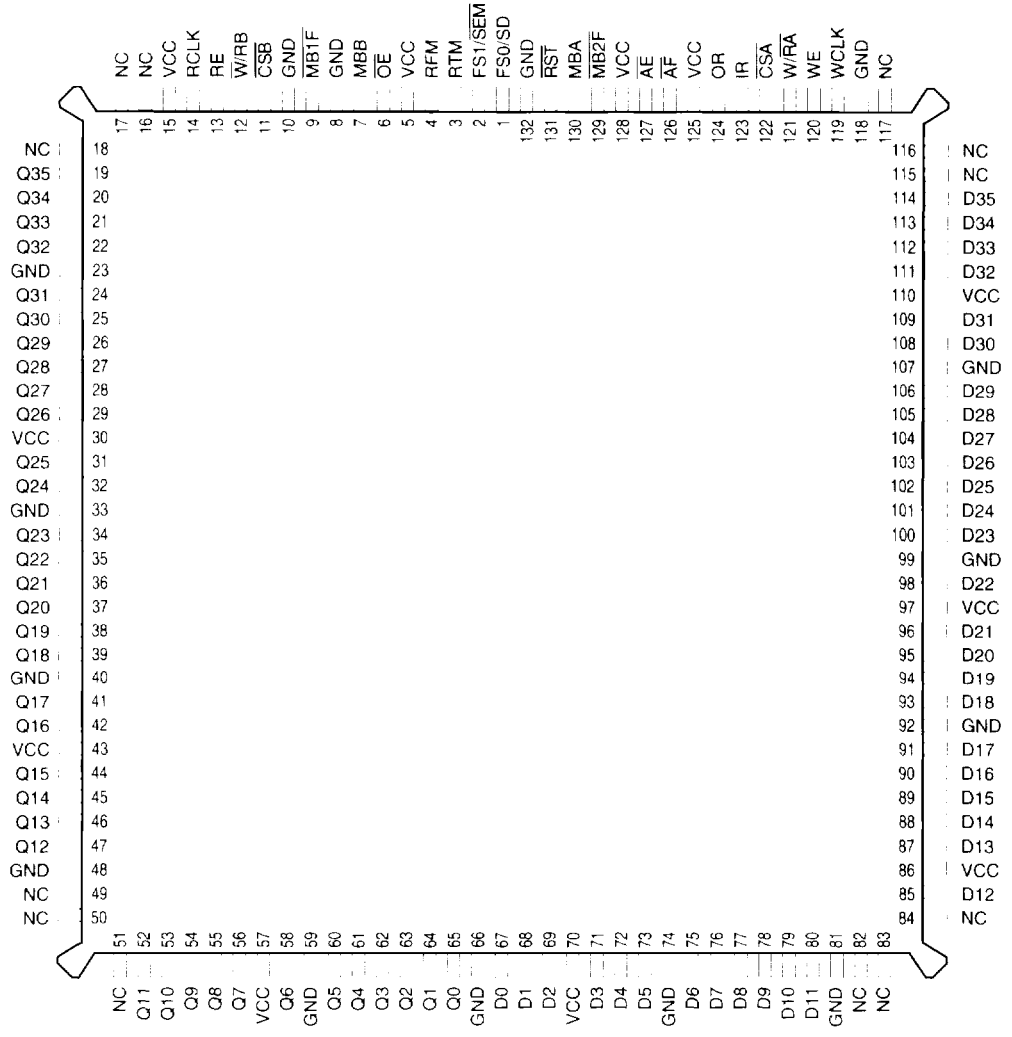


FIGURE 3. 132-PIN PLASTIC QUAD FLAT PACK (PQFP) PINOUT

Counter-clockwise orientation, top view, 1" square, 25-mil pitch



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PIN DESCRIPTION

Pin	Function	I/O	Ref	Description
D35-D0	Data Inputs	I/O	WCLK	36-bit write data port. Provides output for mailbox 2 and input for mailbox 1.
Q35-Q0	Data Outputs	I/O	RCLK	36-bit read data port. Provides output for mailbox 1 and input for mailbox 2.
WCLK	Write Clock	I	N/A	Clock input for write port for synchronizing all input (I) signals. IR and $\overline{AF}$ are synchronous on the rising edge.
RCLK	Read Clock	I	N/A	Clock input for read port for synchronizing all output (O) signals. OR and $\overline{AE}$ are synchronous on the rising edge.
RTM	Retransmit Mark	I	RCLK	Sets the position of the retransmit pointer. RTM HIGH, OR HIGH causes the current read location to be marked in anticipation of a retransmit operation. The retransmit mark is removed when RTM goes LOW during a RCLK rising edge.
RFM	Read from Mark	I	RCLK	Initiates the retransmit function. Causes initialization of the read pointer to the location set by RTM.
$\overline{OE}$	Output Enable	I	N/A	$\overline{OE}$ is an active LOW input. OE has only the effect of enabling or disabling data outputs Q35-Q0.
WE	Write Enable	I	WCLK	When HIGH, allows data to be written to D35-D0. If MBA is LOW, data will be written to the FIFO. MBA HIGH, WE HIGH will cause a write to mailbox 1. MBA HIGH, WE LOW will cause a read from mailbox 2.
RE	Read Enable	I	RCLK	When HIGH, allows data to be read from Q35-Q0. If RMB is LOW, the data will be read from the FIFO. MBB HIGH, RE HIGH causes a read from mailbox 1. MBB HIGH, RE LOW will cause a write to mailbox 2.
$\overline{CSA}$	Write Port Select	I	WCLK	Enables and disables WCLK, tri-states data port D when de-asserted.
$\overline{CSB}$	Read Chip Select	I	RCLK	Enables and disables RCLK, tri-states data port Q when de-asserted.
$\overline{MB1F}$ $\overline{MB2F}$	Mailbox Flags	O	WCLK RCLK	When LOW, indicates that mailbox data is available in the appropriate mailbox. When the flag is LOW (asserted), writing is inhibited.
$\overline{AF}$	Almost Full	O	WCLK	Provide a warning that the FIFO is approaching a full condition. $\overline{AF}$ and $\overline{AE}$ can be user programmed or set to default offset values at reset. When in retransmit mode, $\overline{AF}$ asserts with respect to the retransmit mark (which cannot be overwritten).
$\overline{AE}$	Almost Empty	O	RCLK	Provide a warning that the FIFO is approaching an empty condition.
FS1/$\overline{SEN}$ FS0/SD	Partial Flag Function Bits	I	WCLK	Used to select a default value or program a value of partial flag offset. $\overline{AE}$ and $\overline{AF}$ are independently programmable into storage registers.
OR	Output Ready	O	RCLK	Indicates when the FIFO is not empty and output data is valid. OR de-asserts when the FIFO becomes empty. When the FIFO becomes not-empty, OR will assert after a 3 RCLK cycle latency. OR LOW inhibits further read attempts.
IR	Input Ready	O	WCLK	Indicates when data can be written to the FIFO. IR de-asserts when the FIFO is full or when a retransmit mark is encountered. IR LOW inhibits further write attempts.
MBA	Write Port Mailbox Control	I	WCLK	When HIGH, selects mailbox mode. Writing to mailbox 1 or reading from mailbox 2 is controlled by WE.
MBB	Read Port Mailbox Control	I	RCLK	When HIGH, selects mailbox mode. Writing to mailbox 2 or reading from mailbox 1 is controlled by RE.
$\overline{RST}$	Reset	I	N/A	Resets both read and write pointers to array location zero. Causes IR, $\overline{AE}$ to assert and OR, $\overline{AF}$ flags to de-assert. $\overline{RST}$ must be LOW for at least 4 cycles.
W/$\overline{RA}$	Port A Write/Read	I	WCLK	A HIGH selects a write operation on the D_{IN} port and a LOW selects a read operation when WCLK transitions from LOW to HIGH.
$\overline{W}$/RB	Port B Write/Read	I	RCLK	A HIGH selects a read operation on the Q_{OUT} port and a LOW selects a write operation when RCLK transitions from LOW to HIGH.

Note:

Ref Column lists the appropriate clock signal for that input/output. Respective signal is synchronous to that clock.

OPERATIONAL DESCRIPTION

CLOCKED INTERFACE

All inputs and outputs of the QS7236X1 are synchronized to separate write port and read port clocks. These clocks can be operated by independent, free-running clock inputs or can be tied together. Input signals are required to be set-up and held for a specified interval in relation to the rising edge of the clock. Outputs are available with a known delay after the rising edge of the clock. Inputs and outputs are synchronized to a specific flag as defined in the Pin Description table. Both read and write clocks are gated by enable inputs.

READ AND WRITE OPERATION

D35-D0 will configure as active outputs (for mailbox 2) when both $\overline{CSA}$ and WE are LOW. Data is written to the FIFO on the LOW-to-HIGH WCLK transition when $\overline{CSA}$ is LOW, WE is HIGH, MBA is LOW, and the IR flag output is HIGH. The Q35-Q0 outputs are controlled by $\overline{CSB}$ and RE. When $\overline{CSB}$ is LOW and RE is HIGH, the outputs are active. The outputs will be HIGH-Z if $\overline{CSB}$ is HIGH or RE is LOW. Data is read from the FIFO main array on the LOW-to-HIGH transition of RCLK when $\overline{CSB}$ is LOW, RE is HIGH, MBB is LOW, and the OR output flag is HIGH.

POINTERS AND COUNTERS

The QS7236X1 uses two internal counters to control the addresses of the memory array during write and read operations. These counters are also referred to as "pointers." When a 36-bit data word is written to the device, the write counter is incremented. When data is read from the device, the read pointer is incremented. The third address pointer is the retransmit mark which is set by the RTM pin. The retransmit mark is not a counter, but is used to load the read counter during retransmit operations. See "Retransmitting" for more information. Writing to or reading from the mailbox registers does not affect the pointer values.

5

READ AND WRITE OPERATION

Read/Write Functions for Write Port

	Inputs					Flags after Clock				
Mode	**W/$\overline{RA}$**	**$\overline{CSA}$**	**WE**	**WCLK**	**MBA**	**$\overline{MB1F}$**	**$\overline{MB2F}$**	**OR**	**IR**	**Outputs**
Mailbox 2 Output Sel.	0	0	0	X	1	–	–	–	–	Mailbox 2 Register
Read Mailbox 2	0	0	1	↑	1	–	↑	–	–	Mailbox 2 Register
FIFO Write Operation	1	0	1	↑	0	–	–	–	1	HIGH-Z
Write to Mailbox 1	1	0	1	↑	1	↓	–	–	–	HIGH-Z
Hold, No Operation	1	0	0	X	X	–	–	–	–	HIGH-Z
Hold, No Operation	X	1	X	X	X	–	–	–	–	HIGH-Z

Read/Write Functions for Read Port

	Inputs					Flags after Clock				
Mode	**$\overline{W}$/RB**	**$\overline{CSB}$**	**RE**	**RCLK**	**MBB**	**$\overline{MB1F}$**	**$\overline{MB2F}$**	**OR**	**IR**	**Outputs**
Mailbox 1 Output Sel.	1	0	1	X	1	–	–	–	–	Mailbox 1 Register
Read Mailbox 1	1	0	1	↑	1	↑	–	–	–	Mailbox 1 Register
Read Operation	1	0	1	↑	0	–	1	–	–	Active, FIFO Output
Write to Mailbox 2	0	0	1	↑	1	–	↓	–	–	HIGH-Z
Hold, No Operation	0	0	0	X	X	–	–	–	–	HIGH-Z
Hold, No Operation	X	1	X	X	X	–	–	–	–	HIGH-Z
Hold, No Operation	0	0	1	↑	L	–	–	–	–	HIGH-Z

SERIAL LOAD

PARTIAL FLAG PROGRAMMING TABLE

FS1	FS0	$\overline{RST}$	$\overline{AE}$, $\overline{AF}$ Offset
1	1	↑	Serial Load
1	0	↑	8
0	1	↑	16
0	0	↑	Parallel load from D11-D0

PROGRAMMABLE PARTIAL FLAGS

Partial flags are available to provide the user with a warning that the FIFO is nearing a full or empty condition. The offset of these flags is individually programmable during the reset operation to one of two fixed values (8 or 16 words) or to an arbitrary value between 0 and 2047 (QS723651) or 0 and 4095 (QS723661) set by the user. At the rising edge of $\overline{RST}$, FS0/SD and FS1/$\overline{SEN}$ are asserted to select either a predetermined fixed offset or a programmable offset. If FS0/SD and FS1/$\overline{SEN}$ are specified as 00, the first write to the FIFO programs the $\overline{AF}$ offset, and the second write programs the $\overline{AE}$ offset. The third write to the FIFO stores the first data word to the device. Because a maximum offset value of 2K (2048) or 4K (4096) for the QS723651 and QS723661, respectively, is allowed, only the 11 LSBs are relevant for the QS723651 and 12 LSBs for the QS723661. Therefore, D35-D12 can be ignored during offset programming. For more information on the flag status inputs, see the "Flag Programming" table above. To program the X and Y registers serially, the device is reset with FS0/SD and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of $\overline{RST}$. After this reset is complete, the X and Y register values are loaded bitwise through the FS0/SD input on each LOW-to-HIGH transition of WCLK that the FS1/$\overline{SEN}$ input is LOW. To complete the programming for the QS723651 and QS723661, 22-bit or 24-bit writes are needed, respectively. The first-bit write stores the most significant bit of the Y register, and the last-bit write stores the least significant bit of the X register. Each register value can be programmed from 0 to 2047 (QS723651), or 0 to 4095 (QS723661).

When the option to program the offset registers serially is chosen, the input-ready (IR) flag remains LOW until all 22 or 24 bits are written. The IR flag is set HIGH by the LOW-to-HIGH transition of WCLK after the last bit is loaded to allow normal FIFO operation.

OUTPUT-READY FLAG (OR)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array (RCLK). When the output-ready flag is HIGH, new data is present in the FIFO output register. When the output-ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty + 1, or empty + 2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of RCLK. Therefore, an output-ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three RCLK cycles have not elapsed since the time the word was written. The output-ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of RCLK occurs, simultaneously forcing the output-ready flag HIGH and shifting the word to the FIFO output register.

A LOW-to-HIGH transition on RCLK begins the first synchronization cycle of a write if the clock transition occurs at time $t_{SK(1)}$ or greater after the write. Otherwise, the subsequent RCLK cycle may be the first synchronization cycle.

INPUT-READY FLAG (IR)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array (WCLK). When the input-ready flag is HIGH, a memory location is free in the SRAM to write new data. No memory locations are free when the input-ready flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full – 1, or full – 2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of WCLK. Therefore, an input-ready flag is LOW if less than two cycles of WCLK have elapsed since the next memory-write location has been read. The second LOW-to-HIGH transition on WCLK after the read sets the input-ready flag HIGH, and data can be written in the following cycle.

A LOW-to-HIGH transition on WCLK begins the first synchronization cycle of a read if the clock transition occurs at time t_{SK1} or greater after the read. Otherwise, the subsequent WCLK cycle may be the first synchronization.

ALMOST-EMPTY FLAG ($\overline{AE}$)

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array (RCLK). The state machine that controls an Almost-Empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost-empty, almost-empty + 1, or almost-empty + 2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming above). The Almost-Empty flag is LOW when the FIFO contains X or less words and is HIGH when the FIFO contains X + 1 or more words. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of RCLK are required after a FIFO write for the Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing X + 1 or more words remains LOW if two cycles of RCLK have not elapsed since the write that filled the memory to the X + 1 level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of RCLK after the FIFO write that fills memory to the X + 1 level.

ALMOST-FULL FLAG ($\overline{AF}$)

The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array (WCLK). The state machine that controls an Almost-Full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost-full, almost-full – 1, or almost-full – 2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming above). The Almost-Full flag is LOW when the number of words in the FIFO is greater than 2048 – Y for the QS723651 and 4096 – Y, for the QS723661. The Almost-Full flag is HIGH when the number of words in the FIFO is less than or equal to 2048 – (Y + 1) for the QS723651 and 4096 – (Y + 1) for the QS723661. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of WCLK are required after a FIFO read for its Almost-Full flag to reflect the new number of words. Therefore, the Almost-Full flag of a FIFO containing 2048 – (Y + 1) (QS723651) or 4096 – (Y + 1) (QS723661) or less words remains LOW if two cycles of WCLK have not elapsed since the read that reduced the number of words in memory to 2048/4096 – (Y + 1). An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of WCLK after the FIFO read that reduces the number of words in memory to 2048/4096 – (Y + 1). A LOW-to-HIGH transition of WCLK begins the first synchronization cycle if it occurs at time t_{SK2} or greater after the read that reduces the number of words in memory to 2048/4096 – (Y + 1). Otherwise, the subsequent WCLK cycle may be the first synchronization cycle.

SYNCHRONOUS RETRANSMIT

The synchronous retransmit feature of the QS723651/61 allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode to select a beginning word and prevent ongoing FIFO write operations from destroying retransmit data. Data vectors with a *minimum length three words* can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a LOW-to-HIGH transition on RCLK when the retransmit mode (RTM) input is HIGH and OR is HIGH. This rising RCLK edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a LOW-to-HIGH transition occurs while RTM is LOW.

When two or more reads have been done past the initial retransmit word, a retransmit is initiated by a LOW-to-HIGH transition on RCLK when the read-from-mark (RFM) input is HIGH. This rising RCLK edge shifts the first retransmit word to the FIFO output register, and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be LOW during the RCLK rising edge that takes the FIFO out of retransmit mode.

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO output register and used by the OR and $\overline{AE}$ flags. The shadow read pointer stores the SRAM location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer is used by the IR and $\overline{AF}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{AF}$ is set LOW by the write that stores 2048 – Y or 4096 – Y words after the first retransmit word for the QS723651/61, respectively. The IR flag is set LOW by the 2048th or 4096th write after the first retransmit word for the QS723651 or QS723661.

The data-out control signals are identical to those of the data-in port with the exception that the data-out write/read select (W/RB) is the inverse of the data-in write/read select ($W/\overline{R}_A$). The state of the data-out data (Q35-Q0) outputs is controlled by the data-out chip select ($\overline{CSB}$) and the data-out write/read select ($\overline{W}/R_B$). The Q35-Q0 outputs are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}/R_B$ is LOW. The Q35-Q0 outputs are active when $\overline{CSB}$ is LOW and $\overline{W}/R_B$ is HIGH.

Data is read from the FIFO to its output register on a LOW-to-HIGH transition of RCLK when $\overline{CSB}$ is LOW, W/RB is HIGH, the data-out enable (RE) is HIGH, the data-out mailbox select (MBx) is LOW, and the output-ready (OR) flag is HIGH (see "Read and Write Operations" table, p.2-7). Reads from the FIFO are independent of any concurrent FIFO writes.

When the FIFO is in retransmit mode and RFM is HIGH, a rising RCLK edge loads the current read pointer with the shadow read-pointer value and the OR and $\overline{AE}$ flags reflect the new level of fill immediately. The rising RCLK edge that takes the FIFO out of retransmit mode shifts the read pointer used by the IR and $\overline{AF}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{AF}$ should cause one or both flags to transition HIGH, at least two WCLK synchronizing cycles are needed before the flag the change. A rising WCLK edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time t_{SK1} or greater after the rising RCLK edge. A rising WCLK edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{AF}$ if it occurs at time t_{SK2} or greater after the rising RCLK edge. The retransmit feature does not function when the device is being used for depth expansion.

MAILBOX REGISTERS

The QS7236X1 features a bi-directional mailbox, which is especially useful for handshaking during data transfer. A typical application for the mailbox is for inter-CPU transmission in a multiprocessing system. Two 36-bit bypass registers are on the QS723651/61 to pass command-and-control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on WCLK writes D35-D0 data to the Mail1 register when a data-in write is selected by $\overline{CSA}$, W/$\overline{R}_A$, and WE with MBA HIGH. A LOW-to-HIGH transition on RCLK writes Q0-Q35 data to the Mail2 register when a data-out write is selected by $\overline{CSB}$, $\overline{W}/R_B$, and RE with MBB HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MB1F}$ or $\overline{MB2F}$) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the data-out data (Q35-Q0) outputs are active, the data on the bus comes from the FIFO output register when the data-out mailbox select (MBB) input is LOW and from the Mail1 register when MBB is HIGH. Mail 2 data is always present on the data-in data (D35-D0) outputs when they are active. The Mail1 register flag ($\overline{MB1F}$) is set HIGH by a LOW-to-HIGH transition on RCLK when a data-out read is selected by $\overline{CSB}$, $\overline{W}/R_B$, and RE with MBB HIGH. The Mail2 register flag ($\overline{MB2F}$) is set HIGH by a LOW-to-HIGH transition on WCLK when a data-in read is selected by $\overline{CSA}$, W/$\overline{R}_A$, and WE with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

FIXED FLAGS

Input ready (IR) and output ready (OR) flags indicate when the FIFO has reached a boundary. De-assertion of IR occurs when the write pointer has reached a position 2K (QS723651) or 4K (QS723661) words away from the read pointer (a full condition). Writing is subsequently disabled regardless of the state of the write controls. IR is synchronized to the write clock and de-asserts in the same clock cycle as the last write operation. If the read pointer is incremented as the result of a read, then IR will reassert. Because read operations are synchronized to a different clock than that of the Full flag, a metastability hazard could result when the internal flag logic decides a value. Consequently, the design of the IR flag circuitry uses a two-stage, metastable-resistant assertion circuit. This causes assertion two write clock cycles after the read clock.

The output ready flag, when asserted, indicates when the FIFO is not empty and reading is allowed. When the read pointer "catches up to" the write pointer and their addresses coincide, OR will de-assert within the same read cycle (an empty condition). Once this happens, further reads are inhibited. Like the input ready flag, the output ready flag asserts within three cycles. Once the last word is read from the FIFO and OR de-asserts, that word will remain on the outputs until new data is written to the FIFO and the flag asserts.

In addition to input- and output-ready flags, mailbox flags ($\overline{MB1F}$, $\overline{MB2F}$) are used to indicate that new data has been loaded into a 36-bit mailbox register. Once the mailbox data is read and the flag de-asserts, the data remains intact until new data is written to the register.

RESET

The /RST pin resets the FIFO by zeroing the write, read and mark pointers, and clearing the mailbox flags. The reset function will not reset any register contents. $\overline{RST}$ must be held LOW for four write clock and four read clock cycles. On the rising edge of the reset pulse, inputs FS1-FS0 are asserted to select partial flag offset mode. Note FS0/SD and FS1/$\overline{SEN}$ should be set-up and held with respect to the reset pulse edge, not a clock edge. When $\overline{RST}$ is asserted, IR, OR, and $\overline{AE}$ go LOW, while $\overline{AF}$ goes HIGH. After a single clock cycle flag latency, IR will assert, allowing programming of the partial flags (described above).

OUTPUT ENABLE

$\overline{OE}$ is an assertive-LOW, overriding output enable. $\overline{OE}$ has only the effect of enabling or disabling data outputs Q35-Q0. When Q35-Q0 are enabled, each of these 36 data outputs is in a normal HIGH or LOW state, according to the bit pattern of the data word in the output register. When Q35-Q0 are disabled, each of these outputs is tri-stated regardless of the state of the other pins.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min	Max
V_{CC}	Supply Voltage	4.5V	5.5V
GND	Ground	0V	0V
T_A	Ambient Operating Temperature	0°C	+70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	−0.5 to 7.0V
DC Output Voltage V_{OUT}	−0.5 to Vcc +0.5V
DC Input Voltage V_{IN}	−0.5 to Vcc +0.5V
AC Input Voltage (Pulse Width ≤ 20ns)	-3.0V
DC Input Diode Current with V_{IN} < 0	-20 mA
DC Output Diode Current with V_{OUT} < 0	-50 mA
DC Output Current with V_{OUT} > V_{CC}	50 mA
DC Output Current Max Sink Current/Pin	70 mA
DC Output Current Max Source Current/Pin	−30 mA
Total DC Ground Current	(NxI_{OL} + MxΔ Icc) mA
Total Dc V_{CC} Power Supply Current	(NxI_{OH} + MxΔ Icc) mA
N = Number of Outputs, M = Number of Inputs	
Maximum Power Dissipation	1.5 Watts
T_{STG} StorageTemperature	−65°C to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device, resulting in functional- or reliability-type failures.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage		2.0	–	V
V_{IL}	Input LOW Voltage		–	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −4 mA, V_{CC} = 4.5V	2.4	–	V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA, V_{CC} = 4.5V	–	0.4	V
$\lvert I_{OZ} \rvert$	Output Leakage	V_{CC} = 5.5V, V_{OUT} = V_{CC} or 0V	–	10	µA
$\lvert I_{IL} \rvert$	Input Leakage	V_{CC} = 5.5V, GND < V_{IN} < V_{CC}	–	10	µA

Note: Transient inputs with V_{IL} not more negative than −1.5V are permitted for pulse widths < 10 ns.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz TQFP (TF) package

Name	Description	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz	4	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1 MHz	8	10	pF

Note: Capacitance is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS QS723661

Symbol	Parameter	Speed (ns) -25	-30	-40	Units
I_{CC1}	Operating Current Vcc = Max, Outputs Open	200	180	175	mA
I_{CC2}	TTL Standby Current $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0, $\overline{CSB}$ = 1, $\overline{CSA}$ = 1	25	25	25	mA
I_{CC3}	CMOS Standby Current $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, $\overline{CSB}$ = 1, $\overline{CSA}$ = 1	15	15	15	mA

POWER SUPPLY CHARACTERISTICS QS723651

Symbol	Parameter	Speed (ns) -25	-30	-40	Units
I_{CC1}	Operating Current Vcc = Max, Outputs Open	200	175	170	mA
I_{CC2}	TTL Standby Current $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0, $\overline{CSB}$ = 1, $\overline{CSA}$ = 1	25	25	25	mA
I_{CC3}	CMOS Standby Current $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, $\overline{CSB}$ = 1, $\overline{CSA}$ = 1	15	15	15	mA

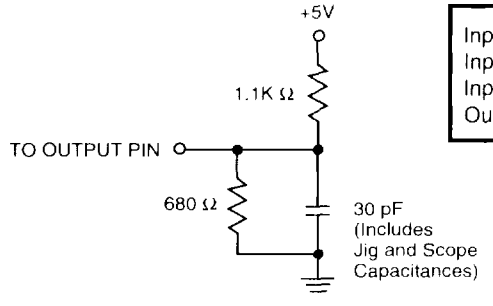
SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

Symbol	Parameter		-25	-30	-40	Units	Type
f_C	Read or Write Frequency[2]		40	33.3	25	MHz	Min
t_{TC}	Read or Write Cycle Time		25	30	40	ns	Min
t_{CWH}	Write Clock Time	HIGH	12	15	16	ns	Min
t_{CWL}		LOW	12	15	16		
t_{CRH}	Read Clock Time	HIGH	12	15	16	ns	Min
t_{CRL}		LOW	12	15	16		
t_A	RAM Access Time		12	15	17	ns	Min
t_S	Enable, Write Data Setup Time		5	6	8	ns	Min
t_H	Enable, Write Data Hold Time		0	0	0	ns	Min
t_{CF}	Clock to Flag Output Delay		14	15	16	ns	Min
t_{CD}	Clock to Data Output Delay		14	15	16	ns	Max
t_{OH}	Output Hold from Clock		0	0	0	ns	Max
t_{RSTH}	$\overline{RST}$ Hold From Last Reset Cycle Clock[4]		6	7	8	ns	Max
t_{HZ}	Output Disable Time		12	14	15	ns	Max
t_{LZ}	Output to LOW-Z Time		2	2	2	ns	Min
t_{DOE}	Output Enable to Data Valid		12	14	15	ns	Max
t_{SK1}	WCLK to RCLK Flag and Data Latency[3] (OR, IR, Q35-Q0)		9	10	11	ns	Min
t_{SK2}	WCLK to RCLK Partial Flag Latency[3] ($\overline{AF}$, $\overline{AE}$)		18	20	22	ns	Min
t_{RST}	$\overline{RST}$ LOW to Flags Valid		22	25	27	ns	Max

Notes: These timing parameters are measured as defined in AC TEST CONDITIONS.

1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested.
3. t_{SK1} and t_{SK2} are not operational constraints. They indicate that if violated, flags and data will be delayed until the next RCLK edge. If reading from a previously empty FIFO, normal latency is three RCLK cycles. If t_{SK1} is violated, data and OR may not assert until the 4th RCLK edge.
4. See timing diagram. The reset cycle requires four RCLKs and four WCLKs. t_{RSTH} applies to the last appropriate clock edge.

FIGURE 4. AC TEST CONDITIONS



Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

TIMING DIAGRAMS

FIGURE 5. FIFO WRITE CYCLE TIMING

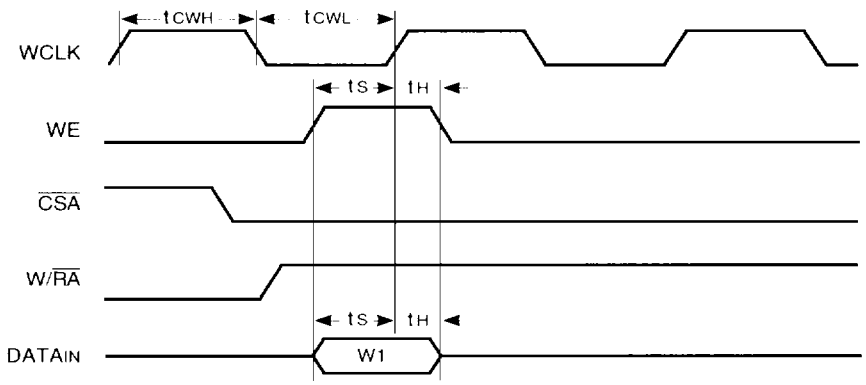
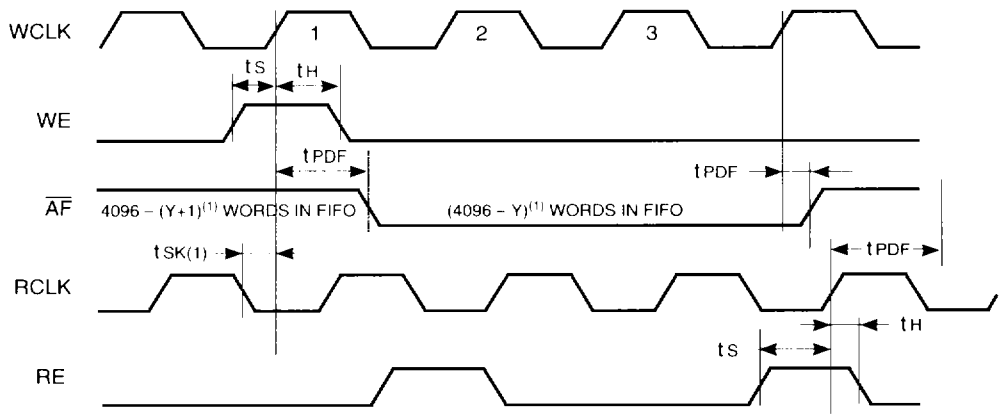


FIGURE 6. FIFO TIMING $\overline{AF}$ WHEN FIFO IS ALMOST FULL

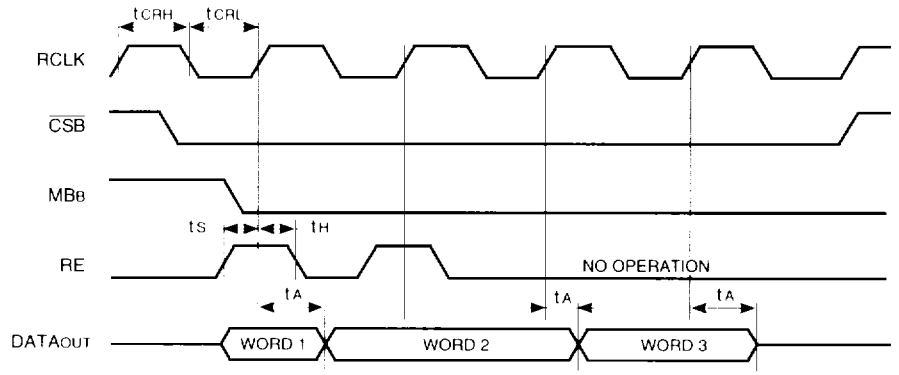


Notes:

1. 4096 for the 723661, 4K x 36
   2048 fo rthe 723651, 2K x 36
2. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L),
   FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L).
3. $t_{SK(1)}$ is the minimum time between a falling RCLK edge and a rising WCLK edge for IR to transition HIGH in the next WCLK cycle. If the time between the falling RCLK and the rising WCLK edge is less than $t_{SK(1)}$, then IR can transition HIGH one WCLK cycle later.

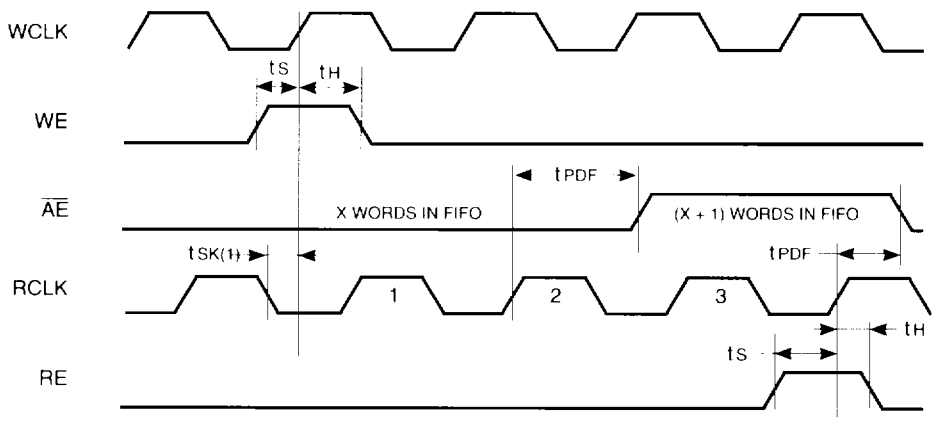
PARTIAL FLAG TIMING

FIGURE 7. FIFO READ CYCLE TIMING



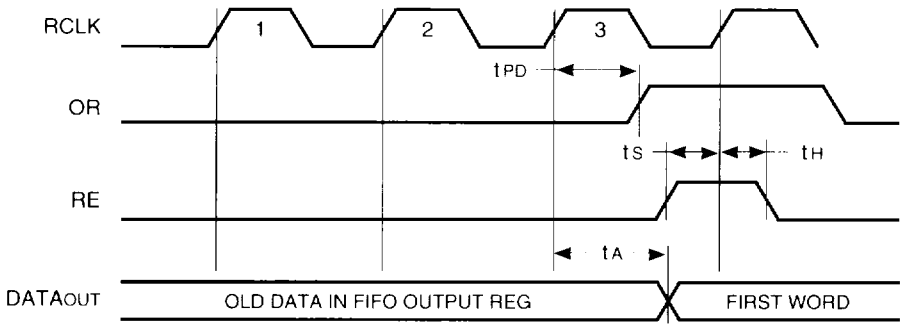
Note:
$\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L.

FIGURE 8. TIMING FOR $\overline{AE}$ WHEN FIFO IS ALMOST EMPTY



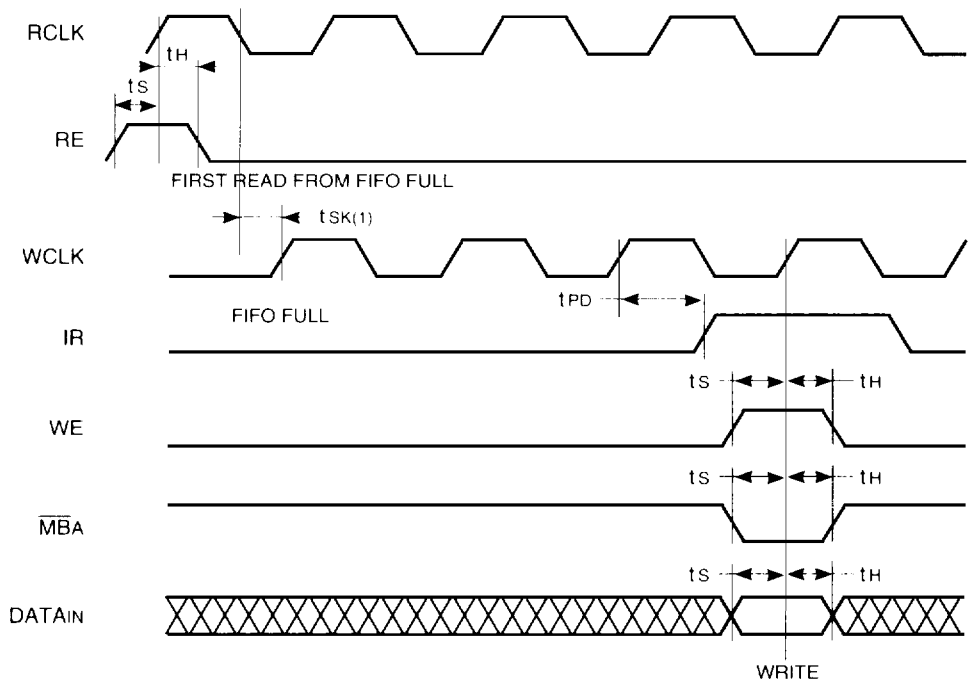
Notes:
1. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L).
   FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L).
2. $t_{SK(1)}$ is the minimum time between a falling RCLK edge and a rising WCLK edge for IR to transition high in the next WCLK cycle. If the time between the falling RCLK and the rising WCLK edge is less than $t_{SK(1)}$, then IR can transition high one WCLK cycle later.

FIGURE 9. OUTPUT READY FLAG (OR) AND FIRST DATA FALL THROUGH WHEN FIFO IS EMPTY



Note: Assumes one data word has already been written in.

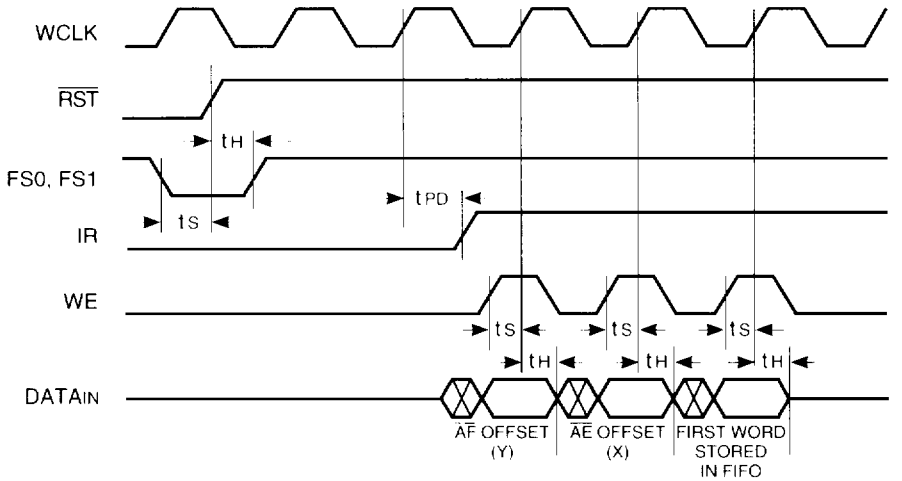
FIGURE 10. INPUT READY (IR) FLAG TIMING AND FIRST AVAILABLE WRITE WHEN FIFO IS FULL



Note:

$t_{SK(1)}$ is the minimum time between a falling RCLK edge and a rising WCLK edge for IR to transition high in the next WCLK cycle. If the time between the falling RCLK and the rising WCLK edge is less than $t_{SK(1)}$, then IR can transition high one WCLK cycle later.

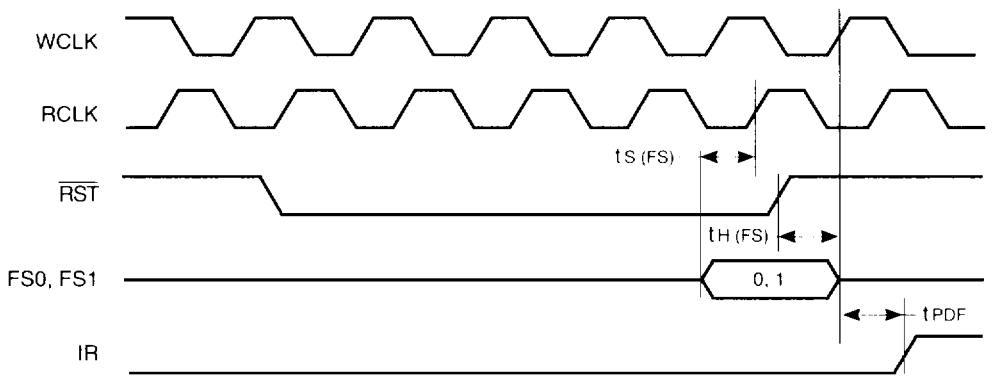
FIGURE 11. PROGRAMMING THE PARTIAL FLAGS ($\overline{AF}$ AND $\overline{AE}$) OFFSET VALUES FROM PORT A



Notes:

1. $\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L.
2. It is necessary to program the offset register on consecutive clock cycles and at the first clock cycle after IR goes high.

FIGURE 12. FIFO RESET PROGRAMMING OF THE PARTIAL FLAGS OF THE PRESET VALUE OF EIGHT

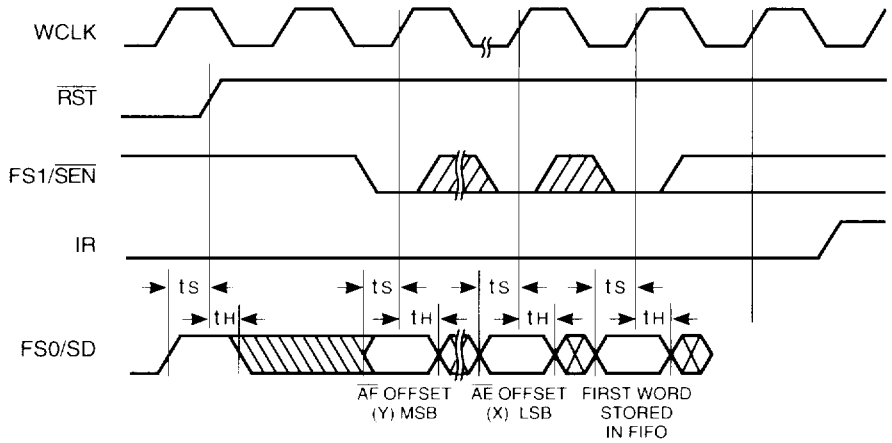


Note:

$\overline{AF}$ = H, $\overline{AE}$ = L, OR = L.

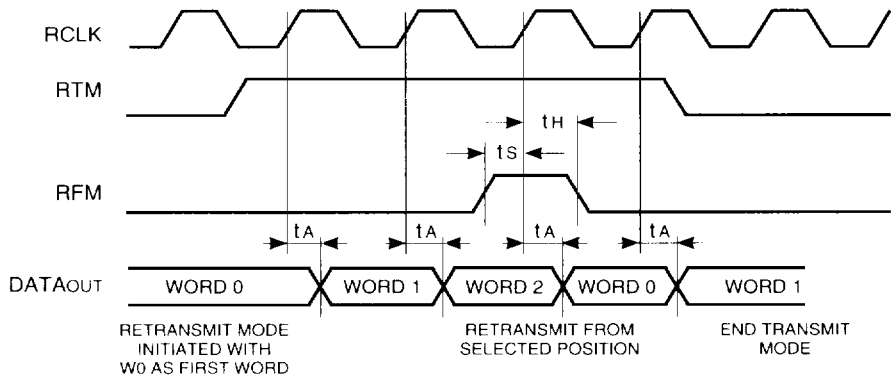
$\overline{MBF1}$ and $\overline{MBF2}$ = H after reset state.

FIGURE 13. PROGRAMMING THE PARTIAL FLAGS ($\overline{AF}$ AND $\overline{AE}$) VIA THE SERIAL PORT



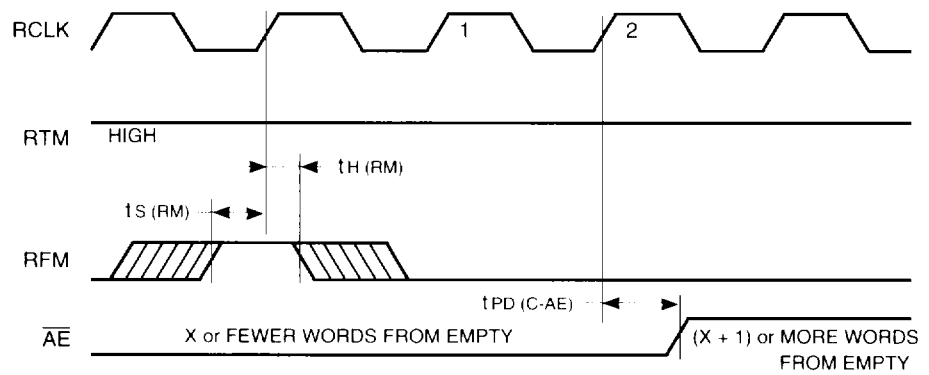
5

FIGURE 14. RETRANSMIT SHOWING MINIMUM RETRANSMIT LENGTH



Note:
$\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L.

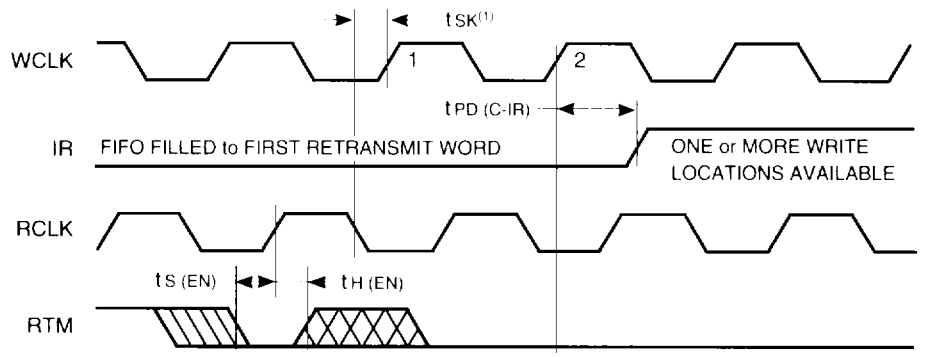
FIGURE 15. $\overline{AE}$ MAXIMUM LATENCY WHEN RETRANSMIT INCREASES THE NUMBER OF STORED WORDS ABOVE X



Note:

X is the value loaded in the almost-empty flag offset register.

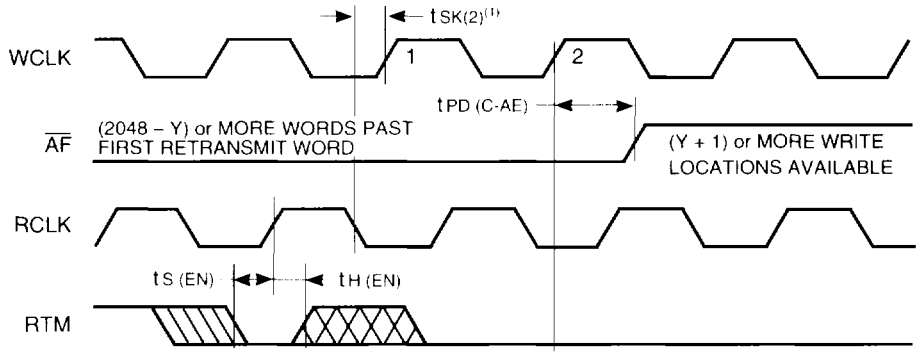
FIGURE 16. IR TIMING FROM THE END OF RETRANSMIT MODE WHEN ONE OR MORE WRITE LOCATIONS ARE AVAILABLE



Note:

1. $t_{SK(2)}$ is the minimum time between a falling RCLK edge and a rising WCLK edge for IR to transition HIGH in the next WCLK cycle. If the time between the falling RCLK edge and rising WCLK edge is less than $t_{SK(2)}$, then IR can transition HIGH one WCLK cycle later than shown.

FIGURE 17. $\overline{AF}$ TIMING FROM THE END OF RETRANSMIT MODE WHEN (Y + 1) OR MORE WRITE LOCATIONS ARE AVAILABLE



Note:

1. $t_{SK(2)}$ is the minimum time between a falling RCLK edge and a rising WCLK edge for $\overline{AF}$ to transition HIGH in the next WCLK cycle. If the time between the falling RCLK edge and rising WCLK edge is less than $t_{SK(2)}$, then $\overline{AF}$ can transition HIGH one WCLK cycle later than shown.

5

FIGURE 18. TIMING FOR MAIL 1 REGISTER AND $\overline{\text{MBF1}}$ FLAG

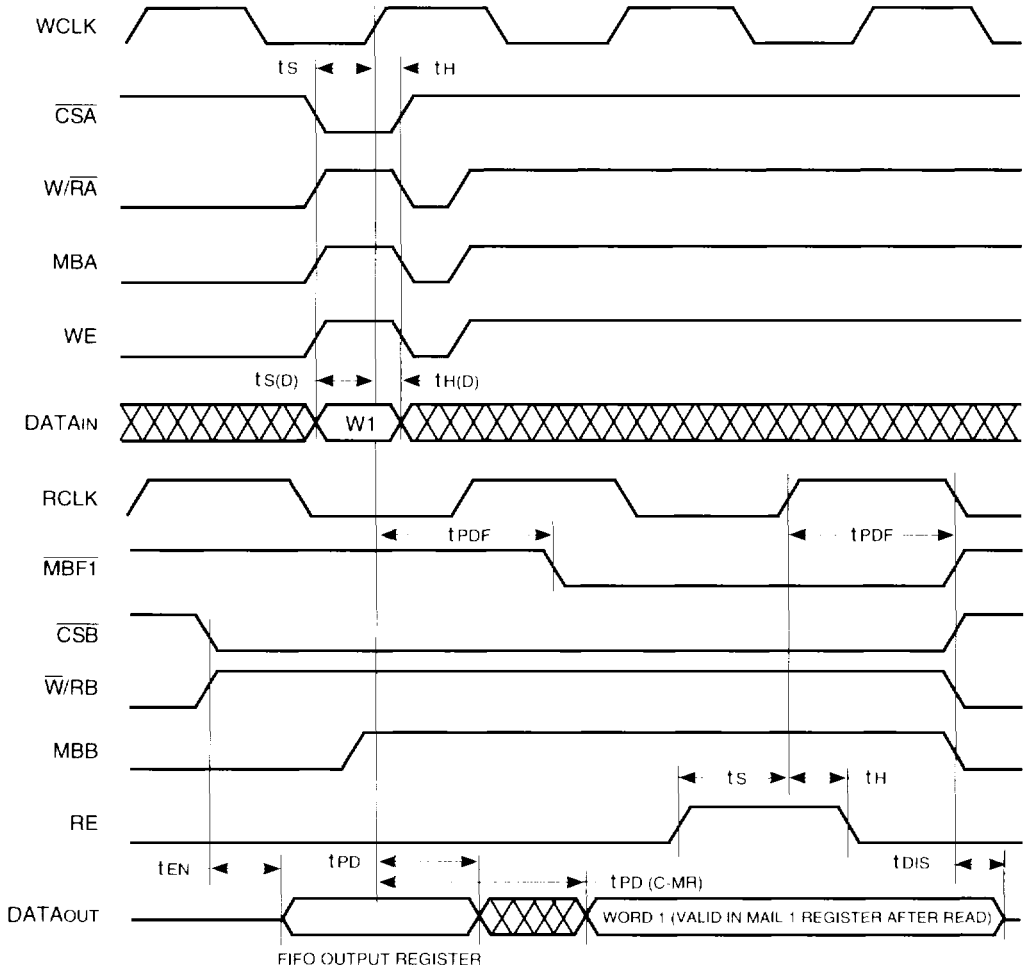
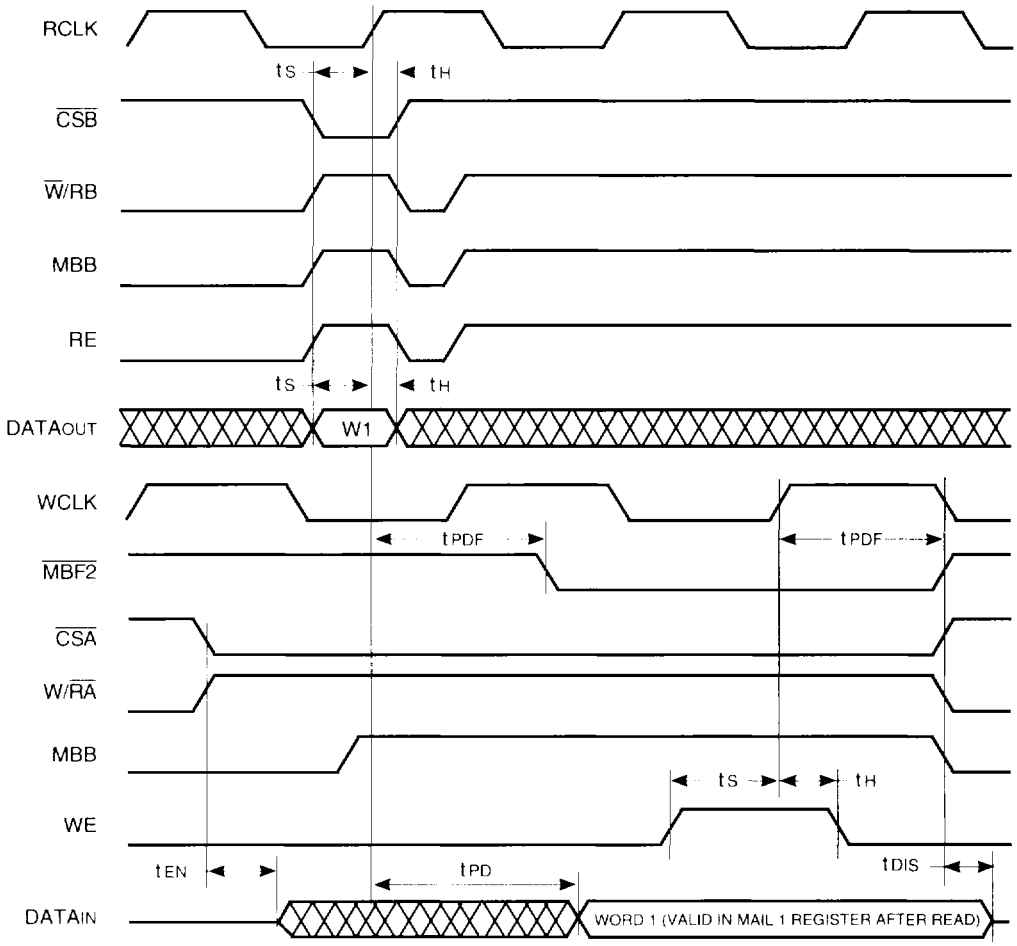


FIGURE 19. TIMING FOR MAIL 2 REGISTER AND $\overline{MBF2}$ FLAG



5

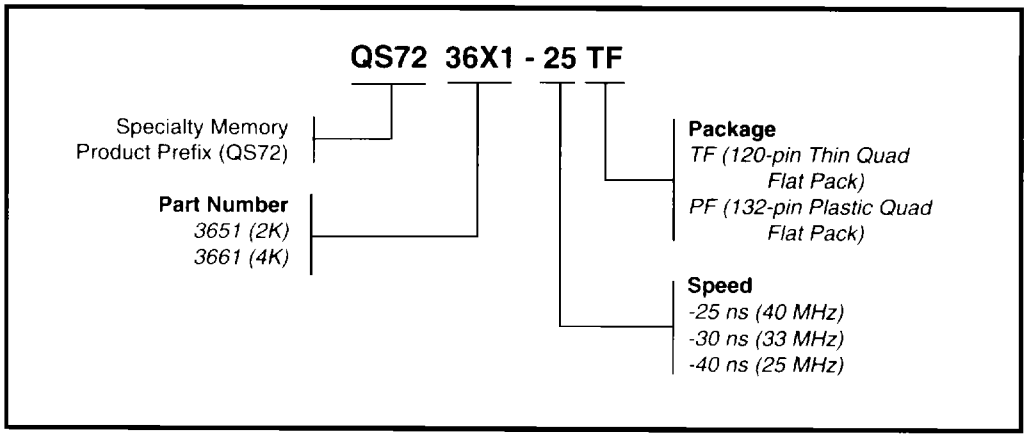
APPLICATION INFORMATION

WIDTH EXPANSION

The QS736X1 FIFO may be expanded in width by connecting the clocks, enables and reset lines of the FIFOs in parallel. Read and write operations occur synchronous to each other, so internal pointer location and flag states will be identical to each FIFO.

ORDERING INFORMATION

Example:

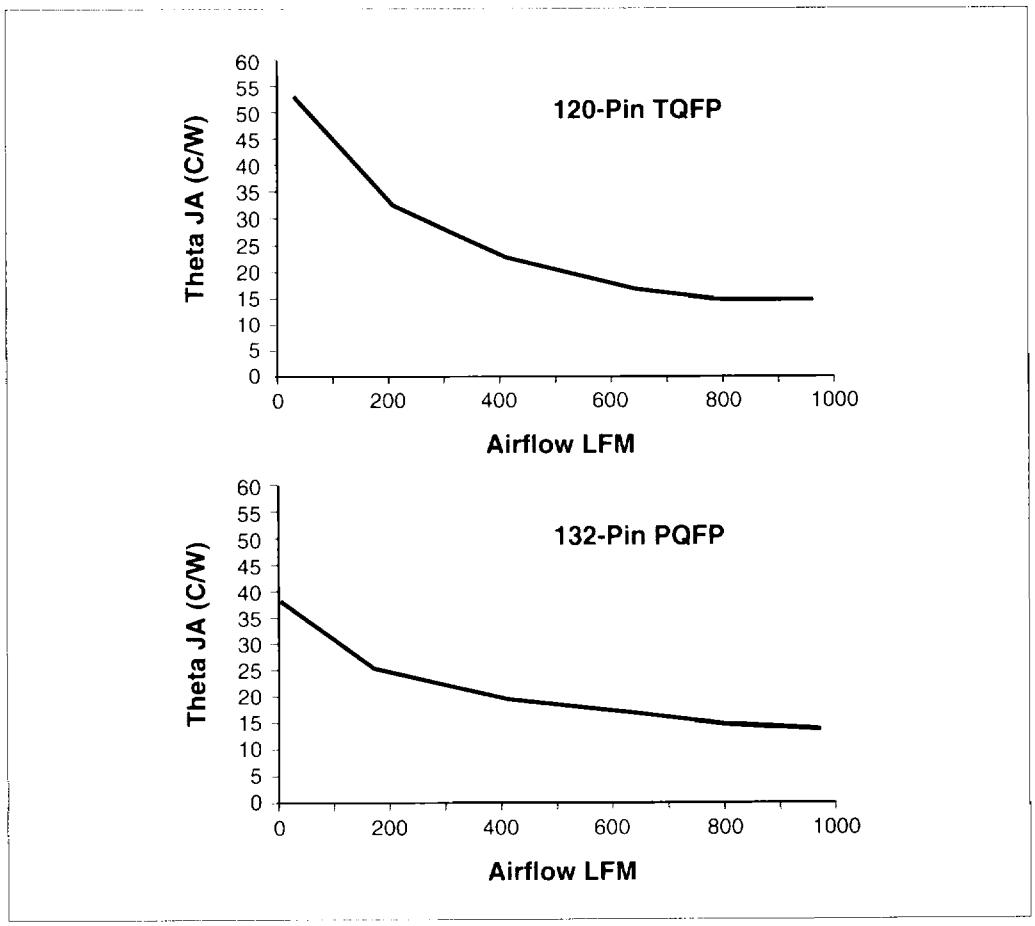


PACKAGING INFORMATION

The QS723661 family of devices is offered in a 132-pin PQFP package, as well as the JEDEC standard 120-pin TQFP (Thin QFP) plastic package. This package offers the best combination of small footprint, manufacturability and low cost. Test sockets are available from Yamaichi and may be available from ITT Pomona as of this writing. TQFP products are shipped in plastic trays. θja for the TQFP is 64°C/W.

As with all large plastic packages, care should be taken to avoid moisture related mechanical failure. This typically occurs when moisture absorbed into the porous molding compound vaporizes during reflow operations. To prevent moisture related assembly problems, it is recommended that customers perform a baking operation prior to assembly. By baking the units for 24 hours at 125°C, excess moisture is removed from the part. In a typical environment of 60% relative humidity at <30°C, parts can sit up to 48 hours before assembly. In higher humidity environments, the time between bake and solder reflow should be shorter. In dry environments (<20% RH), or when sealed in moisture barrier bags with dessicant, shelf life is indefinite.

FIGURE 20. PACKAGE THERMAL CHARACTERISTICS



5