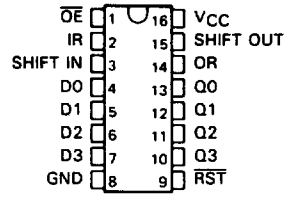
D2958, OCTOBER 1986 - REVISED APRIL 1988

- **Asynchronous Operation**
- **Organized as 64 Words of 4 Bits**
- **Data Rates from 0 to 30 MHz**
- **3-State Outputs**
- **Similar to MMI67401B with Higher Speed and 3-State Outputs**
- **Dependable Texas Instruments Quality and Reliability**

SN74ALS234 . . . N PACKAGE
(TOP VIEW)



description

The SN74ALS234 is a 256-bit memory utilizing Advanced Low-Power Schottky IMPACT™ Technology. It features high speed with fast fall-through times and is organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS234 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{RST}$ goes low.

Status of the 'ALS234 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

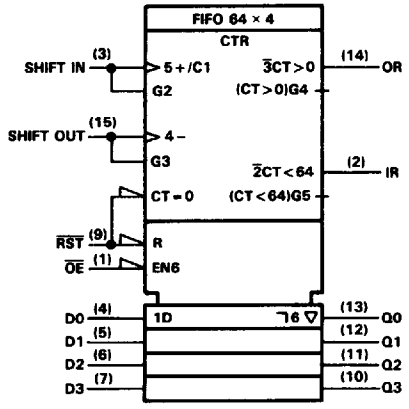
When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input ($\overline{RST}$). This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when $\overline{RST}$ goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before $\overline{RST}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable ($\overline{OE}$) is high. $\overline{OE}$ does not affect the IR and OR outputs.

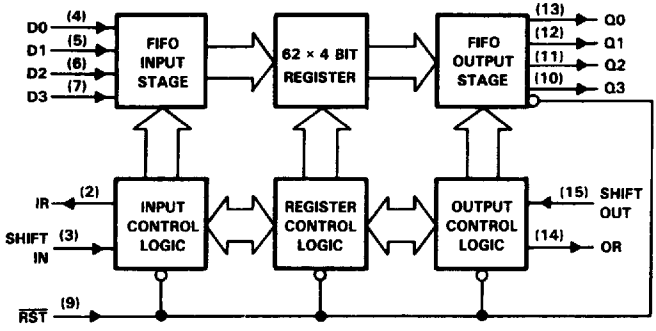
The SN74ALS234 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Pin numbers shown are for N packages.

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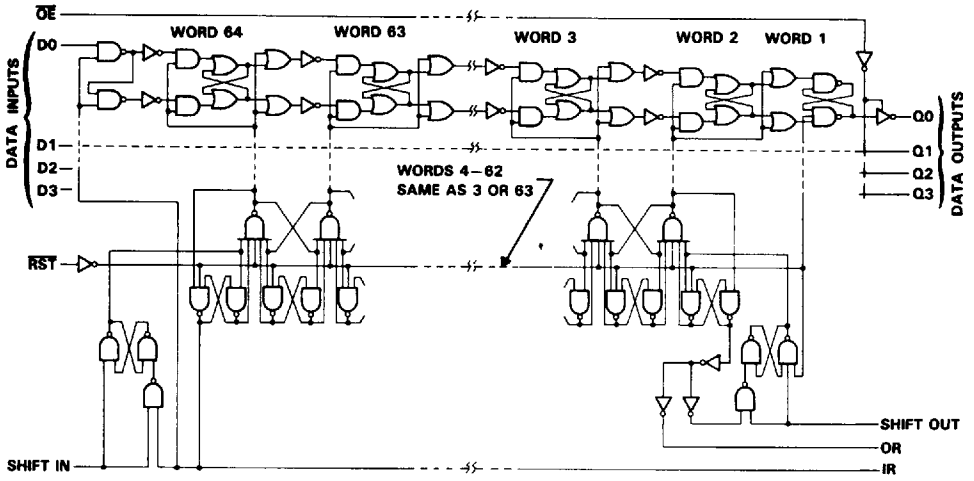
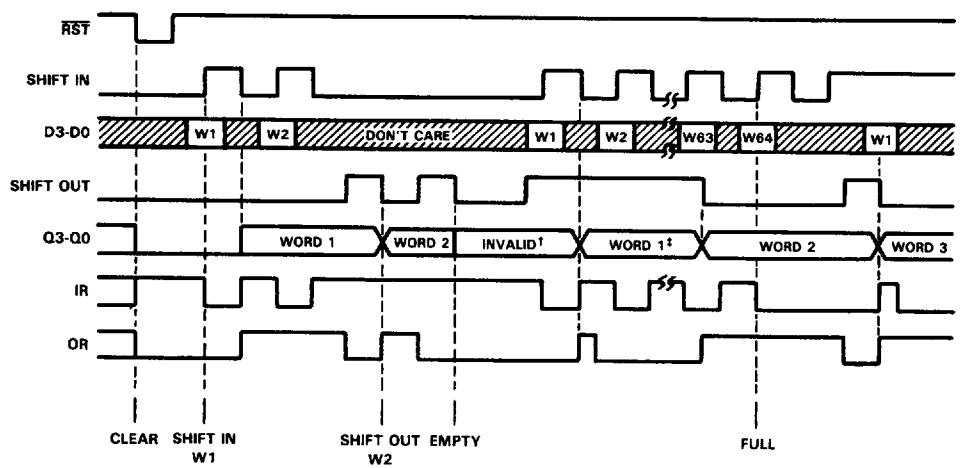
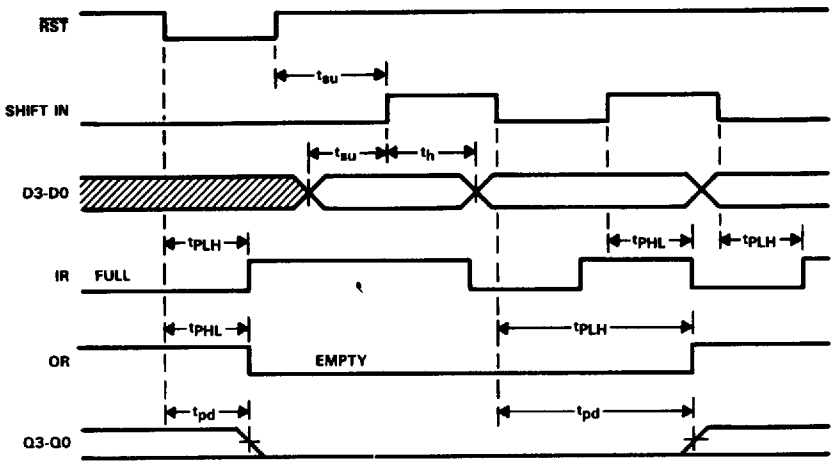
logic diagram (positive logic)



timing diagram

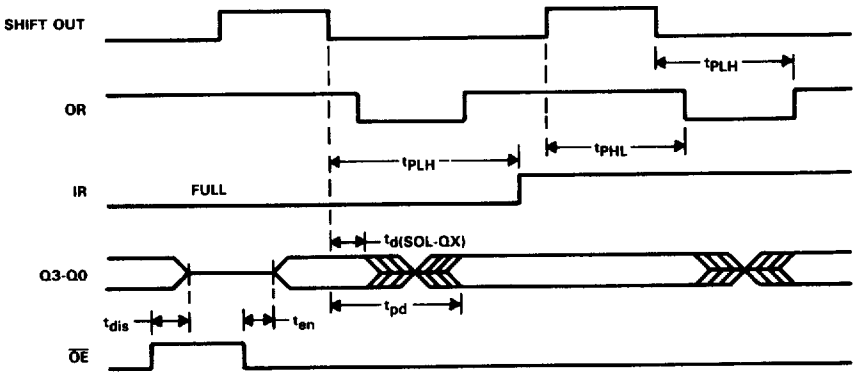


† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.
‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER RESET AND DATA IN WAVEFORMS



NOTE SHIFT IN is low

FIGURE 2. DATA OUT WAVEFORMS

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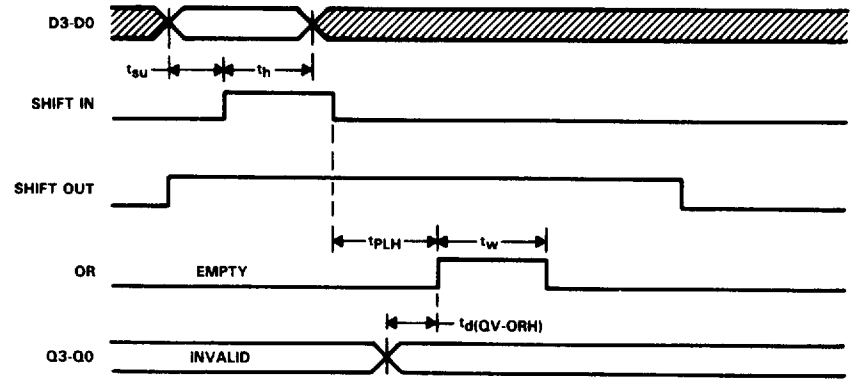

FIGURE 3. DATA FALL THROUGH WAVEFORMS

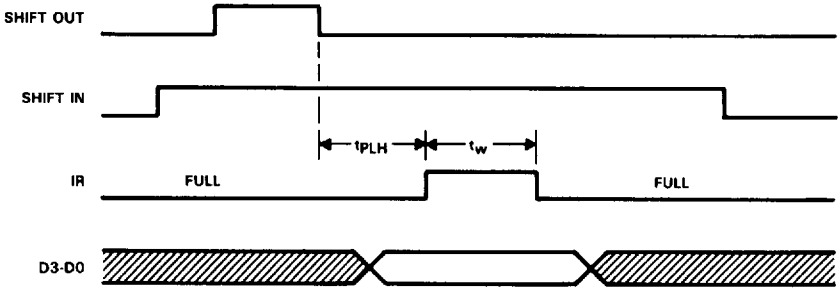

FIGURE 4. AUTOMATIC DATA IN WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN74ALS234 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN74ALS234			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		IR and OR			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		IR and OR			8	
f_{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		30	MHz
t_w	Pulse duration	SHIFT IN or SHIFT OUT high or low	15			ns
		$\overline{RST}$ low	15			
t_{su}	Setup time before SHIFT IN↑	Data	0			ns
		$\overline{RST}$ high (inactive)	15			
t_h	Hold time, data after SHIFT IN↑		17			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS234			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q	V_{CC} = 4.5 V,	I_{OH} = −1 mA				V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.7	3.4		
V_{OL}	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	I_{CCL}		100	145	mA
			I_{CCH}		97	142	
			I_{CCZ}		103	148	

† All typical values are at V_{CC} = 5 V, T_A = 25°C
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			'ALS234			SN74ALS234		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SHIFT IN			35		30		MHz
	SHIFT OUT			35		30		
t_w†	IR high			15		8		ns
t_w‡	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR ↑			6	9	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SHIFT OUT ↓			13		4		ns
t_{pd}	SHIFT IN ↓	Q		600	800	350	1000	ns
t_{PHL}	SHIFT IN ↑	IR		20	26	8	30	ns
t_{PLH}	SHIFT IN ↓	IR		16	21	6	25	ns
t_{PLH}§	SHIFT IN ↓	OR		600	800	350	1000	ns
t_{pd}	SHIFT OUT ↓	Q		13	17	4	22	ns
t_{PHL}	SHIFT OUT ↑	OR		23	27	7	33	ns
t_{PLH}	SHIFT OUT ↓	OR		20	24	6	30	ns
t_{PLH}§	SHIFT OUT ↓	IR		600	800	350	1000	ns
t_{PHL}	$\overline{RST}$ ↓	OR		22	26	10	34	ns
t_{PLH}	$\overline{RST}$ ↓	IR		17	21	6	27	ns
t_{PHL}	$\overline{RST}$ ↓	Q		14	17	5	19	ns
t_{dis}	$\overline{OE}$ ↑	Q		7	13	2	15	ns
t_{en}	$\overline{OE}$ ↓	Q		6	12	2	13	ns

† The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).
‡ The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3)
§ Data throughput or "fall through" times
NOTE 1 Load circuit and voltage waveforms are shown in Section 1

TYPICAL APPLICATION INFORMATION

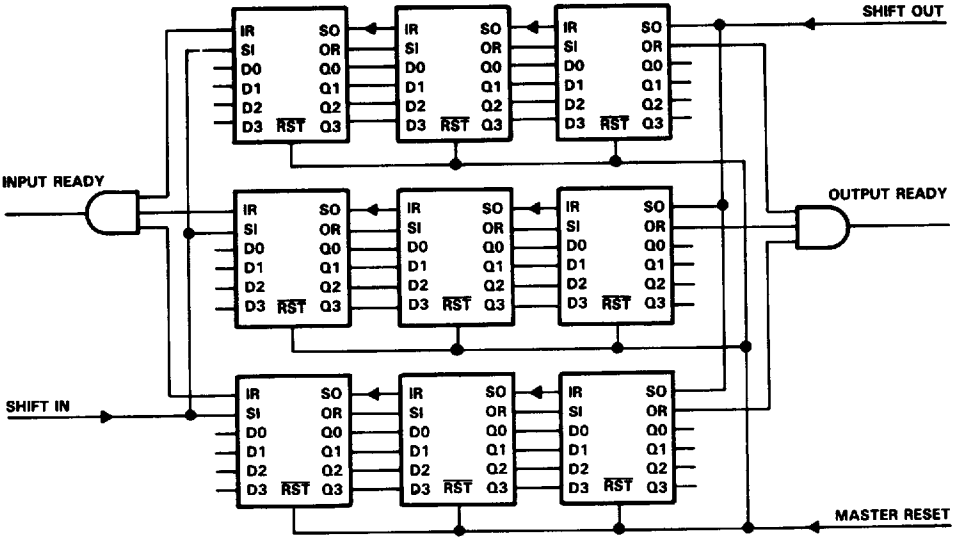

FIGURE 5. 192-WORD BY 12-BIT EXPANSION

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