HFBR-59L1AL

1.25 GBd Ethernet and 1.0625 GBd Fibre Channel 850 nm SFF Low Voltage (3.3 V) Optical Transceiver

Data Sheet



Description

The HFBR-59L1AL from Avago Technologies is a high performance, cost-effective optical transceiver for serial optical data communications applications operating at 1.25 Gb/s and 1.0625 Gb/s. This module is designed for multimode fiber and operates at a nominal wavelength of 850 nm.

The transceiver incorporates 3.3 V DC compatible technology including an 850 nm VCSEL transmitter. The HFBR-59L1AL offers maximum flexibility to Fibre Channel and Ethernet designers, manufacturers, and system integrators. It is designed for use in short reach multimode fiber optic 1000BASE-SX and Fiber Channel (100-M5-SN-1) links.

This device is also designed for a wide voltage and temperature range of operation. This transceiver is compliant with the Small Form Factor Multi-Source Agreement and is fully compliant with all equipment meeting the Gigabit Ethernet (1000 Base-SX) and Fibre Channel (FC-PI 100-M5-SN-I, FC-PI 100-M6-SN-I, FC-PH2 100-M5-SN and FC-PH2 100-M6-SN-I 1.0625 GBd) specifications.

Related Products

- HFCT-59L1ATL: 1300 nm Small Form Factor optical transceiver for 10 km Gigabit Ethernet links
- HFBR-5911L/AL: 850 nm Small Form Factor optical transceiver for short reach Gigabit Ethernet (1000BASE-SX) links
- HFBR-5701L/LP: 850 nm Small Form Factor Pluggable optical transceiver for short reach Gigabit Ethernet (1000BASE-SX) and 1.0625 Gbd Fibre Channel links
- HDMP-2634: Single SerDes IC 2.5/1.25 Gigabit
- HDMP-1687: Quad SerDes IC for Gigabit Ethernet with 10 bit parallel interface and TTL clock input
- HDMP-1685A: Quad SerDes IC for Gigabit Ethernet with 5 bit parallel interface and DDR TTL clock input
- HDMP-1636A/46A: Single SerDes IC for Gigabit Ethernet and Fiber Channel
- HDMP-1637A: Single SerDes IC with PECL RefClk
- HDMP-1638: Single SerDes IC with PECL RefClk and Dual Serial I/O

Features

- Data rate specification: 1.25 GBd operation for IEEE 802.3 Gigabit Ethernet 1000BASE-SX 1.0625 GBd operation for FC-PI 100-M5-SN-I and FC-PI 100-M6-SN-I
- Wide temperature and supply voltage operation
- Industry standard 2 x 5 SFF package
- LC-duplex connector optical interface
- Link lengths at 1.25 GBd:
  0.5 to 500 m – 50/125 mm MMF
  0.5 to 275 m – 62.5/125 mm MMF
- Link lengths at 1.0625 GBd:
  0.5 to 500 m – 50/125 mm MMF
  0.5 to 300 m – 62.5/125 mm MMF
- Reliable 850 nm Vertical Cavity Surface Emitting Laser (VCSEL) source technology
- Laser AEL Class I (eye safe) per:
  US 21 CFR (J)
  EN 60825-1 (+All)
- Single +3.3 V power supply operation
- Wave solder and aqueous wash process compatible

Applications

- Short reach Gigabit Ethernet links
- High speed backplane interconnects
- Switched backbones
- iSCSI applications
- Mass storage system I/O
- Computer system I/O
- High speed peripheral interface
- High speed switching systems
- Host adaptor I/O

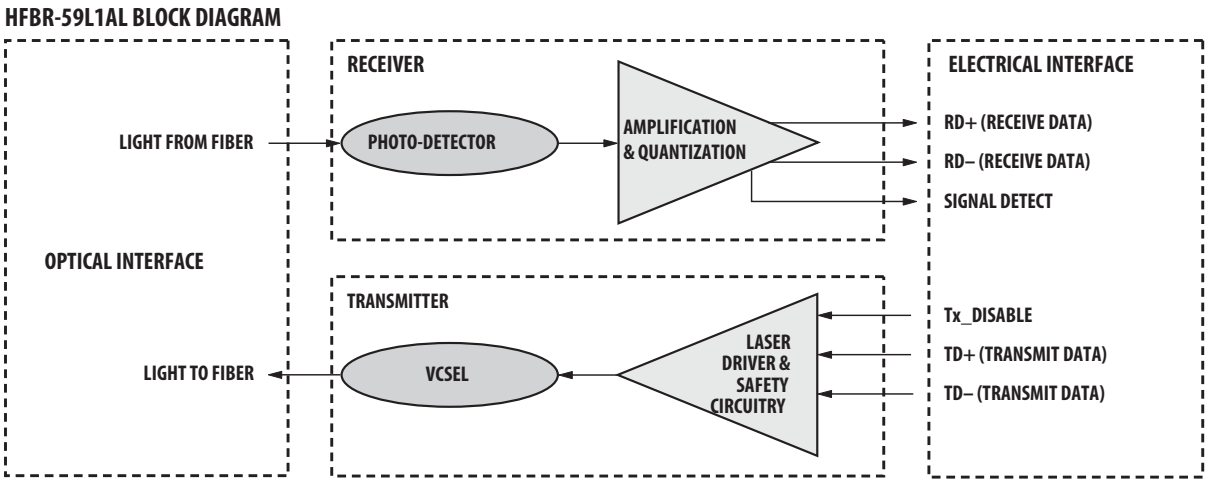


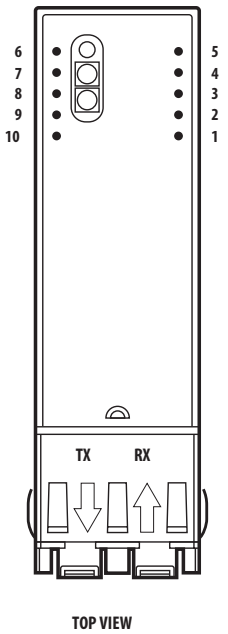
Figure 1. Transceiver functional diagram. (See Process Compatibility Specifications)

Module Package

Avago offers the Pin Through Hole package utilizing an integral LC Duplex optical interface connector. The transceiver uses a reliable 850 nm VCSEL source and requires a 3.3 V dc power supply for optimal system design.

Module Diagrams

Figure 1 illustrates the major functional components of the HFBR-59L1AL. The connection diagram for both modules are shown in Figure 2. Figures 6a and 6b depict the external configuration and dimensions of the module.



Pin Description

Pin	Name	Type
1	RX Ground	Ground
2	RX Power	Power
3	RX SD	Status Out
4	RX Data Bar	Signal Out
5	RX Data	Signal Out
6	TX Power	Power
7	TX Ground	Ground
8	TX Disable	Control In
9	TX Data	Signal In
10	TX Data Bar	Signal In

Figure 2. Module pin assignments and pin configuration

Installation

The HFBR-59L1AL can be installed in any MSA compliant Pin Through Hole port. The module Pin Description is shown in Figure 2.

Solder and Wash Process Capability

These transceivers are delivered with protective process plugs inserted into the LC connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping. These transceivers are compatible with industry standard wave or hand solder processes.

Recommended Solder Fluxes

Solder fluxes used with the HFBR-59L1AL should be watersoluble, organic fluxes. Recommended solder fluxes include Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-Metals of Jersey City, NJ.

Recommended Cleaning/Degreasing Chemicals

Alcohols: methyl, isopropyl, isobutyl.

Aliphatics: hexane, heptane.

Other: naphtha. Do not use partially halogenated hydrocarbons such as 1,1.1 trichoroethane or ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone.

Also, Avago does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

Transmitter Section

The transmitter section includes an 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) light source and a transmitter driver circuit. The driver circuit maintains a constant optical power level provided that the data pattern is valid 8B/10B code. Connection to the transmitter is provided via an LC optical connector.

TX Disable

The HFBR-59L1AL accepts a LVTTL transmit disable control signal input which shuts down the transmitter. A high signal implements this function while a low signal allows normal laser operation. In the event of a fault (e.g., eye safety circuit activated), cycling this control signal resets the module. The TX Disable control should be actuated upon initialization of the module. See Figure 5 for product timing diagrams.

Eye Safety Circuit

For an optical transmitter device to be eye-safe in the event of a single fault failure, the transmitter will either maintain normal, eye-safe operation or be disabled. In the event of an eye safety fault, the VCSEL will be disabled.

Receiver Section

Connection to the receiver is provided via an LC optical connector. The receiver circuit also includes a Signal Detect (SD) circuit which provides an open collector logic low output in the absence of a usable input optical signal level.

Signal Detect

The Signal Detect (SD) output indicates if the optical input signal to the receiver does not meet the minimum detectable level for Fibre Channel compliant signals. When SD is low it indicates loss of signal. When SD is high it indicates normal operation. The Signal Detect thresholds are set to indicate a definite optical fault has occurred (e.g., disconnected or broken fiber connection to receiver, failed transmitter).

Functional Data I/O

Avago's HFBR-59L1AL fiberoptic transceiver is designed to accept industry standard differential signals. In order to reduce the number of passive components required on the customer's board, Avago has included the functionality of the transmitter bias resistors and coupling capacitors within the fiber optic module. The transceiver is compatible with an "ac-coupled" configuration and is internally terminated. Figure 1 depicts the functional diagram of the HFBR-59L1AL. Caution should be taken to account for the proper interconnection between the supporting Physical Layer integrated circuits and the HFBR-59L1AL. Figure 3 illustrates the recommended interface circuit.

Reference Designs

Figure 3 depicts a typical application configuration, while Figure 4 depicts the multisourced power supply filter circuit design. Regulatory Compliance See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions in which immunity to ESD damage is important. Table 1 documents our immunity to both of these conditions. The first condition is during handling of the transceiver prior to attachment to the PCB. To protect the transceiver, it is important to use normal ESD handling precautions. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The ESD sensitivity of the HFBR-59L1AL is compatible with typical industry production environments. The second condition is static discharges to the exterior of the host equipment chassis after installation. To the extent that the duplex LC optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements. The ESD performance of the HFBR- 59L1AL exceeds typical industry standards.

Immunity

Equipment hosting the HFBR- 59L1AL modules will be subjected to radio-frequency electromagnetic fields in some environments. The transceivers have good immunity to such fields due to their shielded design.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The metal housing and shielded design of the HFBR-59L1AL minimize the EMI challenge facing the host equipment designer.

These transceivers provide superior EMI performance. This greatly assists the designer in the management of the overall system EMI performance.

Eye Safety

These 850 nm VCSEL-based transceivers provide Class 1 eye safety by design. Avago has tested the transceiver design for compliance with the requirements listed in Table 1: Regulatory Compliance, under normal operating conditions and under a single fault condition.

Flammability

The HFBR-59L1AL VCSEL transceiver housing is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Caution

There are no user serviceable parts nor is any maintenance required for the HFBR-59L1AL. All adjustments are made at the factory before shipment to our customers.

Tampering with or modifying the performance of the HFBR- 59L1AL will result in voided product warranty. It may also result in improper operation of the HFBR-59L1AL circuitry, and possible overstress of the laser source. Device degradation or product failure may result. Connection of the HFBR-59L1AL to a non-approved optical source, operating above the recommended absolute maximum conditions or operating the HFBR-59L1AL in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product.

The person(s) performing such an act is required by law to recertify and reidentify the laser product under the provisions of U.S. 21 CFR (Subchapter J) and the TUV.

Ordering Information

Please contact your local field sales engineer or one of Avago Technologies franchised distributors for ordering information. For technical information regarding this product, including the MSA, please visit Avago Technologies Semiconductors Products Website at www.Avago.com/ view/fiber. Use the quick search feature to search for this part number. You may also contact Avago Technologies Semiconductor Products Customer Response Center at 1-800-235-0312.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 2 (>2000 V)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the duplex LC connector receptacle is contaced by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 1000 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	US FDA CDRH AEL Class 1 EN (IEC)60825-1, 2 EN60950 Class 1	CDRH file # 9720151 TUV file # R2079009
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment.	UL file # E173874

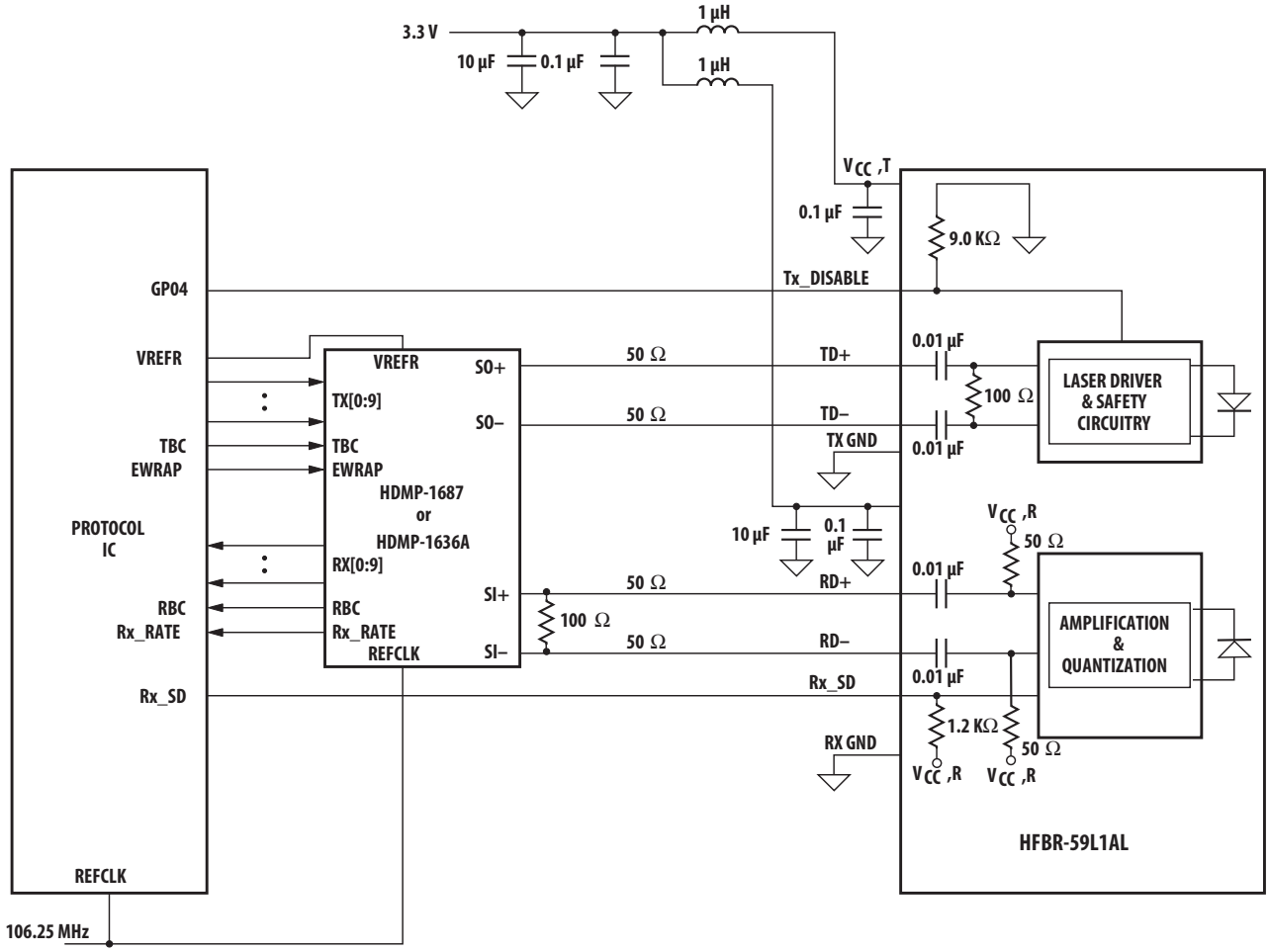
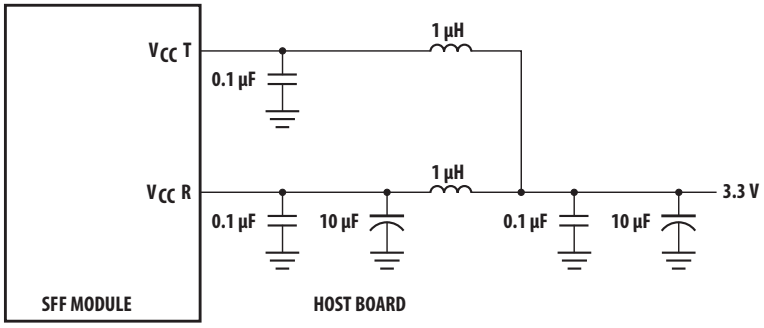


Figure 3. Typical application configuration



NOTE: INDUCTORS MUST HAVE LESS THAN 1 Ω SERIES RESISTANCE PER MSA.

Figure 4. MSA recommended power supply filter

Table 2. Pin Description

Pin	Name	Function/Description	MSA Notes
1	$V_{EE}R$	Receiver Ground	1
2	$V_{CC}R$	Receiver Power: 3.3 V ±10%	5
3	SD	Signal Detect: Low indicates Loss of Signal	3
4	RD-	Inverse Received Data Out	4
5	RD+	Received Data Out	4
6	$V_{CC}T$	Transmitter Power: 3.3V ±10%	5
7	$V_{EE}T$	Transmitter Ground	1
8	TX Disable	Transmitter Disable: Module disables on High	2
9	TD+	Transmitter Data In	
10	TD-	Inverse Transmitter Data In	

Notes:

1. Transmitter and Receiver Ground are common in the internal module PCB. They are electrically connected to signal ground within the module, and to the housing shield (see Note 5 in Figure 7c). This housing shield is electrically isolated from the nose shield which is connected to chassis ground (see Note 4 in Figure 7c).
2. TX disable input is used to shut down the laser output per the state table below. It is pulled down internally within the module with a 9.0 KΩ resistor.
   Low (0 – 0.8 V): Transmitter on
   Between (0.8 V and 2.0 V): Undefined
   High (2.0 – 3.465 V): Transmitter Disabled
   Open: Transmitter Enabled
3. SD (Signal Detect) is a normally high LVTTL output. When high it indicates that the received optical power is adequate for normal operation. When Low, it indicates that the received optical power is below the worst case receiver sensitivity, a fault has occurred, and the link is no longer valid.
4. RD-/+: These are the differential receiver outputs. They are ac coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the user SerDes. The ac coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 2000 mV differential (200 – 1000 mV single ended) when properly terminated. These levels are compatible with CML and LVPECL voltage swings.
5. $V_{CC}R$ and $V_{CC}T$ are the receiver and transmitter power supplies. They are defined as 2.97 – 3.63 V at the PTH connector pin. The maximum supply current is 200 mA.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Storage Temperature	T_S	-40		+100	°C	1
Case Temperature	T_C	-10		+85	°C	1, 2
Relative Humidity	RH	5		95	%	1
Supply Voltage	V_{CC}T, R	-0.5		4	V	1, 2
Data/Control Input Voltage	V_I	-0.5		V_{CC} + 0.3	V	1
Sense Output CurrentSignal Detect [SD]	I_D			5.0	mA	1

Notes:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time. See Reliability Data Sheets for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions, functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature	T_C	-10	+25	+85	°C	1
Module Supply Voltage	V_{CC}T, R	2.97	3.3	3.63	V	1
Data Rate:						
Fibre Channel			1.0625		Gb/s	1
Ethernet			1.25		Gb/s	1

Notes:
1. Recommended operating conditions are those values outside of which functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time. See Reliability Data Sheet for specific reliability performance.

Table 5. Process Compatibility

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Hand Lead Solder:						
Temperature	T_{solder}			+260	°C	
Time	t_{time}			10	sec	
Wave Solder and Aqueous Wash:						
Temperature	T_{solder}			+260	°C	1
Time	t_{time}			10	sec	

Notes:
1. Aqueous wash pressure < 110 psi.

Table 6. Transceiver Electrical Characteristics

(T_C = -10°C to +85°C, $V_{CC}T$, R = 3.3 V ±10%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
AC Electrical Characteristics						
Power Supply Noise Rejection (Peak-to-Peak)	PSNR		100		mV	1
DC Electrical Characteristics						
Module Supply Current	I_{CC}			200	mA	
Power Dissipation	P_{DISS}			726	mW	
Sense Outputs:						
Signal Detect [SD]	V_{OH}	2.4		$V_{CC}R$ + 0.3	V	2
	V_{OL}			0.4	V	
Control Inputs:						
Transmitter Disable	V_{IH}	2.4		V_{CC} + 0.3	V	3
[TX_DISABLE]	V_{IL}	0.0		0.4	V	

Notes:
1. MSA filter is required on host board 10 Hz to 2 MHz.
2. LVTTL, 1.2 kΩ internal pull-up resistor to $V_{CC}R$.
3. 9.0 KΩ internal pull-down resistor to V_{EE}.
4. Please refer to the HFBR-59L1AL characterization report for typical values.

Table 7. Transmitter and Receiver Electrical Characteristics

(T_C = -10°C to +85°C, $V_{CC}T$, R = 3.3 V ±10%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Data Input: Transmitter Differential Input Voltage (TD +/-)	VI	400		2400	mV	1
Data Output: Receiver Differential Output Voltage (RD +/-)	V_O	400	625	2000	mV	2
Receive Data Rise and Fall Times (Receiver)	$T_{rise/fall}$			200	ps	3
Contributed Deterministic Jitter (Receiver) 1.25 Gb/s	DJ			0.212	UI	4, 6
				170	ps	
Contributed Deterministic Jitter (Receiver) 1.0625 Gb/s	DJ			0.12	UI	
	DJ			113	ps	
Contributed Random Jitter (Receiver) 1.25 Gb/s	RJ			0.120	UI	5, 6
	RJ			96	ps	
Contributed Random Jitter (Receiver) 1.0625 Gb/s	RJ			0.098	UI	
	RJ			92	ps	

Notes:
1. Internally ac coupled and terminated (100 Ohm differential). These levels are compatible with CML and LVPECL voltage swings.
2. Internally ac coupled with internal 50 Ohm pullups to V_{CC} (single-ended) and a required external 100 Ohm differential load termination.
3. 20% - 80% rise and fall times measured with a 500 MHz signal utilizing a 1010 data pattern.
4. Contributed DJ is measured on an oscilloscope in average mode with 50% threshold and K28.5 pattern.
5. Contributed RJ is calculated for 1E-12 BER by multiplying the RMS jitter (measured on a single rise or fall edge) from the oscilloscope by 14. Per the FC-PI standard (Table 13 - MM jitter output, note 1), the actual contributed RJ is allowed to increase above its limit if the actual contributed DJ decreases below its limits, as long as the component output DJ and TJ remain within their specified FC-PI maximum limits with the worst case specified component jitter input.
6. In a network link, each component's output jitter equals each component's input jitter combined with each component's contributed jitter. Contributed DJ adds in a linear fashion and contributed RJ adds in a RMS fashion. In the Fibre Channel specification, there is a table specifying the input and output DJ and TJ for the receiver at each data rate. In that table, RJ is found from TJ –DJ, where the RX input jitter is noted as Gamma R, and the Rx output jitter is noted as Delta R. The HFBR-59L1AL contributed jitter is such that, if the maximum specified input jitter is present, and is combined with our maximum contributed jitter, then we meet the specified maximum output jitter limits listed in the FC-PI MM jitter specification table.
7. Please refer to the HFBR-59L1AL characterization report for typical values.

Table 8. Transmitter Optical Characteristics

(T_C = -10°C to +85°C, $V_{CC}T$, R = 3.3 V ±10%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Optical Power (Average)	POUT	-9.5		0	dBm	50/125 μm NA = 0.2 Note 1
	POUT	-9.5		0	dBm	62.5/125 μm NA = 0.275 Note 1
Optical Extinction Ratio	ER	9			dB	
Optical Modulation Amplitude (Peak-to-Peak) 1.0625 Gb/s	OMA	156			μW	FC-PI Std Note 3
Center Wavelength	λ_C	830		860	nm	FC-PI Std
Spectral Width - rms	σ			0.85	nm	FC-PI Std
Optical Rise/Fall Time	$T_{rise/fall}$			150	ps	20%-80%, FC-PI Std
RIN_{12} (OMA), maximum	RIN			-117	dB/Hz	FC-PI Std
Contributed Deterministic Jitter (Transmitter) 1.25 Gb/s	DJ			0.1	UI	Notes 3, 4
	DJ			80	ps	
Contributed Deterministic Jitter (Transmitter) 1.0625 Gb/s	DJ			.09	UI	Notes 3, 4
	DJ			85	ps	
Contributed Random Jitter (Transmitter) 1.25 Gb/s	RJ			.184	UI	Notes 4, 5
	RJ			147	ps	
Contributed Random Jitter (Transmitter) 1.0625 Gb/s	RJ			.177	UI	Notes 4, 5
	RJ			167	ps	
POUT TX_DISABLE Asserted	P_{OFF}			-35	dBm	

Notes:

1. Max Pout is the lesser of 0 dBm or Maximum allowable per Eye Safety Standard.
2. An OMA of 156 is approximately equal to an average power of –10 dBm assuming an Extinction Ratio of 9 dB.
3. Contributed DJ is measured on an oscilloscope in average mode with 50% threshold and K28.5 pattern.
4. Contributed RJ is calculated for 1E-12 BER by multiplying the RMS jitter (measured on a single rise or fall edge) from the oscilloscope by 14. Per the FC-PI standard (Table 13 - MM jitter output, note 1), the actual contributed RJ is allowed to increase above its limit if the actual contributed DJ decreases below its limits, as long as the component output DJ and TJ remain within their specified FC-PI maximum limits with the worst case specified component jitter input.
5. In a network link, each component's output jitter equals each component's input jitter combined with each component's contributed jitter. Contributed DJ adds in a linear fashion and contributed RJ adds in a RMS fashion. In the Fibre Channel specification, there is a table specifying the input and output DJ and TJ for the transmitter at each data rate. In that table, RJ is found from TJ – DJ, where the TX input jitter is noted as Delta T, and the TX output jitter is noted as Gamma T. The HFBR-59L1AL contributed jitter is such that, if the maximum specified input jitter is present, and is combined with our maximum contributed jitter, then we meet the specified maximum output jitter limits listed in the FC-PI MM jitter specification table.
6. Please refer to the HFBR-59L1AL characterization report for typical values.

Table 9. Receiver Optical Characteristics

(T_C = -10°C to +85°C, $V_{CC}T$, R = 3.3 V ±10%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Optical Power	PIN			0	dBm	FC-PI Std
Receiver Sensitivity (Optical Input Power) 1.25 Gb/s	PRMIN			-17	dBm	Note 1
Min Optical Modulation Amplitude (Peak-to-Peak)1.0625 Gb/s	OMA	31			µW	FC-PI Std Note 2
Stressed Receiver Sensitivity						Note 3
62.5 µm fiber 1.25 Gb/s	PRMIN				dBm	Note 4
62.5 µm fiber 1.0625 Gb/s	OMA	67		-12.5	µW	
50 µm fiber 1.25 Gb/s	PRMIN				dBm	
50 µm fiber 1.0625 Gb/s	OMA	55		-13.5	µW	
Return Loss		12			dB	FC-PI Std
Signal Detect - De-Assert	P_D	-31		-17.5	dBm	Note 5
Signal Detect - Assert	P_A			-17.0	dBm	Note 5
Signal Detect - Hysteresis	$P_A - P_D$	0.5	2.1	5	dB	

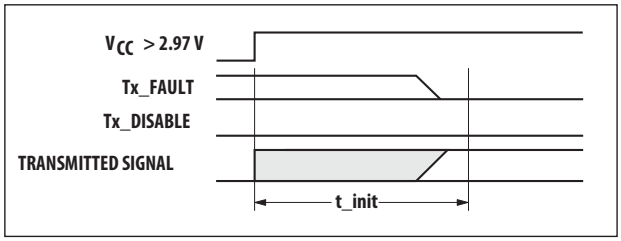
Notes:
1. Sensitivity measurements are made at eye center with BER = $1E^{-12}$.
2. An OMA of 31 is approximately equal to an average power of –17 dBm assuming an Extinction Ratio of 9 dB.
3. 1.25 Gb/s Stressed receiver vertical eye closure penalty (ISI) min is 2.2 dB for 50 µm fiber and 2.6 dB for 62.5 µm fiber. Stressed receiver DCD component min (at TX) is 65 ps.
4. 1.0625 Gb/s Stressed receiver vertical eye closure penalty (ISI) min is 0.96 dB for 50 µm fiber and 2.18 dB for 62.5 µm fiber. Stressed receiver DCD component min (at TX) is 80 ps.
5. These average power values are specified with an Extinction Ratio of 9 dB. The Signal Detect circuitry responds to OMA (peak-to-peak) power, not to average power.
6. Please refer to the HFBR-59L1AL characterization report for typical values.

Table 10. Transmitter Timing Characteristics

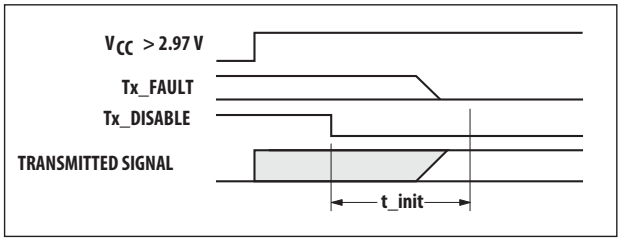
(T_C = -10°C to +85°C, $V_{CC}T$, R = 3.3 V ±10%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
TX Disable Assert Time	t_off			10	µs	1
TX Disable Negate Time	t_on			1	ms	2
Time to Initialize	t_init			300	ms	3
TX Disable to Reset	t_reset	10			µs	4
SD Assert Time	t_loss_on			100	µs	5
SD De-assert Time	t_loss_off			100	µs	6

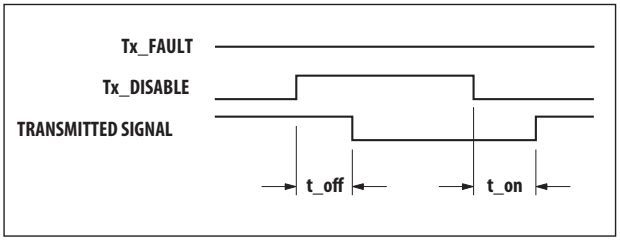
Notes:
1. Time from rising edge of TX Disable to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX Disable to when the modulated optical output rises above 90% of nominal.
3. From power on or negation of TX Fault using TX Disable.
4. Time TX Disable must be held high to reset TX Fault.
5. Time from optical signal loss to SD assert. See transceiver timing diagrams.
6. Time from optical signal recovery to SD deassert. See transceiver timing diagrams.



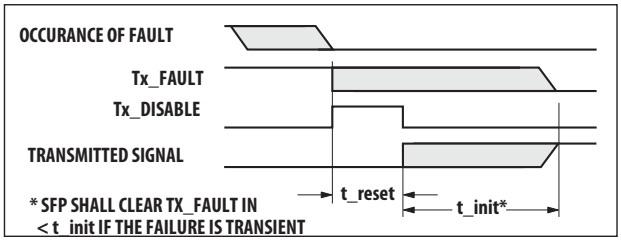
t-init: TX DISABLE DE-ASSERTED



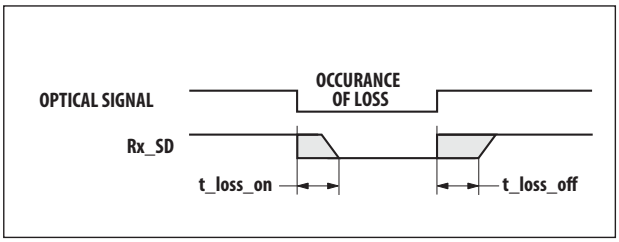
t-init: TX DISABLE ASSERTED



t-off & t-on: TX DISABLE ASSERTED THEN NEGATED

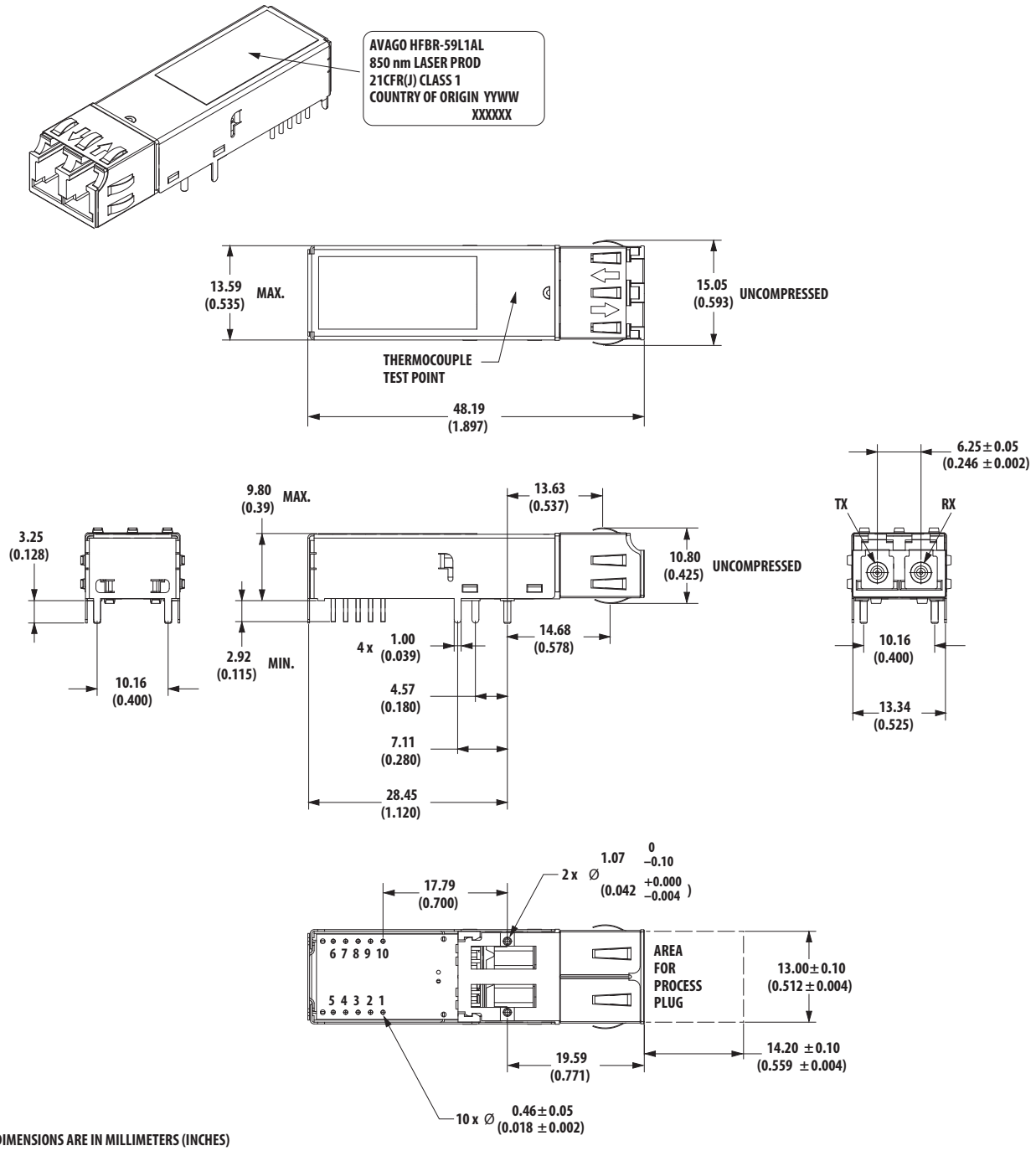


t-reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



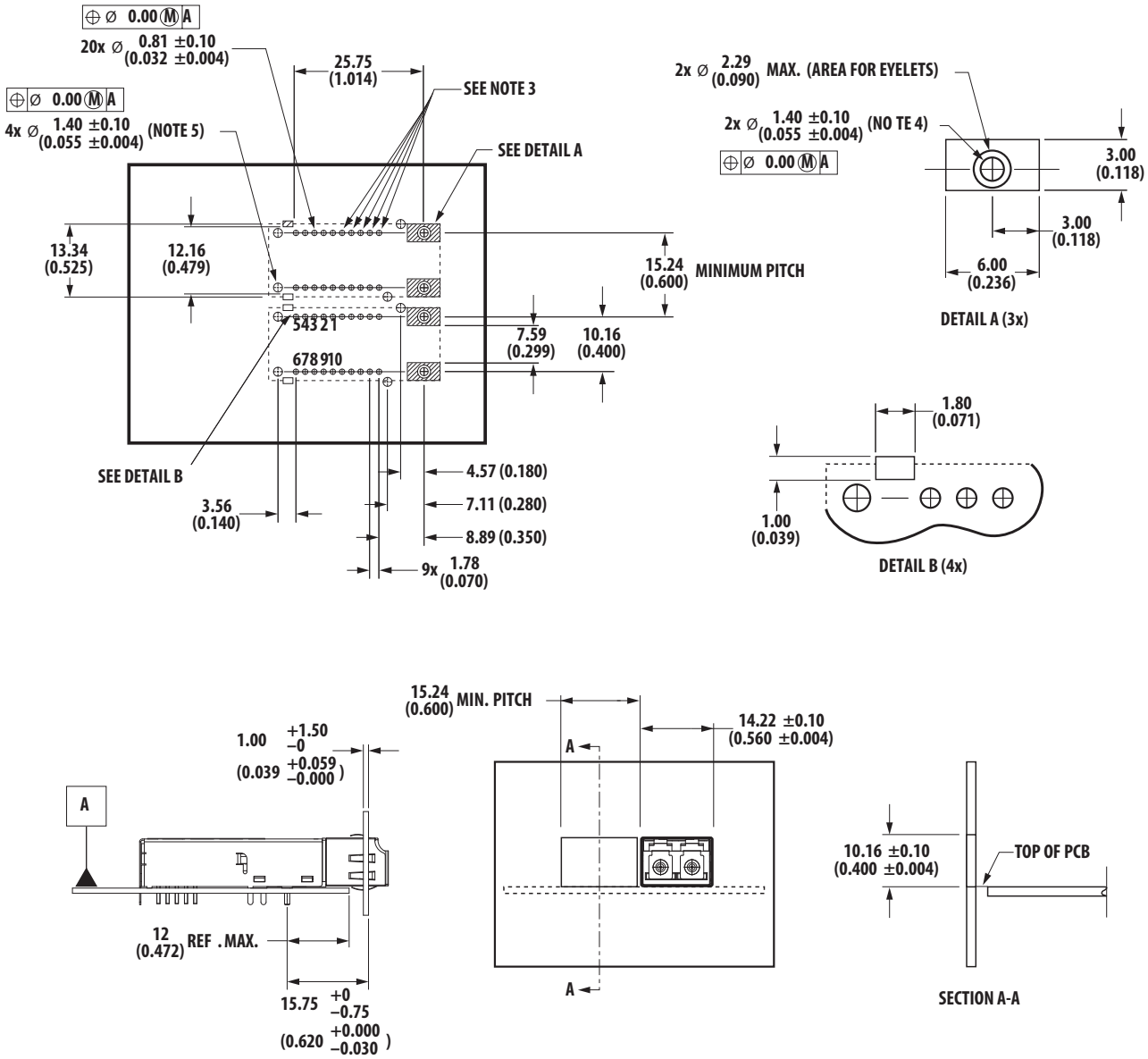
t-loss-on & t-loss-off

Figure 5. Transceiver timing diagrams



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Figure 6a. Module drawing



Notes:

1. This page describes the recommended circuit board layout and front panel openings for SFF transceivers.
2. The hatched areas are keep-out areas reserved for housing standoffs. No metal traces allowed in keep-out areas..
3. The drawing shows extra pin holes for 2x10 pin transceivers. These extra holes are not required for HFBR-59L1AL.
4. Holes for mounting studs must be tied to chassis ground.
5. Holes for housing leads mst be tied to signal ground.
6. Dimensions are in millimeters (inches).

Figure 6b. Recommended SFF host board and front panel layout

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