HFBR-5764AP

Multimode Small Form Factor Pluggable Transceivers for 200 MBd SBCON

AVAGO TECHNOLOGIES

Data Sheet

Description

The HFBR-5764AP transceiver from Avago Technologies is compatible with the SBCON specification and the IBM ESCON architecture. This transceiver conforms to the industry standard Small Form Pluggable (SFP) form factor.

This transceiver operates at a nominal wavelength of 1300 nm with an LC fiber connector interface with an external connector shield.

Transmitter Section

The transmitter section utilizes a 1300 nm InGaAsP LED. This LED is packaged in the optical subassembly portion of the transmitter section. It is driven by a custom silicon IC which converts differential PECL logic signals, ECL referenced (shifted) to a +3.3 V supply, into an analog LED drive current.

Receiver Section

The receiver section utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. It is packaged in the optical subassembly portion of the receiver.

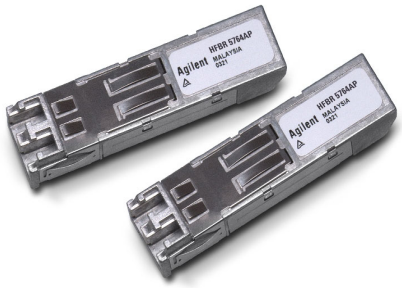
This PIN/preamplifier combination is coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Loss of Signal (LOS) function. The data output is differential. The data output is PECL compatible, ECL referenced (shifted) to a +3.3 V power supply. This circuit also includes a loss of signal (LOS) detection circuit which provides an open collector logic high output in the absence of a usable input .optical signal. The LOS output is +3.3 V TTL.

Features

- SBCON 200 MBd specification
- Industry standard Small Form Pluggable (SFP) package
- LC duplex connector optical interface
- Single +3.3 V power supply
- +3.3 V TTL LOS output
- Manufactured in an ISO 9001 certified facility
- Temperature range:
  -20 °C to +85 °C HFBR-5764AP
- Bail de-latch option

Applications

- Interconnection with IBM ® compatible processors, directors and channel attachment units
  – Disk and tape drives
  – Communication controllers
- Data communication equipment
  – Local area networks
  – Point-to-point communication



Transmitter Disable

The HFBR-5764AP accepts a transmit disable control signal input which shuts down the transmitter. A high signal implements this function while a low signal allows normal LED operation.

Loss of Signal

The Loss of Signal (LOS) output indicates that the optical input signal to the receiver does not meet the minimum detectable level for SBCON compliant signals. When LOS is high it indicates loss of signal. When LOS is low it indicates normal operation. The LOS thresholds are set to indicate a definite optical fault has occurred (e.g., disconnected or broken fiber connection to receiver, failed transmitter).

Module Package

The transceiver meets the Small Form Pluggable (SFP) industry standard package utilizing an integral LC duplex optical interface connector. The hot-pluggable capability of the SFP package allows the module to be installed at any time – even with the host system operating and on-line. This allows for system configuration changes or maintenance without system down time. The HFBR-5764AP uses a reliable 1300 nm LED source and requires a 3.3 V dc power supply for optimal design.

Module Diagrams

Figure 1 illustrates the major functional components of the HFBR-5764AP. The connection diagram of the module is shown in Figure 2. Figures 5 and 7 depict the external configuration and dimensions of the module.

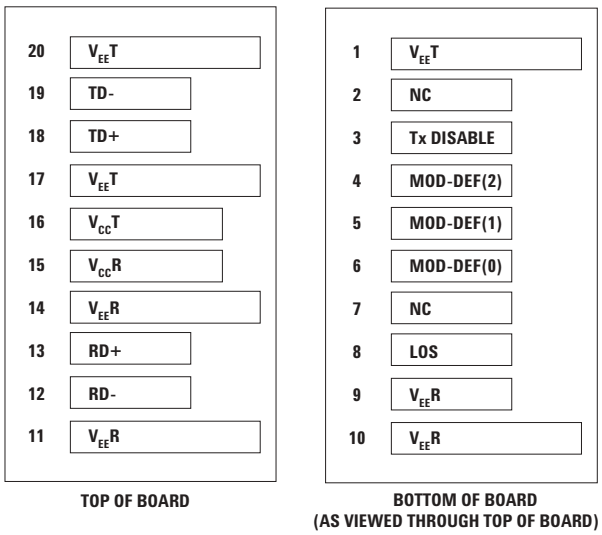


Figure 2. Connection diagram of module printed circuit board.

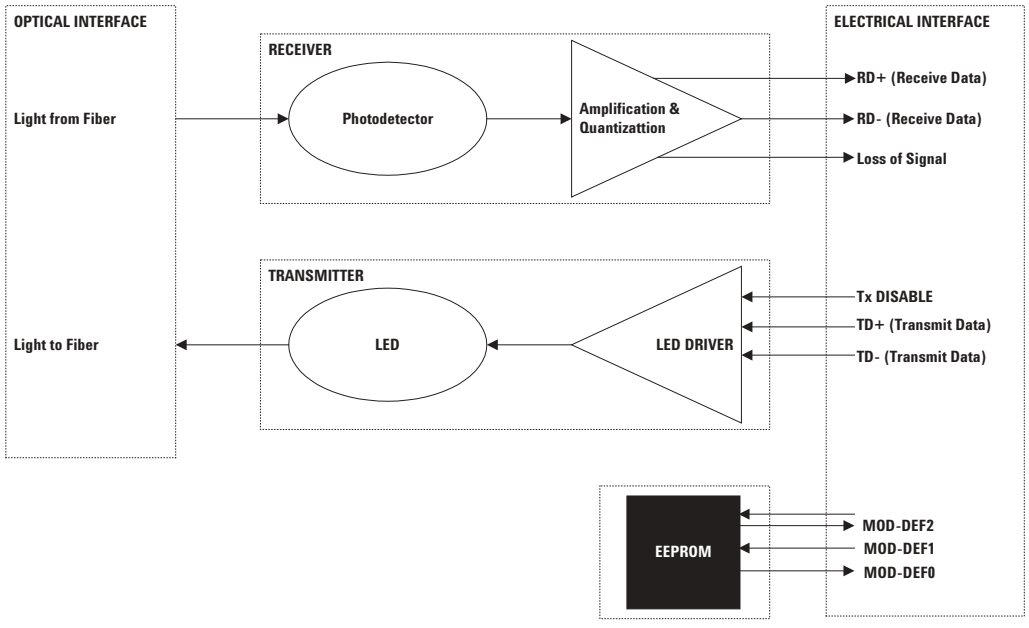


Figure 1. Transceiver functional diagram

Installation

The HFBR-5764AP can be installed in or removed from any MultiSource Agreement (MSA) – compliant Small Form Pluggable port regardless of whether the host equipment is operating or not. The module is simply inserted, electrical interface first, under finger pressure. Controlled hot-plugging is ensured by design and by 3-stage pin sequencing at the electrical interface. The module housing makes initial contact with the host board EMI shield mitigating potential damage due to Electro-Static Discharge (ESD). The 3-stage pin contact sequencing involves (1) Ground, (2) Power, and then (3) Signal pins, making contact with the host board surface mount connector in that order. This printed circuit board card-edge connector is depicted in Figure 2.

Serial Identification (EEPROM)

The HFBR-5764AP complies with the industry standard MSA that defines the serial identification protocol. This protocol uses the 2-wire serial CMOS E2PROM protocol of the ATMEL AT24C01A or equivalent. The contents of the HFBR-5764AP serial ID memory are defined in Table 3 as specified in the SFP MSA.

Functional Data I/O

The HFBR-5764AP fiberoptic transceiver is designed to accept industry standard differential signals. In order to reduce the number of passive components required on the customer's board, Avago Technologies has included the functionality of the transmitter bias resistors and coupling capacitors within the fiberoptic module. The transceiver is compatible with an "ac-coupled" configuration and is internally terminated. Figure 5 depicts the functional diagram of the HFBR-5764AP.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions in which immunity to ESD damage is important. Table 1 documents our immunity to both of these conditions. The first condition is during handling of the transceiver prior to insertion into the transceiver port. To protect the transceiver, it is important to use normal ESD handling precautions.

These precautions include using grounded wrist straps, workbenches, and floor mats in ESD controlled areas. The ESD sensitivity of the HFBR-5764AP is compatible with typical industry production environments. The second condition is static discharges to the exterior of the host equipment chassis after installation. To the extent that the duplex LC optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements. The ESD performance of the HFBR-5764AP exceeds typical industry standards.

Immunity

Equipment hosting the HFBR-5764AP modules will be subjected to radio-frequency electro magnetic fields in some environments. These transceivers have good immunity to such fields due to their shielded design.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C	Meets Class 2 (2000 to 3999 Volts). Withstand up to 2200 V applied between electrical pins.
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the LC connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 Class B (CISPR 21) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 450 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	AEL Class 1 EN60825-1 (+A11)	Compliant per Avago Technologies testing under single fault conditions. TUV Certification: R02071015.0007

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The metal housing and shielded design of the HFBR-5764AP minimize the EMI challenge facing the host equipment designer. These transceivers provide superior EMI performance. This greatly assists the designer in the management of the overall system EMI performance.

Eye Safety

These transceivers provide Class 1 eye safety by design. Avago Technologies has tested the transceiver design for compliance with the requirements listed in Table 1 under normal operating conditions and under a single fault condition.

Flammability

The HFBR-5764AP transceiver housing is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiberoptic link to accommodate fiber cable loses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Avago Technologies LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The 1300 nm Avago Technologies LEDs are specified to experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Avago Technologies sales representative for additional details.

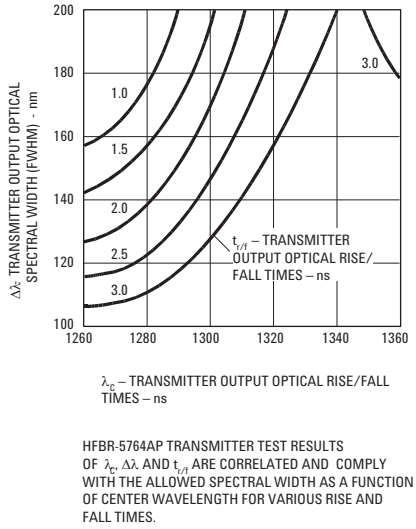


Figure 3. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times

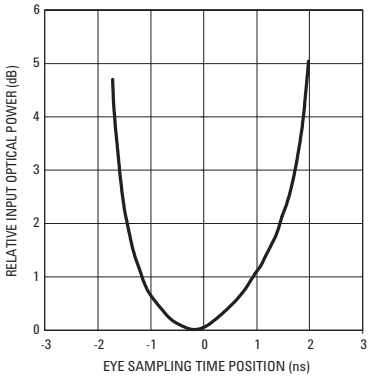


Figure 4. Relative Input Optical Power vs. Eye Sampling Time Position

Ordering Information

The HFBR-5764AP 1300 nm product is available for production orders through the Avago Technologies Component Field Sales Offices and Authorized Distributors worldwide.

For technical information regarding this product, please visit Avago Technologies website at www.avagotech,com

Use the quick search feature to search for this part number. You may also contact Avago Technologies Customer Response Centre.

Applications Support Materials

Contact your local Avago Technologies Component Field Sales Office for information on how to obtain PCB layouts and evaluation boards for the transceivers.

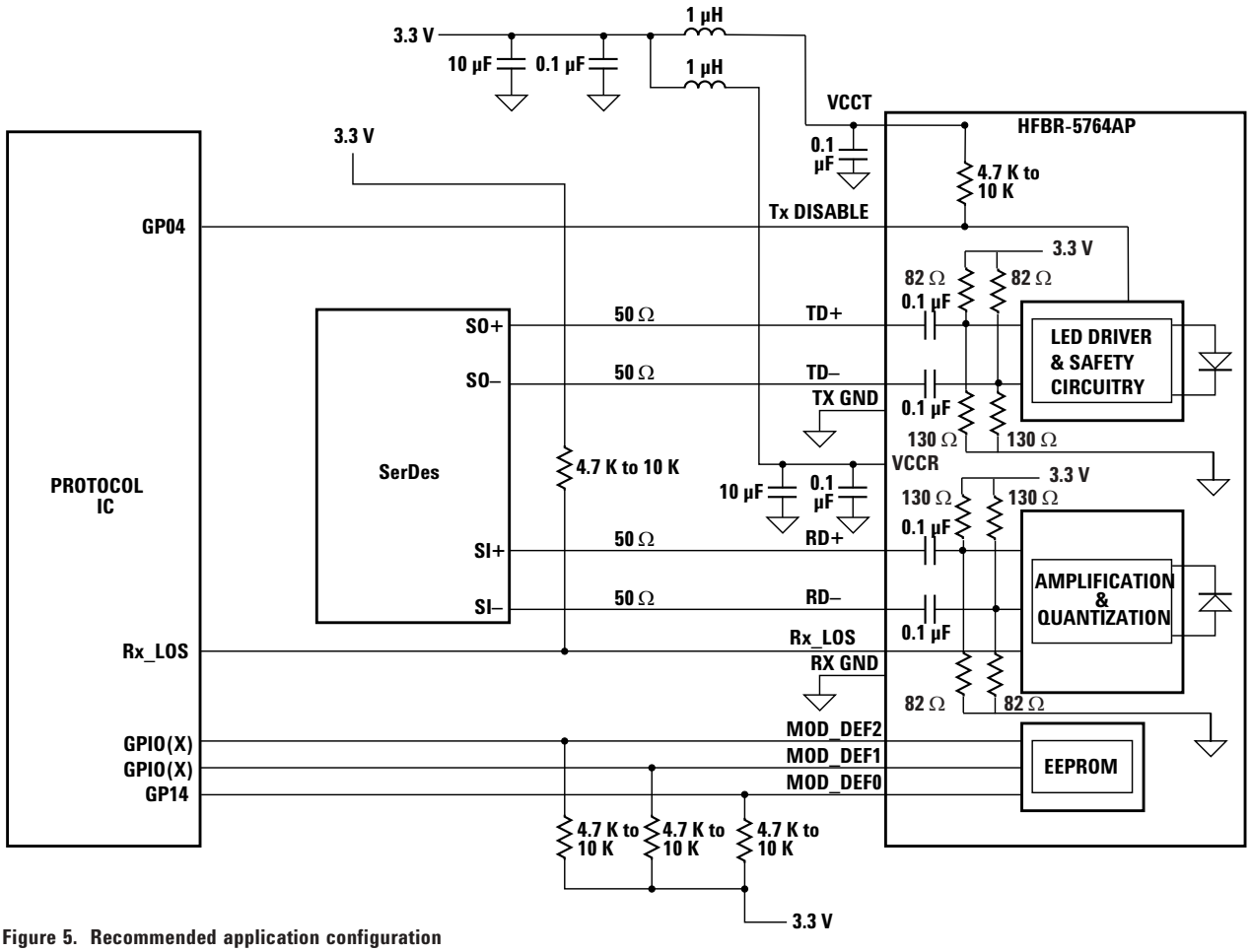
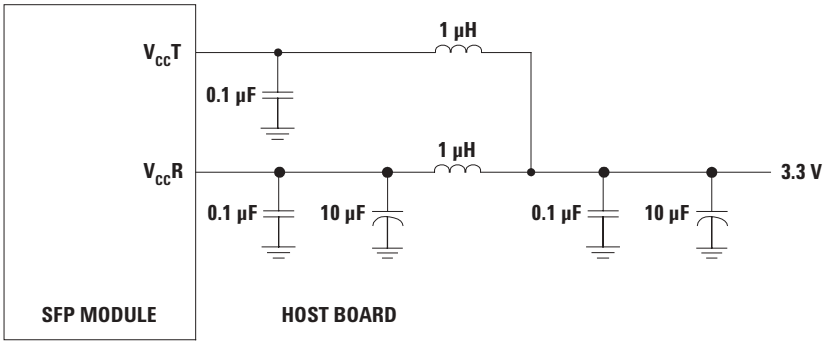


Figure 5. Recommended application configuration



Note: Inductors must have less than 1 ohm series resistance per MSA.

Figure 6. MSA required power supply filter

Table 2. Pin Description

Pin	Name	Function/Description	MSA Notes
1	$V_{EE}T$	Transmitter Ground	
2	NC	NC	
3	Tx DISABLE	Transmitter Disable - Module Disables on High or Open	1
4	MOD-DEF2	Module Definition 2 - Two Wire Serial ID Interface	2
5	MOD-DEF1	Module Definition 1 - Two Wire Serial ID Interface	2
6	MOD-DEF0	Module Definition 0 - grounded in module	2
7	NC	NC	
8	LOS	Loss of Signal - high indicates loss of signal	3
9	$V_{EE}R$	Receiver Ground	
10	$V_{EE}R$	Receiver Ground	
11	$V_{EE}R$	Receiver Ground	
12	RD-	Inverse Received Data Out	4
13	RD+	Received Data Out	4
14	$V_{EE}R$	Receiver Ground	
15	$V_{CC}R$	Receiver Power -3.3 V ± 10%	5
16	$V_{CC}T$	Transmitter Power -3.3 V ± 10%	5
17	$V_{EE}T$	Transmitter Ground	
18	TD+	Transmitter Data In	6
19	TD-	Inverse Transmitter Data In	6
20	$V_{EE}T$	Transmitter Ground	

Notes:

1. Tx disable input is used to shut down the LED output per the state table below. It is pulled up within the module with a 4.7 K - 10 KΩ resistor.
   - Low (0 - 0.8 V): Transmitter On
   - Between (0.8 V and 2.0 V): Undefined
   - High (2.0 - 3.63 V): Transmitter Disabled
   - Open: Transmitter Disabled
2. Mod-Def 0, 1, 2. are the module definition pins. They should be pulled up with a 4.7 K - 10 KΩ resistor on the host board to a supply less than $V_{CC}T$ +0.3 V or $V_{CC}R$ +0.3 V.
   - Mod-Def 0 is grounded by the module to indicate that the module is present.
   - Mod-Def 1 is clock line of two wire serial interface for optional serial ID.
   - Mod-Def 2 is data line of two wire serial interface for optional serial ID.
3. LOS (Loss of Signal) is an open collector/drain output which should be pulled up externally with a 4.7 - 10 KΩ resistor on the host board to a supply < $V_{CC}T$, R +0.3 V. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to <0.8 V.
4. RD-/+: These are the differential receiver outputs. They are ac coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the SERDES. The ac coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 2000 mV differential (200 - 1000 mV single ended) when properly terminated.
5. $V_{CC}R$ and $V_{CC}T$ are the receiver and transmitter power supplies. They are defined as 2.97 - 3.63 V at the SFP connector pin. The maximum supply current is 360 mA and the associated in-rush current will typically be no more than 30 mA above steady state after 500 nanoseconds.
6. TD-/+: These are the differential transmitter inputs. They are ac coupled differential lines with 100 Ω differential termination inside the module. The ac coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 400 - 2000 mV (200 - 1000 mV single ended), though it is recommended that values between 400 and 1200 mV differential (200 - 600 mV single ended) be used for best EMI performance. These levels are compatible with CML and LVPECL voltage swings.

Table 3. EEPROM Serial ID Memory Contents

Add	Hex	ASCII	Add	Hex	ASCII	Add	Hex	ASCII	Add	Hex	ASCII
0	03		34	20		68	Note 1		96	Note 4	
1	04		35	20		69	Note 1		97	Note 4	
2	07		36	00		70	Note 1		98	Note 4	
3	00		37	00		71	Note 1		99	Note 4	
4	80		38	30		72	Note 1		100	Note 4	
5	00		39	D3		73	Note 1		101	Note 4	
6	00		40	48	H	74	Note 1		102	Note 4	
7	00		41	46	F	75	Note 1		103	Note 4	
8	00		42	42	B	76	Note 1		104	Note 4	
9	00		43	52	R	77	Note 1		105	Note 4	
10	00		44	2D	-	78	Note 1		106	Note 4	
11	01		45	35	5	79	Note 1		107	Note 4	
12	02		46	37	7	80	Note 1		108	Note 4	
13	00		47	36	6	81	Note 1		109	Note 4	
14	00		48	34	4	82	Note 1		110	Note 4	
15	00		49	41	A	83	Note 1		111	Note 4	
16	C8		50	50	P	84	Note 2		112	Note 4	
17	C8		51	20		85	Note 2		113	Note 4	
18	00		52	20		86	Note 2		114	Note 4	
19	00		53	20		87	Note 2		115	Note 4	
20	41	A	54	20		88	Note 2		116	Note 4	
21	47	G	55	20		89	Note 2		117	Note 4	
22	49	I	56	20		90	Note 2		118	Note 4	
23	4C	L	57	20		91	Note 2		119	Note 4	
24	45	E	58	20		92	00		120	Note 4	
25	4E	N	59	20		93	00		121	Note 4	
26	54	T	60	05		94	00		122	Note 4	
27	20		61	1E		95	Note 3		123	Note 4	
28	20		62	00					124	Note 4	
29	20		63	Note 3					125	Note 4	
30	20		64	00					126	Note 4	
31	20		65	12					127	Note 4	
32	20		66	00							
33	20		67	00							

Notes:

1. Addresses 68 - 83 specify a unique identifier.
2. Addresses 84 - 91 specify the date code.
3. Addresses 63 and 95 are check sums. Address 63 is the check sum for bytes 0 - 62 and address 95 is the check sum for bytes 64 - 94.
4. Addresses 96-127 are vendor specific data.

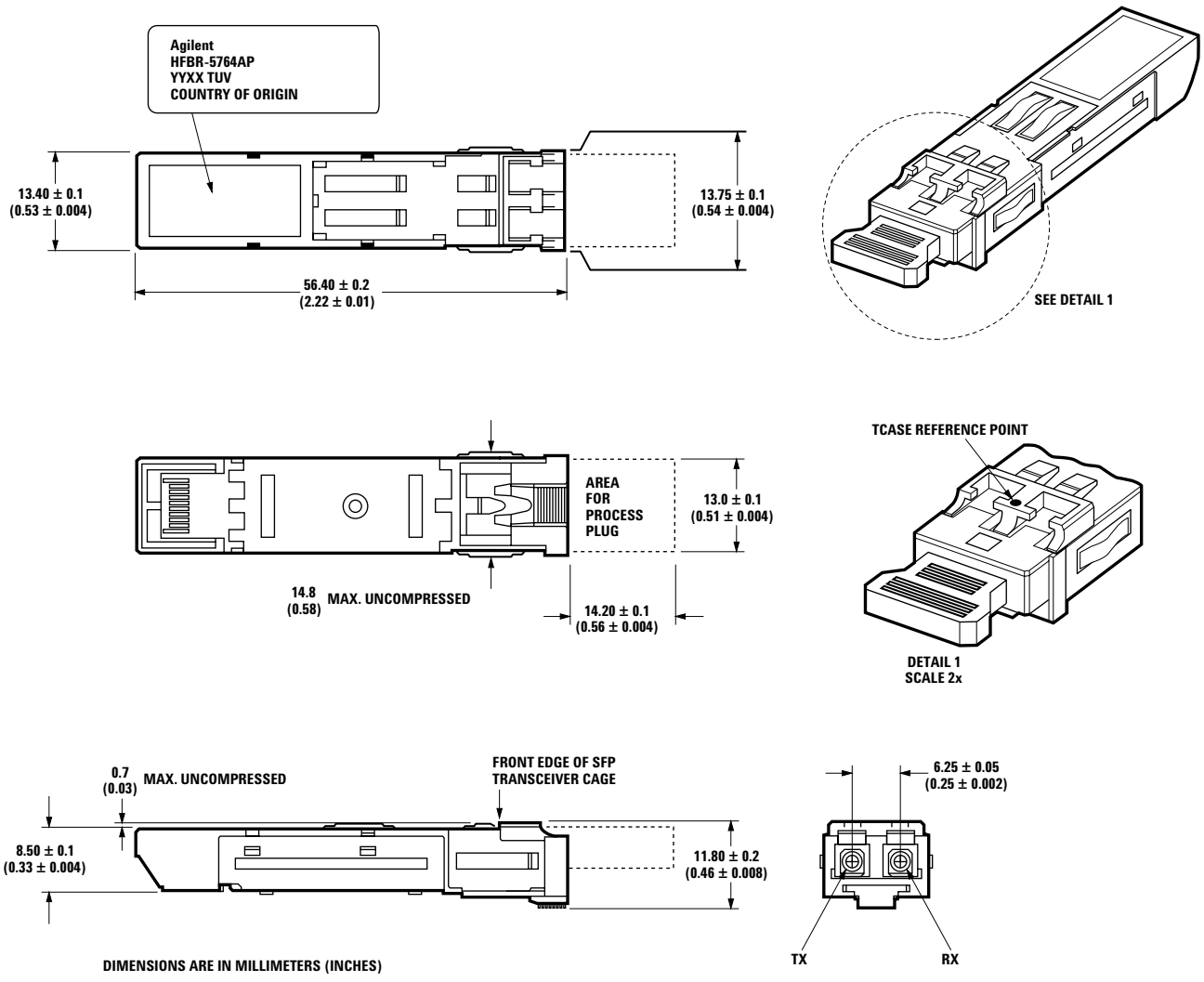
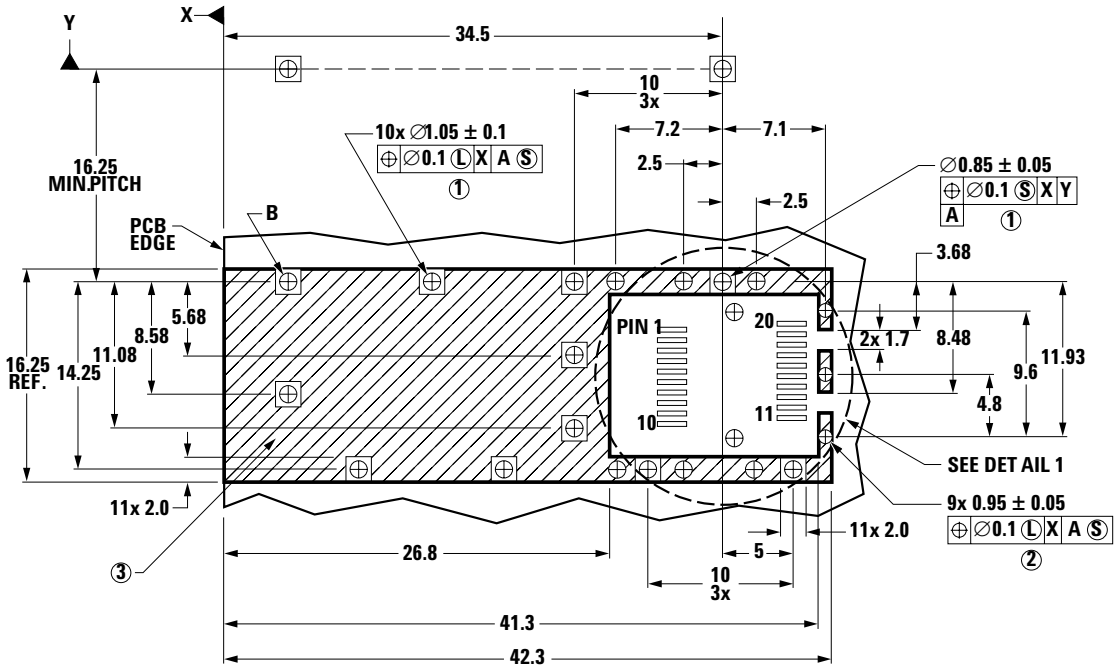
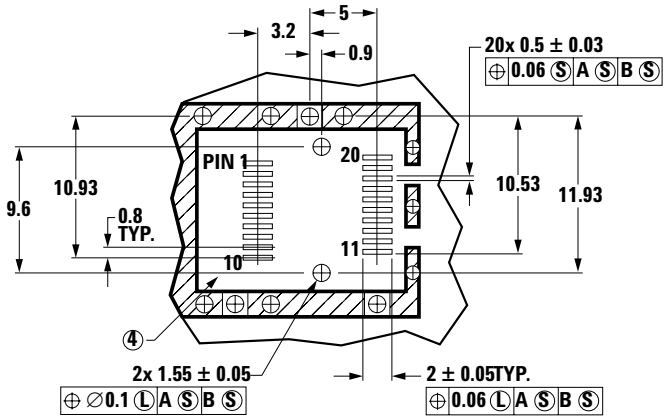


Figure 7a. Module drawing





DETAIL 1

NOTES:

1. PADS ANDVIAS ARE CHASSIS GROUND.
2. THROUGH HOLES, PLATING OPTIONAL.
3. HATCHED AREA DENO TES COMPONENT ANDTRACE KEEPOUT (EXCEPT CHASSIS GROUND).
4. AREA DENOTES COMPONENT KEEPOUT (TRA CES ALLO WED).

DIMENSIONS ARE IN MILLIMETERS

Figure 7b. SFP host board mechanical layout

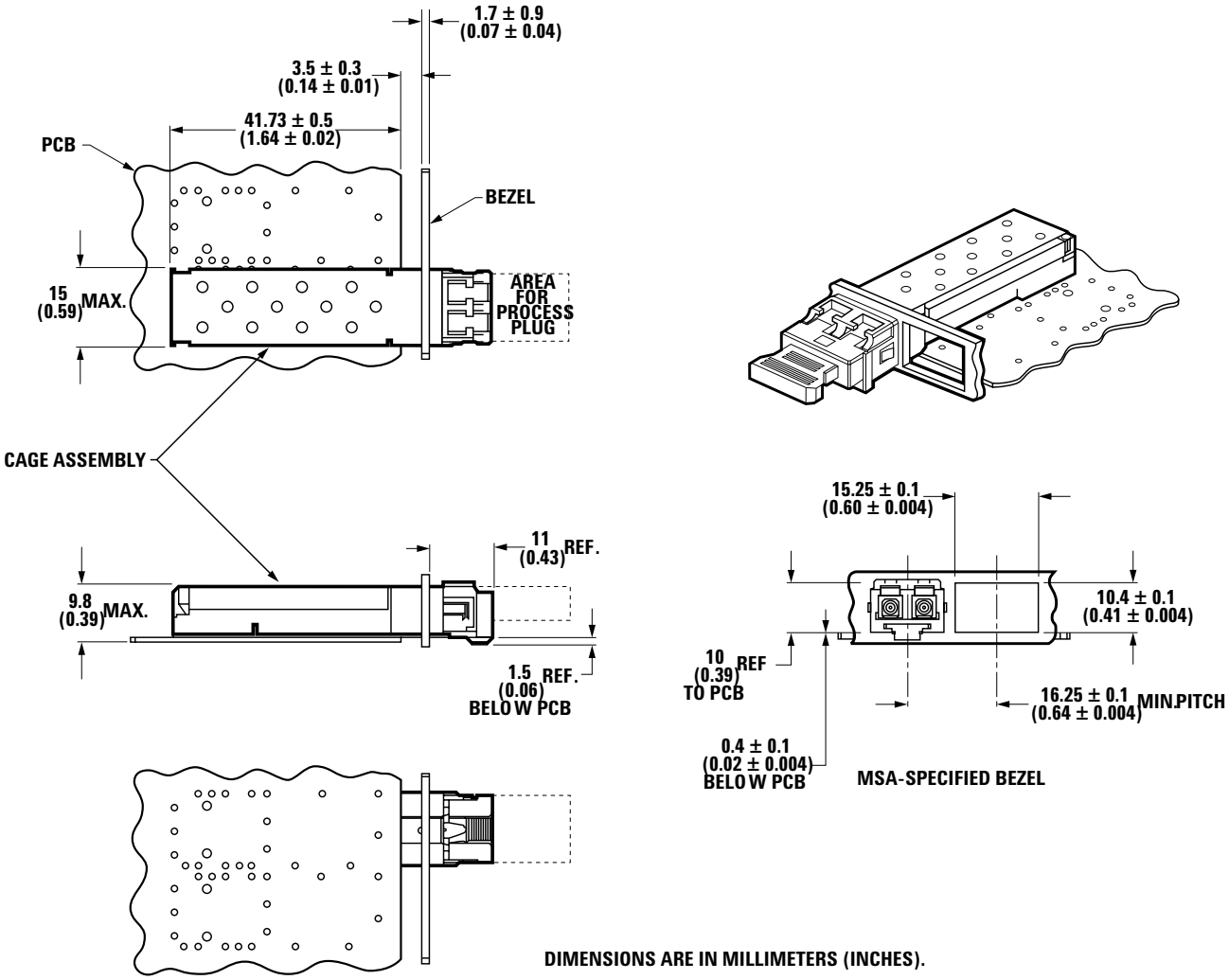


Figure 7c. Assembly drawing

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Storage Temperature	T_S	-40		+100	°C	
Supply Voltage	V_{CC}	-0.5		3.63	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage (p-p)	V_D			2.0	V	1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Case Operating Temperature	T_C	-20		+85	°C	
Supply Voltage	V_{CC}	2.97	3.3	3.63	V	
Data Input: Transmitter Differential Input Voltage (TD+/-)	V_I	0.4		2.0	V	
Data Output Load	R_L		50		Ω	

Transmitter Electrical Characteristics

HFBR-5764AP (T_C = -20 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}		165	210	mA	2
Power Dissipation	P_{DISS}		0.55	0.77	W	4a
Transmitter Disable Input Voltage - Low	V_{IL}	0		0.8	V	
Transmitter Disable Input Voltage - High	V_{IH}	2.0		V_{CC}	V	
Transmitter Disable Assert Time	t_off			10	µs	20
Transmitter Disable Deassert Time	t_on			1	ms	21

Receiver Electrical Characteristics

HFBR-5764AP (T_C = -20 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}		95	150	mA	3
Power Dissipation	P_{DISS}		0.32	0.55	W	4b
Data Output: Receiver Differential Output Voltage (RD+/-)	V_O	0.4		2.0	V	5
Data Output Rise Time	t_r	0.35		1.3	ns	6
Data Output Fall Time	t_f	0.35		1.3	ns	6
Loss of Signal Output Voltage - Low	$LOSV_{OL}$			0.8	V	5
Loss of Signal Output Voltage - High	$LOSV_{OH}$	2.0			V	5
Power Supply Noise Rejection	PSNR		50		mV	

Transmitter Optical Characteristics

HFBR-5764AP (T_C = -20 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Output Optical Power BOL 62.5/125 µm, NA = 0.275 Fiber EOL	P_0	-19.5 -20.5	-15.7	-14	dBm avg	7
Optical Extinction Ratio	ER	8			dB	8
Center Wavelength	λ_C	1280		1380	nm	Figure 3
Spectral Width - FWHM	$\Delta\lambda$		147	175	nm	8
Optical Rise Time	t_r		1.0	1.7	ns	9, 10 Figure 3
Optical Fall Time	t_f		1.2	1.7	ns	9, 10 Figure 3
Total Jitter	TJ		0.2	0.8	ns	11

Receiver Optical and Electrical Characteristics

HFBR-5764AP (T_C = -20 °C to +85 °C, V_{CC} = 2.97 V to 3.63 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Input Optical Power minimum at Window Edge	$P_{IN\ MIN}$ (W)			$P_{IN\ MIN}$(C) + 1dB	dBm avg	12, Figure 4
Input Optical Power minimum at Eye Center	$P_{IN\ MIN}$ (C)			-29	dBm avg	13, Figure 4
Input Optical Power Maximum	$P_{IN\ MAX}$	-14			dBm avg	12
Operating Wavelength	λ	1280		1380	nm	
Systematic Jitter Contributed by the Receiver	SJ		0.2	1.0	ns	14
Eye-Width	t_{ew}	1.4			ns	15
Loss of Signal - Asserted	P_A	-45		-36	dBm avg	16
Loss of Signal - Deasserted	P_D	-44.5		-35.5	dBm avg	16
Loss of Signal - Hysteresis	$P_D - P_A$	0.5		4.0	dB	17
Loss of Signal Assert Time (off to on)		0	5	500	µs	18
Loss of Signal Deassert Time (on to off)		0	2	500	µs	19

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
3. This is the receiver supply current measured in mA.

4a. The power dissipation of the transmitter is calculated as the sum of the products of supply voltage and currents.

4b. The power dissipation of the receiver is calculated as the sum of the products of supply voltage and currents.

5. Differential Output Voltage is internally ac coupled. The Loss of Signal low and high voltages are measured with load condition of 4.7 KΩ tied to V_{CC}.
6. The data output rise and fall times are measured between 20% and 80% levels.
7. These optical power values are measured with the following conditions:

   The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Avago Technologies 1300 nm LED products is < 1 dB, as specified in this data sheet. Over the specified operating voltage and temperature ranges. With 200 MBd (100 MHz square-wave), input signal.
8. The Extinction Ratio is a measure of the modulation depth of the optical signal. With the transmitter driven by a 25MHz square wave signal, the Extinction Ratio is the ratio of the optical power at the "1" level compared to the optical power at the "0" level expressed in decibels.
9. Input Conditions: 25MHz, square wave signal, input voltages are in the range specified for V_I and input signal rise and fall times of 0.35 to 1.3ns (20-80%) at the transmitter input pins.
10. Optical rise and fall times are measured between 20% and 80% levels.
11. Transmitter Total Jitter is equal to the sum of Systematic Jitter (SJ) and Random Jitter (RJ). Systematic Jitter is measured at 50% threshold using a 200Mbd, PRBS 2^7-1 data pattern input signal. Random Jitter is specified with a 200 MBd square wave input signal.
12. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following conditions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 10^{-12}.
    - At the Beginning of Life (BOL).
    - Over the specified operating temperature and voltage ranges.
    - Receiver data window time-width is 1.4 ns or greater and centered at mid-symbol.
    - Input signal is 200 MBd, Pseudo Random-Bit-Stream 2^7-1 data pattern.
    - Transmitter cross-talk effects have been included in Receiver sensitivity. Transmitter should be running at 50% duty cycle (nominal) between 8 - 200 Mb/s, while Receiver sensitivity is measured.
13. All conditions of note 12 apply except that the measurement is made at the center of the symbol with no window time-width and with a BER better than or equal to 10^{-15}.
14. The receiver systematic jitter specification applies to optical powers between –14.5 dBm avg. to –27.0 dBm avg. at the receiver. Receiver Systematic Jitter is equal to the sum of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ). DCD is equivalent to Pulse-Width Distortion (PWD). Systematic Jitter is measured at the 50% signal level with 200 MBd, PRBS 2^7-1 electrical output data pattern.
15. Eye-width specified defines the minimum clock time-position range, centered around the center of the 5 ns baud interval, at which the BER must be 10^{-12} or better. Test data pattern is PRBS 2^7-1. The typical change in input optical power to open the eye to 1.4 nsec from a closed eye is less than 1.0 dB.
16. Loss of Signal switching thresholds: Direction of decreasing optical power:
    If Power >–36.0 dBm avg., then LOS = 0 (low)
    If Power <–45.0 dBm avg., then LOS = 1 (high)
    Direction of increasing optical power:
    If Power <–44.5 dBm avg., then LOS = 1 (high)
    If Power >–35.5 dBm avg., then LOS = 0 (low)
17. Loss of Signal Hysteresis is the difference in low-to-high and high-to-low switching thresholds. Thresholds must lie within optical power limits specified. The Hysteresis is desired to avoid Loss of Signal chatter when the optical input is near the threshold.
18. Loss of Signal output shall be asserted within 500 µs after a step decrease in the Input Optical Power. The step will be from a high input optical power > -36.0dBm avg. to < -45.0 dBm avg. At Loss of Signal Assert, the receiver outputs Data Out and Data Out Bar go to steady DC states.
19. The Loss of Signal output shall be de-asserted within 500 µs after a step increase of the Input Optical Power. This step will be from a low Input Optical Power < -44.5dBm avg to > -35.5dBm avg.
20. Time from rising edge of Tx Disable to when the optical output falls below 10% of nominal.
21. Time from falling edge of Tx Disable to when the modulated optical output rises above 90% of nominal.

Ordering Information

1300 nm LED (Operating Case Temperature -20 °C to +85 °C)

HFBR-5764AP Bail De-latch

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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