HFBR-5701L/LP

Small Form Factor Pluggable Optical Transceiver
for Gigabit Ethernet (1.25 GBd) and Fibre Channel (1.0625 GBd)

Data Sheet



Description

The HFBR-5701L optical transceiver is compliant with the specifications set forth in the IEEE802.3 (1000BASE-SX), Fibre Channel (100-M5-SN-I, 100-M6-SN-I), and the Small Form-Factor Pluggable (SFP) Multi-Source Agreement (MSA). Its primary application is servicing Gigabit Ethernet and Fibre Channel links between optical networking equipment. It offers previously unavailable system cost, upgrade, and reliability benefits by virtue of being hot-pluggable. Further, it incorporates the latest 3.3 VDC compatible transceiver technology including an 850 nm VCSEL transmitter as well as a convenient LC-Duplex optical interface.

Related Products

- HFBR-5710L: 1.25 GBd Ethernet (1000BASE-SX) SFP
- HFBR-5720L: 2.125 GBd Fibre Channel (200-M5-SN-I, 200-M6-SN-I) Multi-Mode SFP
- HFBR-5730L: 1.0625 GBd Fibre Channel (100-M5-SN-I, 100-M6-SN-I) Multi-Mode SFP
- HDMP-1687: Quad Channel SerDes IC 1.25 GBd Ethernet
- HDMP-1646A: Single Channel SerDes IC for 1.25 GBd Ethernet and 1.0625 GBd Fibre Channel

Features

- IEEE 802.3 Gigabit Ethernet (1.25 GBd) 1000BASE-SX compliant Fibre Channel (100-M5-SN-I, 100-M6-SN-I) compliant
- Small Form Factor Pluggable (SFP) Multi-Source Agreement (MSA) compliant
- Manufactured in an ISO 9001 compliant facility
- Hot-pluggable
- Optional extended de-latch for high density applications as shown in Figure 10
  - HFBR-5701LP bail-wire pull de-latch
  - HFBR-5701L standard de-latch
- +3.3 V DC power supply
- Industry leading EMI performance for high port density
- 850 nm Vertical Cavity Surface Emitting Laser (VCSEL)
- Eye safety certified:
  - US 21 CFR(J)
  - EN 60825-1 (+All)
- LC-Duplex fiber connector compliant
- Fiber compatibility:
  - 2 to 550 meters with 50/125 µm fiber
  - 2 to 275 meters with 62.5/125 µm fiber

Applications

- Switch to switch interface
- Switched backplane applications
- File server interface
- iSCSI applications

Patent - www.avagotech.com/patents

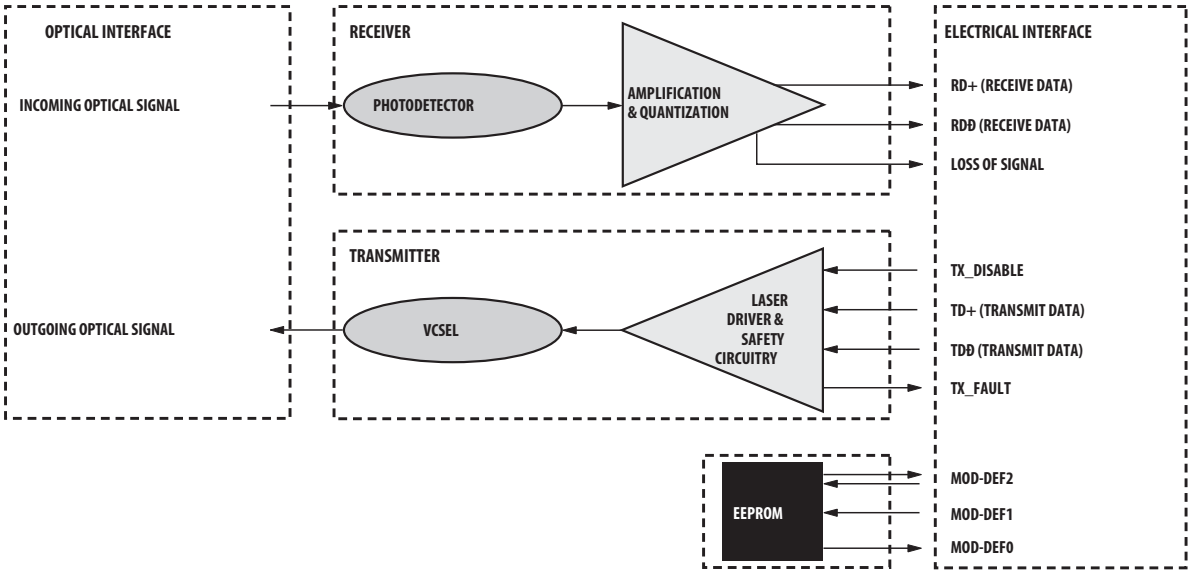


Figure 1. HFBR-5701L block diagram.

Overview

The HFBR-5701L offers maximum flexibility to designers, manufacturers, and operators of Gigabit Ethernet networking equipment. A pluggable architecture allows the module to be installed into MSA standard SFP ports at any time – even with the host equipment operating and online. This facilitates the rapid configuration of equipment to precisely the user's needs – reducing inventory costs and network downtime. Compared with traditional transceivers, the size of the Small Form Factor package enables higher port densities.

Module Diagrams

Figure 1 illustrates the major functional components of the HFBR-5701L. The external configuration of the module is depicted in Figure 7. Figure 8 depicts the panel and host board footprints.

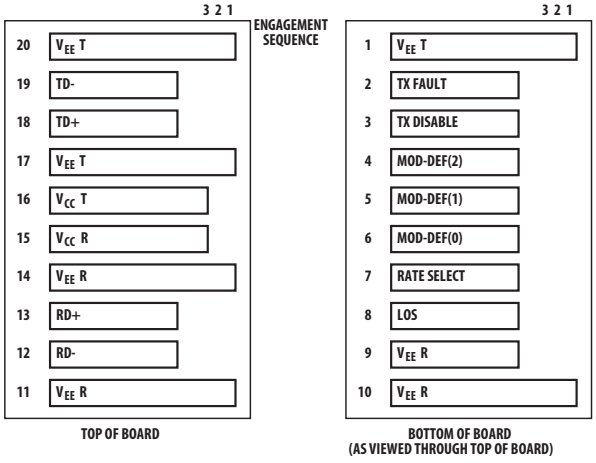


Figure 2. Pin description of the SFP electrical interface.

Installation

The HFBR-5701L can be installed in or removed from any MSA-compliant Pluggable Small Form Factor port regardless of whether the host equipment is operating or not. The module is simply inserted, electrical-interface first, under finger-pressure. Controlled hot-plugging is ensured by 3-stage pin sequencing at the electrical interface. This printed circuit board card-edge connector is depicted in Figure 2.

As the HFBR-5701L is inserted, first contact is made by the housing ground shield, discharging any potentially component-damaging static electricity. Ground pins engage next and are followed by Tx and Rx power supplies. Finally, signal lines are connected. Pin functions and sequencing are listed in Table 2.

Before extracting the module, the black plastic tab beneath the optical port must be depressed, releasing the latch mechanism. The transceiver can then be pulled out of the port manually by gripping the side of the LC ports.

For easier fingertip delatching in high port density applications, an optional extended tab is offered as shown in Figure 10.

Serial Identification (EEPROM)

The HFBR-5701L features an EEPROM for Serial ID. It contains the product data stored for retrieval by host equipment. This data is accessed via the 2-wire serial EEPROM protocol of the ATMEL AT24C01A or similar in compliance with the industry standard SFP Multi-Source Agreement. Contents of the HFBR-5701L serial ID memory are displayed in Table 9.

Transmitter Section

The transmitter section includes the Transmitter Optical Subassembly (TOSA) and laser driver circuitry. The TOSA, containing an 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) light source, is located at the optical interface and mates with the LC optical connector. The TOSA is driven by a custom IC, which converts differential logic signals into an analog laser diode drive current. This Tx driver circuit regulates the optical power at a constant level provided the data pattern is DC balanced (8B10B code for example).

Tx Disable

The HFBR-5701L accepts a transmit disable control signal input which shuts down the transmitter. A high signal implements this function while a low signal allows normal laser operation. In the event of a fault (e.g., eye safety circuit activated), cycling this control signal resets the module as depicted in Figure 6.

Eye Safety Circuit

The HFBR-5701L provides Class 1 eye safety by design and has been tested for compliance with the requirements listed in Table 1. The eye safety circuit continuously monitors optical output power levels and will disable the transmitter and assert a TX_FAULT signal upon detecting an unsafe condition. Such unsafe conditions can be created by inputs from the host board (Vcc fluxuation, unbalanced code) or faults within the module.

Receiver Section

The receiver section includes the Receiver Optical Subassembly (ROSA) and amplification/quantization circuitry. The ROSA, containing a PIN photodiode and custom transimpedance preamplifier, is located at the optical interface and mates with the LC optical connector. The ROSA is mated to a custom IC that provides post-amplification and quantization. Also included is a Loss Of Signal (LOS) detection circuit.

Loss of Signal

The Loss Of Signal (LOS) output indicates an unusable optical input power level. A high LOS output signal indicates a loss of signal while a low LOS output signal indicates normal operation. The Loss Of Signal thresholds are set to indicate a definite optical fault has occurred (e.g., disconnected or broken fiber connection to receiver, failed transmitter, etc.).

Functional I/O

The HFBR-5701L accepts industry standard differential signals such as LVPECL and CML within the scope of the SFP MSA. To simplify board requirements, transmitter bias resistors and coupling capacitors are incorporated into the transceiver module. The module is "ac-coupled" and internally terminated.

Figure 4 illustrates a recommended interface circuit to link the HFBR-5701L to the supporting Physical Layer integrated circuits.

Timing diagrams for the MSA compliant control signals implemented in this module are depicted in Figure 6.

Required Host Board Components

The MSA power supply noise rejection filter is required on the host PCB to meet data sheet performance. The MSA filter incorporates an inductor which should be rated 400 mADC and 1 Ω series resistance or better. It should not be replaced with a ferrite. The required filter is illustrated in Figure 3.

The MSA also specifies that 4.7 K to 10 KΩ pull-up resistors for TX_FAULT, LOS, and MOD_DEF0,1,2 are required on the host PCB.

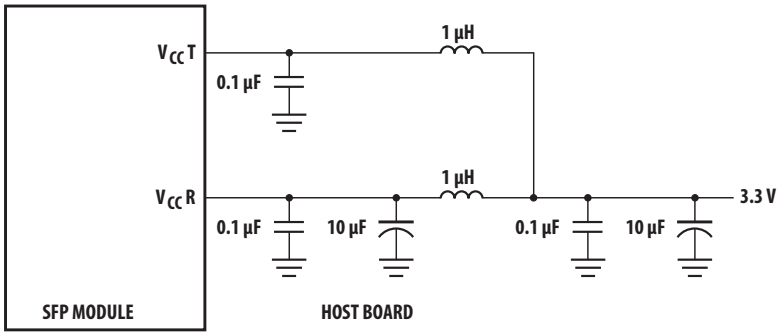


Figure 3. MSA required power supply filter.

Application Support

Evaluation Kit

To assist in the transceiver evaluation process, Avago offers a 1.25 Gbd Gigabit Ethernet evaluation board which facilitates testing of the HFBR-5701L. It can be obtained through the Avago Field Organization by referencing Avago part number HFBR-0571.

Reference Designs

A Reference Design including the HFBR-5701L and the HDMP-1687 GigaBit Quad SerDes is available. It may be obtained through the Avago Field Sales organization.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to insertion into the transceiver port. To protect the transceiver, it's important to use normal ESD handling precautions. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The ESD sensitivity of the HFBR-5701L is compatible with typical industry production environments.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. To the extent that the optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements.

Immunity

The ESD performance of the HFBR-5701L exceeds typical industry standards.

Equipment hosting HFBR-5701L modules will be subjected to radio-frequency electromagnetic fields in some environments. The transceiver has good immunity to such fields due to its shielded design.

Electromagnetic Interference (EMI)

Equipment incorporating Gigabit Ethernet transceivers is typically required to meet the requirements of the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe, and VCCI in Japan.

The metal housing and shielded design of the HFBR-5701L minimize the EMI challenge facing the host equipment designer.

Flammability

The HFBR-5701L transceiver is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Caution

There are no user serviceable parts nor any maintenance required for the HFBR-5701L. All adjustments are made at the factory before shipment to our customers. Tampering with, modifying, misusing or improperly handling the HFBR-5701L will void the product warranty. It may also result in improper operation of the HFBR-5701L circuitry, and possible overstress of the laser source. Device degradation or Product failure may result. Connection of the HFBR-5701L to a non-Gigabit Ethernet-compliant optical source, operating above the recommended absolute maximum conditions or operating the HFBR-5701L in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product. The person(s) performing such an act is required by law to re-certify and re-identify the laser product under the provisions of U.S. 21 CFR (Subchapter J).

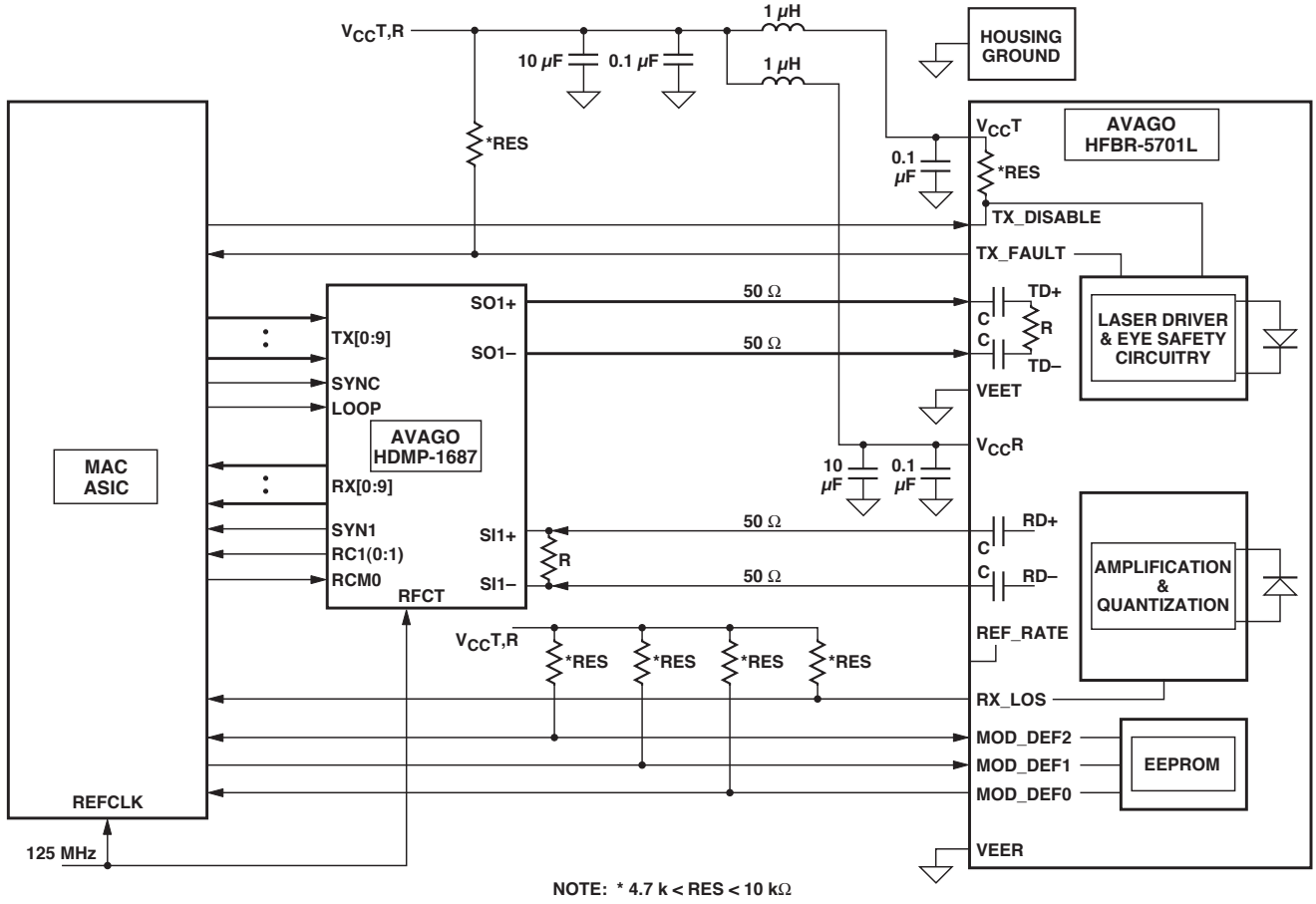


Figure 4. Typical application configuration.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	JEDEC/EIA JESD22-A114-A	Class 2 (> +2000 Volts)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 6100-4-2	Typically withstands at least 25 kV without damage when the duplex LC connector receptacle is contacted by a Human Body Model probe
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	Applications with high SFP port counts are expected to be compliant; however, margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 1000 MHz applied to the transceiver without a chassis enclosure.
Eye Safety[1]	US FDA CDRH AEL Class 1 EN(IEC)60825-1,2, EN60950 Class 1	CDRH certification #9720151-13 TUV file #E9971083.07
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment	UL File #E173874

Note:

1. Changes to IEC 60825-1,2 are currently anticipated to allow higher eye-safe Optical Output Power levels. Avago may choose to take advantage of these in future revisions to this part.

Table 2. Pin Description

Pin	Name	Function/Description	Engagement Order (insertion)	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	1
3	TX Disable	Transmitter Disable - Module disables on high or open	3	2
4	MOD-DEF2	Module Definition 2 - Two wire serial ID interface	3	3
5	MOD-DEF1	Module Definition 1 - Two wire serial ID interface	3	3
6	MOD-DEF0	Module Definition 0 - Grounded in module	3	3
7	Rate Select	Not Connected	3	
8	LOS	Loss of Signal	3	4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inverse Received Data Out	3	5
13	RD+	Received Data Out	3	5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power - 3.3 V ± 5%	2	6
16	VccT	Transmitter Power - 3.3 V ± 5%	2	6
17	VeeT	Transmitter Ground	1	
18	TD+	Transmitter Data In	3	7
19	TD-	Inverse Transmitter Data In	3	7
20	VeeT	Transmitter Ground	1	

Notes:

1. TX Fault is an open collector/drain output which should be pulled up externally with a 4.7K – 10 KΩ resistor on the host board to a supply < VccT+0.3 V or VccR+0.3 V. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
2. TX disable input is used to shut down the laser output per the state table below. It is pulled up within the module with a 4.7-10 K resistor.
   Low (0 – 0.8 V): Transmitter on
   Between (0.8 V and 2.0 V): Undefined
   High (2.0 – 3.465 V): Transmitter Disabled
   Open: Transmitter Disabled
3. Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7-10 KΩ resistor on the host board to a supply less than VccT +0.3 V or VccR+0.3 V.
   Mod-Def 0 is grounded by the module to indicate that the module is present
   Mod-Def 1 is clock line of two wire serial interface for optional serial ID
   Mod-Def 2 is data line of two wire serial interface for optional serial ID
4. LOS (Loss of Signal) is an open collector/drain output which should be pulled up externally with a 4.7 K – 10 KΩ resistor on the host board to a supply < VccT,R+0.3 V. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operatio0n. In the low state, the output will be pulled to < 0.8 V.
5. RD-/+: These are the differential receiver outputs. They are AC coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines must be between 370 and 2000 mV differential (185 – 1000 mV single ended) according to the MSA. Typically it will be 1500mv differential.
6. VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.135 – 3.465 V at the SFP connector pin. The in-rush current will typically be no more than 30 mA above steady state supply current after 500 nanoseconds.
7. TD-/+: These are the differential transmitter inputs. They are AC coupled differential lines with 100 Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 – 2400 mV (250 – 1200 mV single ended). However, the applicable recommended differential voltage swing is found in Table 5.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Ambient Storage Temperature (Non-Operating)	Ts	–40	+100	°C	1
Case Temperature	T_C	–40	+85	°C	1
Relative Humidity	RH	5	95	%	1
Supply Voltage	$V_{CCT,R}$	–0.5	3.6	V	1
Voltage at any Input Pin	V_{IH}	–0.5	V_{CC}	V	1
Sense Output Current – LOS, TX Fault	ID		150	mA	1
Sense Output Current – MOD_DEF2	ID		5	mA	1

Notes:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded. See Reliability Data Sheet for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions functional performance is not intended, device reliability is not implied, and damage to the device may occur.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature	T_C	0	25	70	°C	1, 2
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	1
Data Rate			1.25		Gb/s	1, 3
Data Rate			1.0625		Gb/s	1, 4

Notes:
1. Recommended Operating Conditions are those within which functional performance within data sheet characteristics is intended.
2. Refer to the Reliability Data Sheet for specific reliability performance predictions.
3. IEEE802.3 Gigabit Ethernet.
4. ANSIX3.230 (FC-PI).

Table 5. Transceiver Electrical Characteristics (T_C = 0°C to 70°C, $V_{CCT,R}$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Module Supply Current	I_{CC}		160	220	mA	
Power Dissipation	P_{DISS}		530	765	mW	
Power Supply Noise Rejection (peak-peak)	PSNR		100		mV_{PP}	1
Data Input: Transmitter Differential Input Voltage (TD +/–)	V_I	500		1660	mV_{PP}	2
Data Output: Receiver Differential Output Voltage (RD +/–)	V_O	370	1500	2000	mV_{PP}	3
Receive Data Rise & Fall Times	T_{rf}		220		ps	
Sense Outputs: Transmit Fault [TX_FAULT, Loss of Signal (LOS), MOD_DEF2]	V_{OH}	2.0		V_{CC}	V	
	V_{OL}	0		0.8	V	
Control Inputs: Transmitter Disable [TX_DISABLE, MOD_DEF1,2]	V_{IH}	2.0		V_{CC}	V	
	V_{IL}	0		0.8	V	

Notes:
1. Measured at the input of the required MSA Filter on host board.
2. Internally AC coupled and terminated to 100 Ohm differential load.
3. Internally AC coupled, but requires a 100 Ohm differential termination at or internal to Serializer/Deserializer.

Table 6. Transmitter Optical Characteristics (T_C = 0°C to 70°C, $V_{CCT,R}$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Optical Power (Average)	Pout	–9.5	–6.5	0	dBm	1, 2, 3
Optical Extinction Ratio	ER	9	14.5		dB	1
Center Wavelength	λ_C	830	850	860	nm	1
Spectral Width – rms	σ			0.85	nm	1
Optical Rise/Fall Time (1.25 GBd)	$T_{rise/fall}$		150	260	ps	1
Optical Rise/Fall Time (1.0625 GBd)	$T_{rise/fall}$		150	300	ps	1,4
Relative Intensity Noise, maximum	RIN			–117	dB/Hz	1
Total Jitter (TP1 to TP2 Contribution 1.25 GBd)	TJ			227	ps	1
				0.284	UI	1
(TP1 to TP2 Contribution 1.0625 GBd)					252	ps 4
				0.267	UI	4
Deterministic Jitter (TP1 to TP2 Contribution 1.0625 GBd)	DJ				85	ps 4
				0.09	UI	4
Pout TX_DISABLE Asserted	P_{OFF}			–35	dBm	1
Optical Modulation Amplitude	OMA		156		µW	4

Notes:
1. IEEE 802.3.
2. Max. Pout is the lesser of 0 dBm or Maximum allowable per Eye Safety Standard.
3. 50/125 µm fiber with NA = 0.2, 62.5/125 µm fiber with NA = 0.275.
4. ANSIX3.230 (FC-PI).

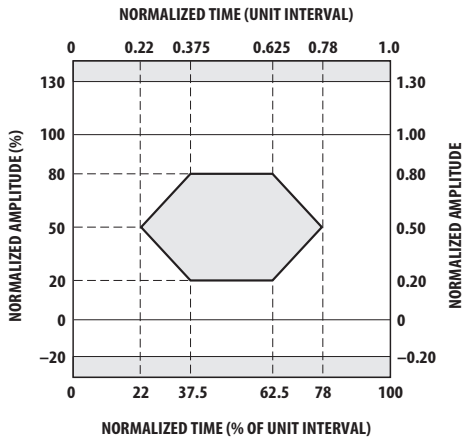


Figure 5a. Gigabit Ethernet transmitter eye mask diagram.

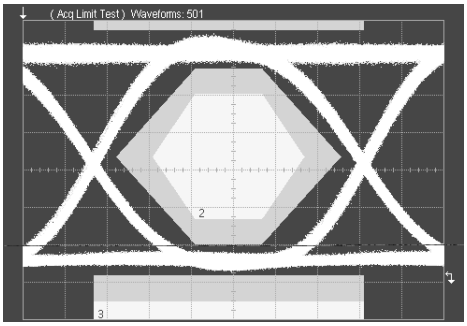


Figure 5b. Typical HFBR-5701L eye mask diagram.

Table 7. Receiver Optical Characteristics (T_C = 0°C to 70°C, $V_{CCT,R}$ = 3.3 V ± 5%)

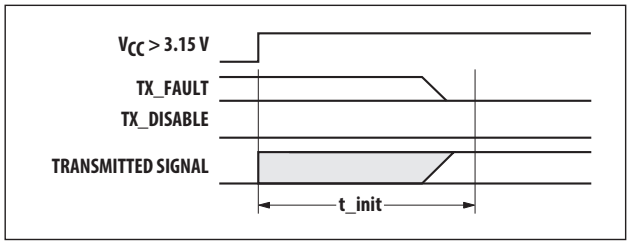
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Optical Input Power	PR	–17		0	dBm	1
Receiver Sensitivity (Optical Input Power)	PRMIN		–21	–17	dBm	1
Stressed Receiver Sensitivity				–12.5	dBm	1, 2
1.25 GBd (GBE)				–13.5	dBm	1, 3
Stressed Receiver Sensitivity				–11.74	dBm	2, 4
1.0625 GBd (FC-PI)				–12.59	dBm	3, 4
Total Jitter	TJ			266	ps	1
(TP3 to TP4 Contribution 1.25 GBd)				0.332	UI	1
Total Jitter	TJ			205	ps	4
(TP3 to TP4 Contribution 1.0625 GBd)				0.218	UI	4
Deterministic Jitter	DJ			113	ps	4
(TP3 to TP4 Contribution 1.0625 GBd)				0.12	UI	4
Return Loss				–12	dB	1
LOS De-Asserted	P_D			–17	dBm	1
LOS Asserted	P_A	–31			dBm	1
LOS Hysterisis	P_D - P_A		3		dB	1
Optical Modulation Amplitude	OMA	31			µW	4

Notes:
1. IEEE 802.3.
2. 62.5/125 µm fiber.
3. 50/125 µm fiber.
4. ANSIX3.230 (FC-PI).

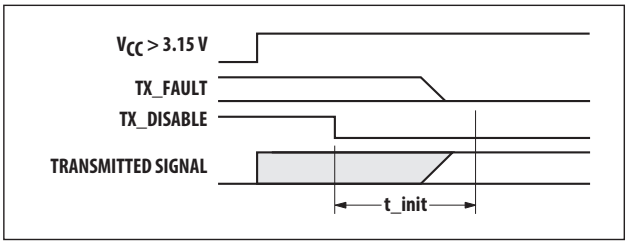
Table 8. Transceiver Timing Characteristics (T_C = 0°C to 70°C, $V_{CCT,R}$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Tx Disable Assert Time	t_off			10	µs	1
Tx Disable Negate Time	t_on			1	ms	2
Time to initialize, including reset of Tx_Fault	t_init			300	ms	3
Tx Fault Assert Time	t_fault			100	µs	4
Tx Disable to Reset	t_reset	10			µs	5
LOS Assert Time	t_loss_on			100	µs	6
LOS Deassert Time	t_loss_off			100	µs	7
Serial ID Clock Rate	f_serial_clock			100	kHz	

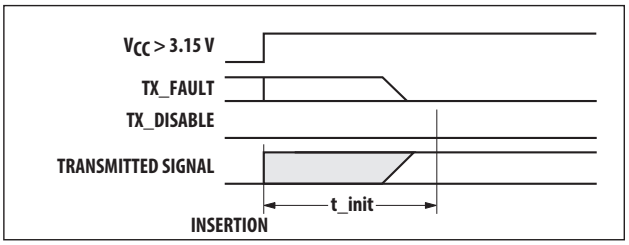
Notes:
1. Time from rising edge of Tx Disable to when the optical output falls below 10% of nominal.
2. Time from falling edge of Tx Disable to when the modulated optical output rises above 90% of nominal.
3. From power on or negation of Tx Fault using Tx Disable.
4. Time from fault to Tx fault on.
5. Time Tx Disable must be held high to reset Tx_fault.
6. Time from LOS state to Rx LOS assert.
7. Time from non-LOS state to RX LOS deassert.



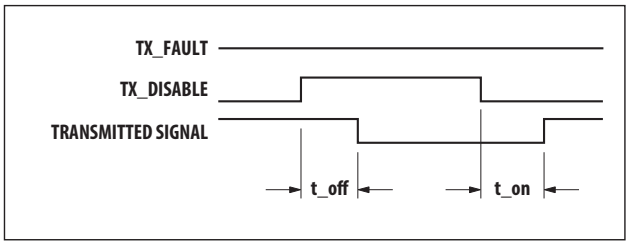
t-init: TX DISABLE NEGATED



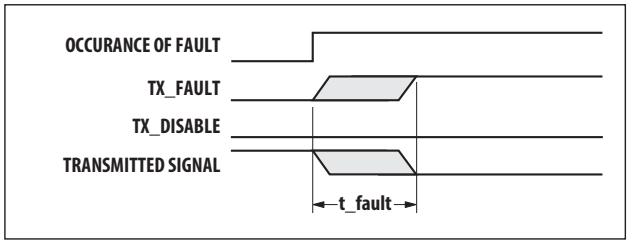
t-init: TX DISABLE ASSERTED



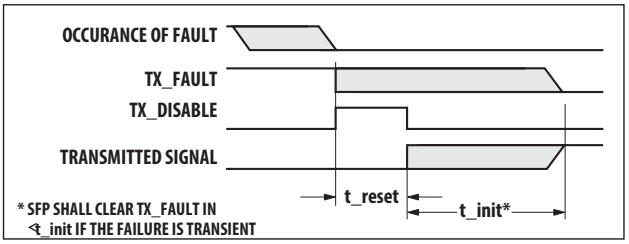
t-init: TX DISABLE NEGATED, MODULE HOT PLUGGED



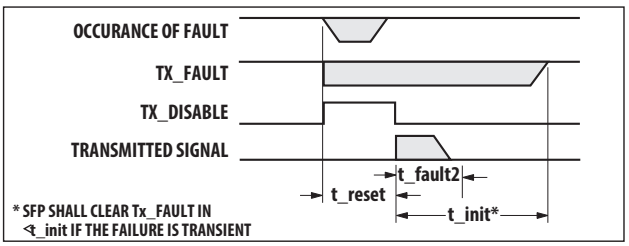
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



t-fault: TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED

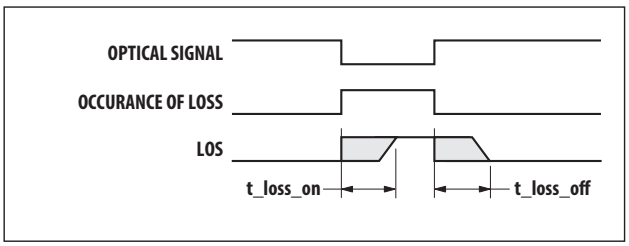


t-reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



t-fault2: TX DISABLE ASSERTED THEN NEGATED,
TX SIGNAL NOT RECOVERED

NOTE: t_fault2 timing is typically 1.7 to 2 ms.



t-loss-on & t-loss-off

Figure 6. Transceiver timing diagrams (Module installed except where noted).

Table 9. EEPROM Serial ID Memory Contents

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
0	03		32	20		64	00		96	Note 4	
1	04		33	20		65	1A		97	Note 4	
2	07		34	20		66	00		98	Note 4	
3	00		35	20		67	00		99	Note 4	
4	00		36	00		68	Note 1		100	Note 4	
5	00		37	00		69	Note 1		101	Note 4	
6	01		38	30		70	Note 1		102	Note 4	
7	20		39	D3		71	Note 1		103	Note 4	
8	40		40	48	H	72	Note 1		104	Note 4	
9	0C		41	46	F	73	Note 1		105	Note 4	
10	00		42	42	B	74	Note 1		106	Note 4	
11	01		43	52	R	75	Note 1		107	Note 4	
12	0C		44	2D	-	76	Note 1		108	Note 4	
13	00		45	35	5	77	Note 1		109	Note 4	
14	00		46	37	7	78	Note 1		110	Note 4	
15	00		47	30	0	79	Note 1		111	Note 4	
16	37		48	31	1	80	Note 1		112	Note 4	
17	1B		49	4C	L	81	Note 1		113	Note 4	
18	00		50	20		82	Note 1		114	Note 4	
19	00		51	20		83	Note 1		115	Note 4	
20	41	A	52	20		84	Note 2		116	Note 4	
21	56	V	53	20		85	Note 2		117	Note 4	
22	41	A	54	20		86	Note 2		118	Note 4	
23	47	G	55	20		87	Note 2		119	Note 4	
24	4F	O	56	20		88	Note 2		120	Note 4	
25	20		57	20		89	Note 2		121	Note 4	
26	20		58	20		90	Note 2		122	Note 4	
27	20		59	20		91	Note 2		123	Note 4	
28	20		60	00		92	00		124	Note 4	
29	20		61	00		93	00		125	Note 4	
30	20		62	00		94	00		126	Note 4	
31	20		63	Note 3		95	Note 3		127	Note 4	

Notes:

1. These addresses are reserved for serial number information and will vary from module to module.
2. These addresses are reserved for date code information and may vary from lot to lot.
3. Byte Addresses 63 and 95 are Check Sums which may vary from module to module.
4. These fields are reserved for future use by Avago Technologies.

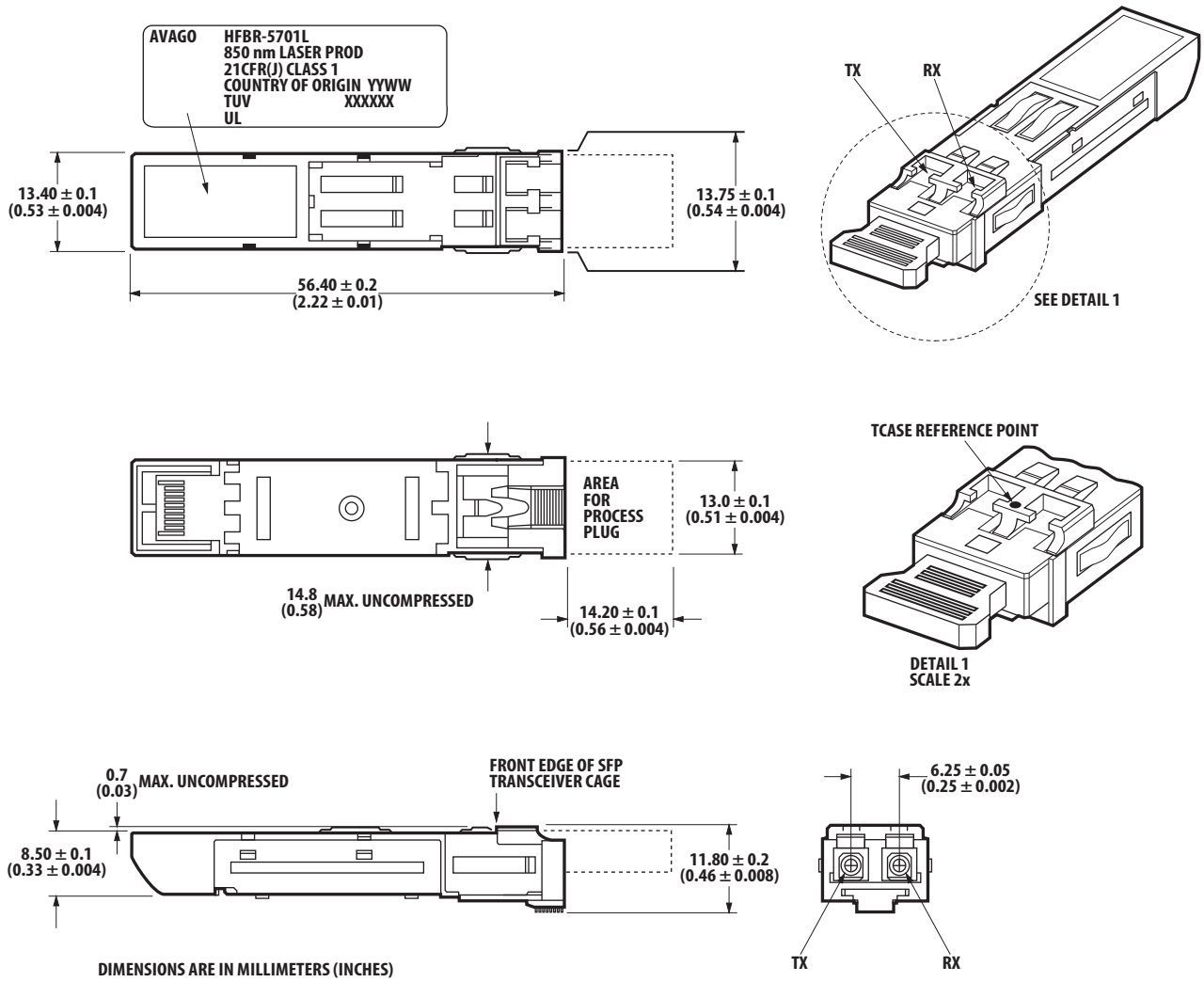
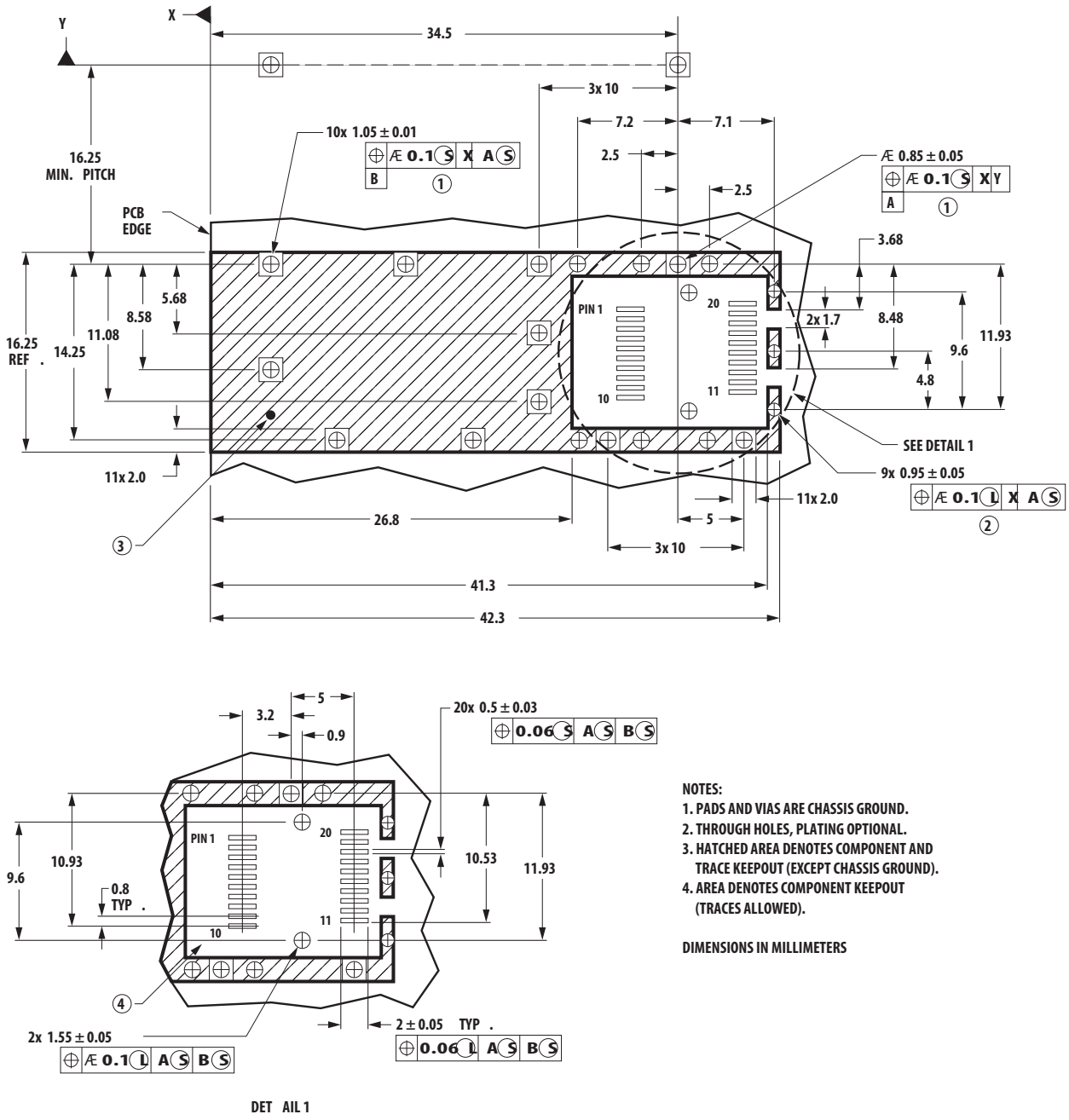


Figure 7. Module drawing.



DET AIL 1

NOTES:
1. PADS AND VIAS ARE CHASSIS GROUND.
2. THROUGH HOLES, PLATING OPTIONAL.
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND).
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED).

DIMENSIONS IN MILLIMETERS

Figure 8. SFP host board mechanical layout.

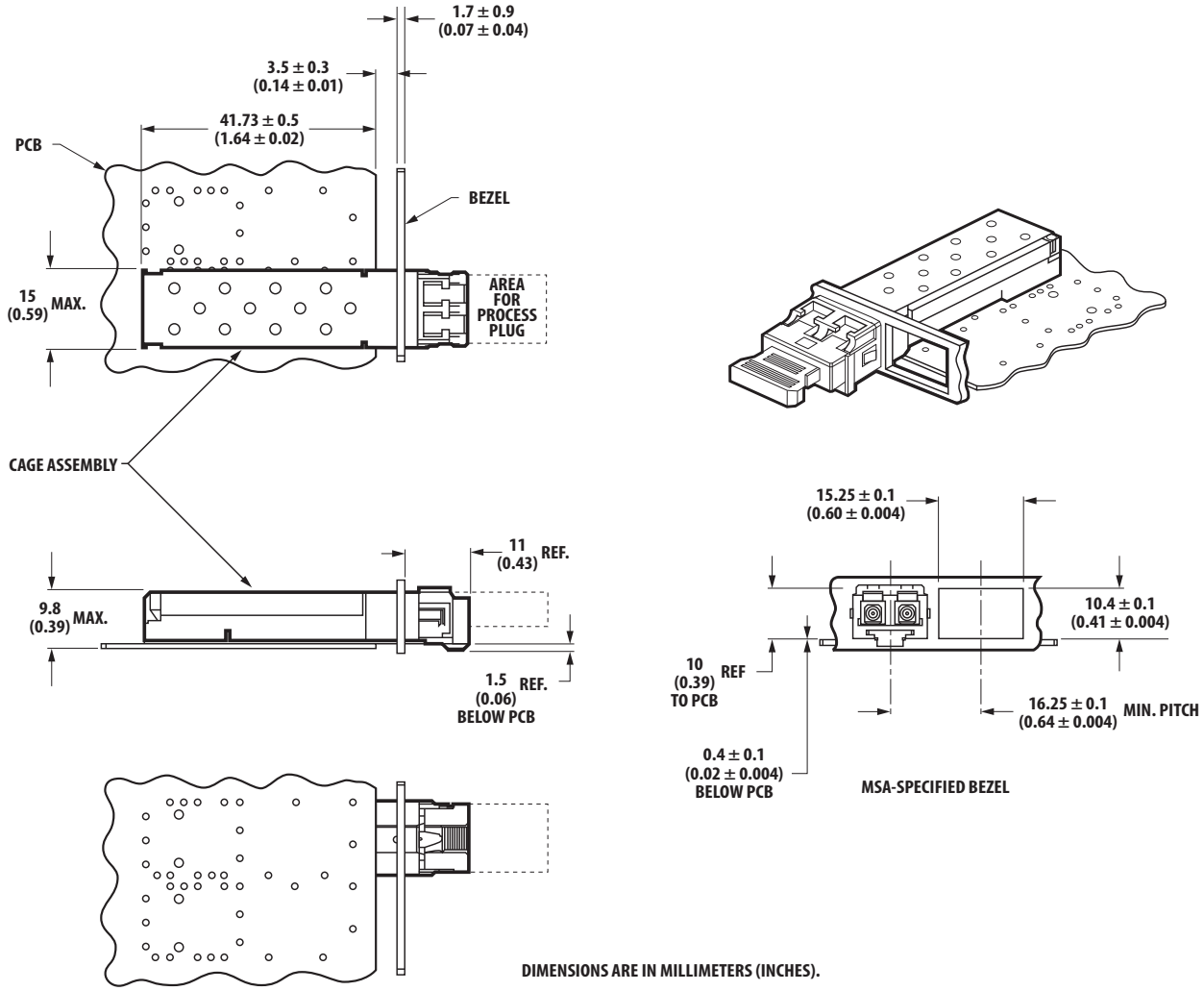


Figure 9. Assembly drawing.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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