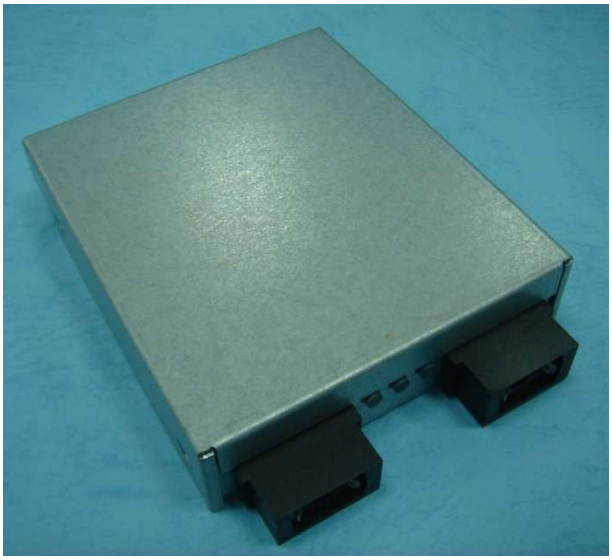
Specification

Dual QSFP28 100GBase-SR4

Optical Bypass Module



O B M – D 3 D H 2 – F 0 1

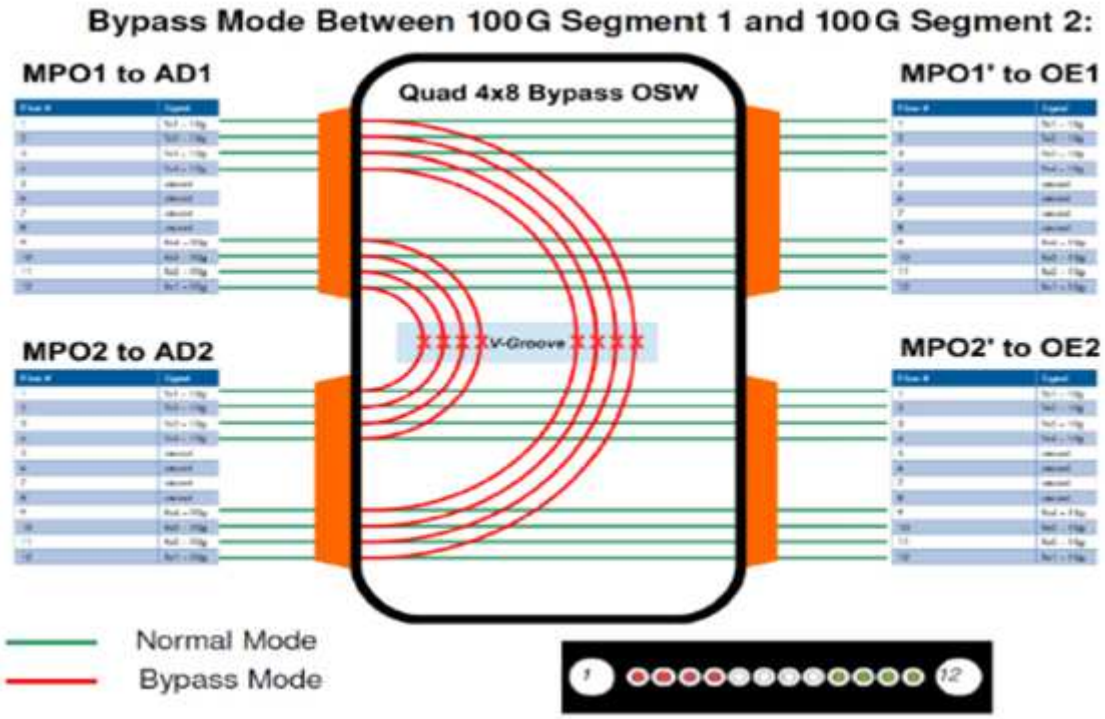
Product Overview

FormericaOE dual 100G (2*100G) QSFP28 Optical Bypass Module (OBM) is a compact box that contains two QSFP28 optical transceivers and optical switches control circuit board. It can be integrated with I/O ports controllers in a Network Interface Card (NIC). The FormericaOE dual QSFP28 OBM is targeted to inline network system that maintains network connectivity when power failure occurs or system fails, particularly for Data Centers that employ extensive QSFP28 for optical inter connects between servers and switches. FormericaOE Dual QSFP28 OBM supports normal and bypass modes, and can be controlled to perform the block mode. In normal mode, the ports are independent interfaces. In bypass mode, all packets received from one port are transmitted to the adjacent port. In block mode, the module blocks the route. FormericaOE Dual QSFP28 OBM can bypass or block its I/O ports on a host system failure, power off, or upon software request. It can be integrated with any brand of CPU controller. It is suitable for connecting with in-line equipment for power failure or system maintenance. When the in-line unit is not on or is in bypass mode, the relays within the OBM are set to bridge the optical signals directly through the optical switch, completely bypassing the in-line equipment. If the in-line equipment is operating normally, then it supplies power to the switch through a high speed connector PIN. Compact and competitive cost, this module provides excellent performance on your network.

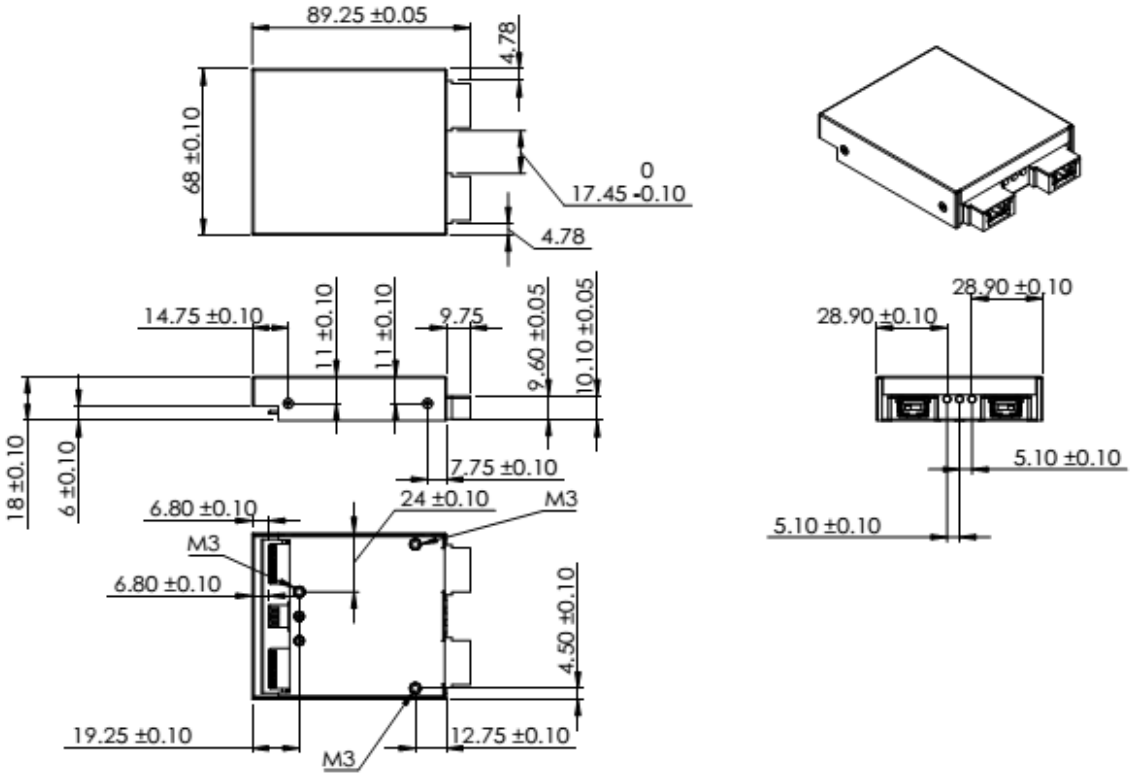
Features

- Reliable Passive Fiber Bypass (Latching)
- Low Return Loss
- Available in 50/125µm Multi Mode Fiber
- PCB Mountable Type
- Fast Ethernet Standard Compliant
- Digital Diagnostic SFF-8472 Rev.10.2 Compliant
- SONET/SDH Standard Compliant
- Two MPO-MT Adapter
- Compliant with CE& FCC Standard
- Compact Format and ROHS Compliant

Block Diagram and Optical Paths



Module Outline Drawing (mm)



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Ts	-40		85	℃
Supply Voltage	Vcc	0		5	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	Top	0		70	℃	1
+5.0V Supply Voltage	Vcc5	4.75		5.25	V	
+3.3V Supply Voltage	Vcc3	3.10		3.50	V	
Relative Humidity (non condensation)		5		85	%	
Data Rate		25.78125 ± 100ppm			Gbps	

Note1 : Please see order information

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
+5.0V Supply Current	Icc5			100	mA	
+3.3V Supply Current	Icc3			1500	mA	
Transmitter (Each QSFP)						
Transmitter Differential Input Voltage	V_{DT}	175		1600	mV	1
Transmitter Disable Input-High	V_{DISH}	2		Vcc+0.3	V	
Transmitter Disable Input-Low	V_{DISL}	-0.3		0.8	V	
Transmitter Fault Pull up Resistor	$R_{TX\ FAULT}$	4.7		10	KΩ	2
Transmitter Fault Output-High	V_{TXFH}	2.4		Vcc	V	2
Transmitter Fault Output-Low	V_{TXFL}	0		0.5	V	2
Receiver (Each QSFP)						
Receiver Differential Output Voltage	V_{DR}	200		900	mV	3
Receiver LOS Load	R_{RXLOS}	4.7		10	KΩ	2
LOS Output Voltage-High	V_{LOSH}	2.4		Vcc	V	2
LOS Output Voltage-Low	V_{LOSL}	0		0.5	V	2

Optical Switch						
Latching Voltage-High	V_{LATH}	4.75	5	5.25	V	
Latching Voltage-Low	V_{LATL}	0		0.8	V	
Latching Resistance	R_{LAT}		125		Ω	

Notes:

1. **Internally AC coupled and terminated to 100Ohm differential load.**
2. **Pull up to Vcc on Host Board.**
3. **Internally AC coupled, but requies a 100Ohm differential termination at or internal to Serializer/Deserializer.**

Optical Characteristics

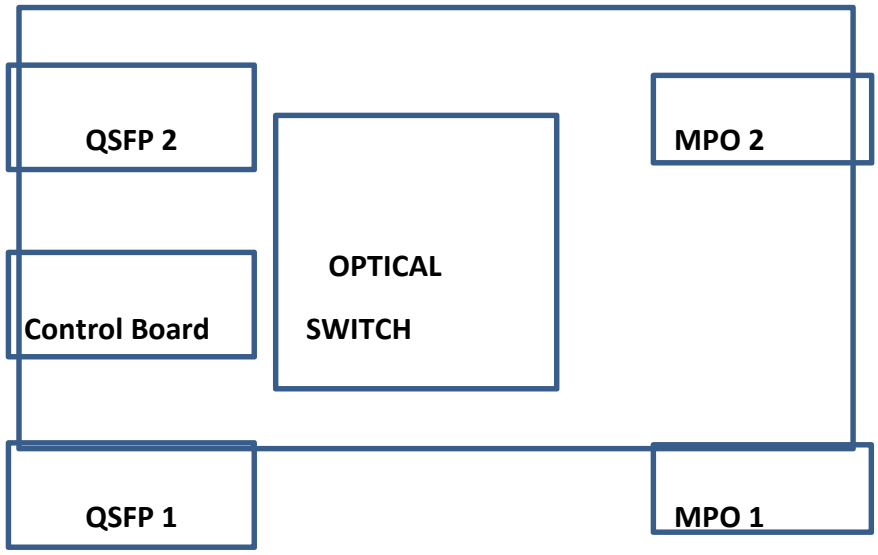
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Output Optical Power (Avg.)	Po	-8.4		2.4	dBm	1
Optical Extinction Ratio	ER	2			dB	
Center Wavelength	λ	840	850	860	nm	
Spectral Width (RMS)	σλ			0.65	nm	
Receiver						
Stress Receiver Sensitivity (OMA) per Lane	SRS			-4.2	dBm	1,2
Input Optical Wavelength	λ	840		860	DBm	
LOS-Deasserted	P_{SA}			-13	dBm	
LOS-Asserted	P_{SD}	-30			dBm	
LOS-Hysteresis	P_{SH}	0.5	2		dB	
Optical Switch						
Wavelength Range	λ	670		980	nm	
Insertion Loss	OIL		0.35	2	dB	
Return Loss	ORL	30			dB	
Switch Time				8	ms	
Lifetime			$\geqq 10^7$		times	
Latching Resistance	R_{LAT}		125		Ω	

Notes:

1. **Normal Mode (Bypass off).**
2. **The sensitivity provided at a BER of 1×10^{-12}or better with an input signal consisting of 25.78125Gb/s, 2^{31}-1 PRBS**

Block Diagram For 2x100G OBM

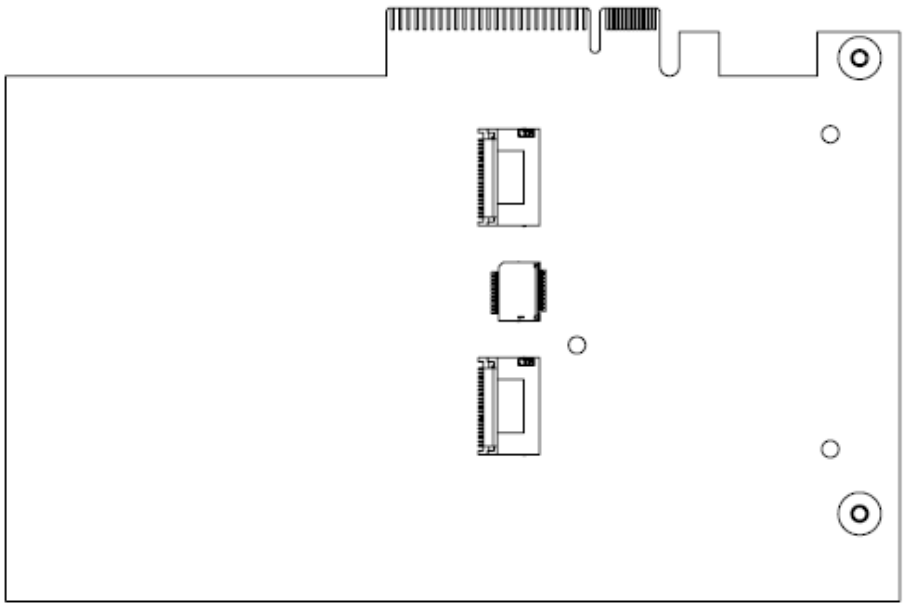
Top View



Host Board Connector

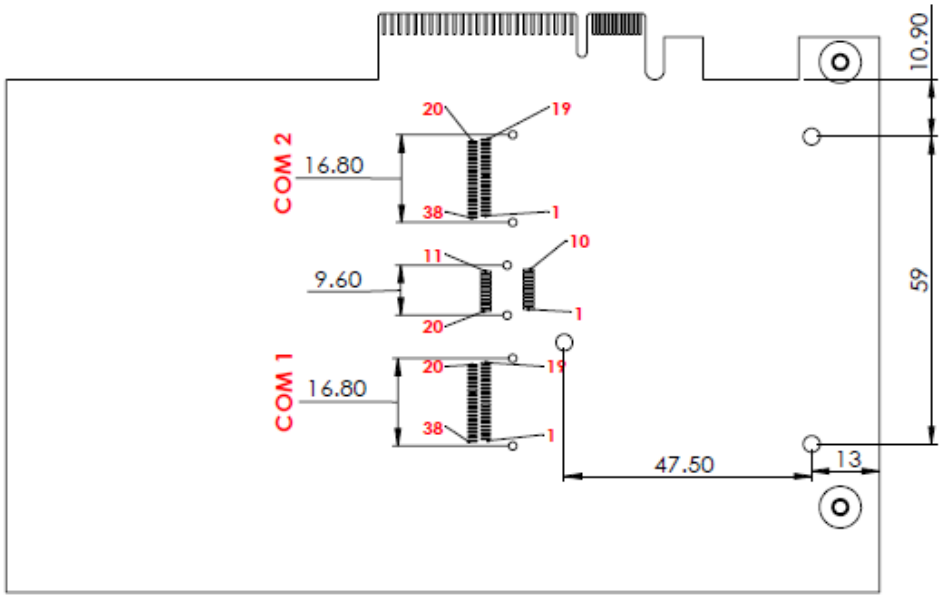
Top View

QSFP Connector x 2
SFP Connector x 1

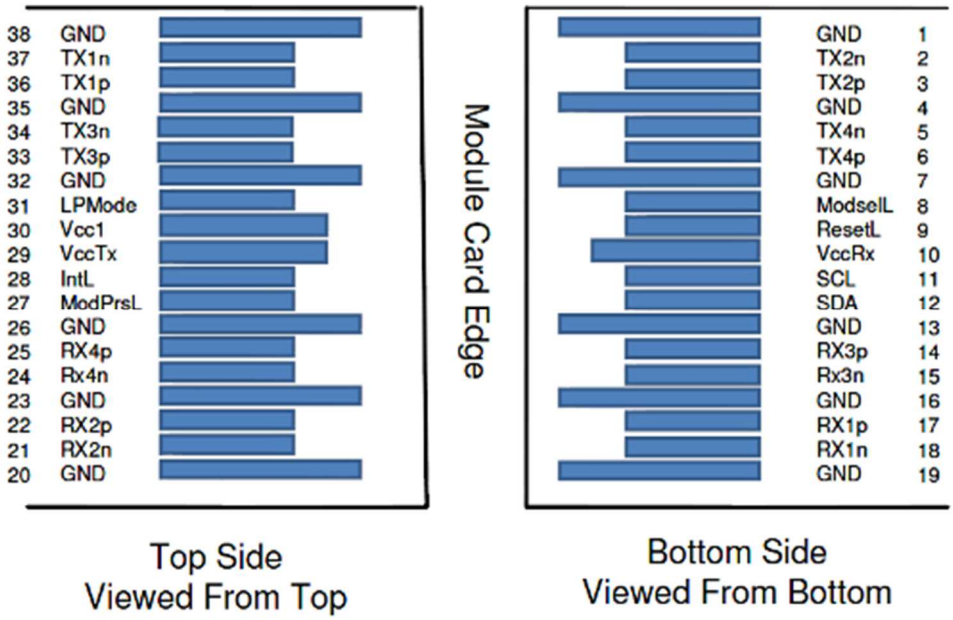


COM 1 & COM 2 Module Pad Assignments

Top View



COM 1 & COM 2 Pin Definition



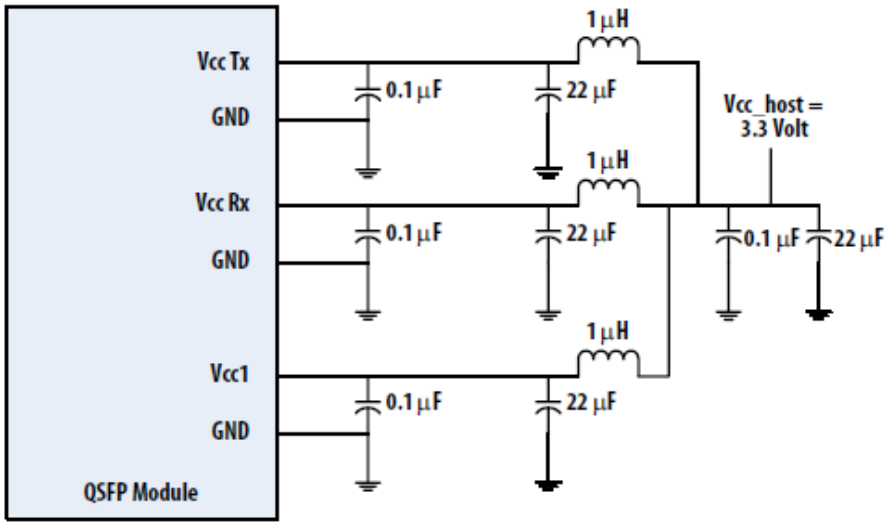
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	2

14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table . Recommended host board power supply filtering is shown in Figure . Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Recommended Host Board Power Supply Circuit



Control Board Pin Definition

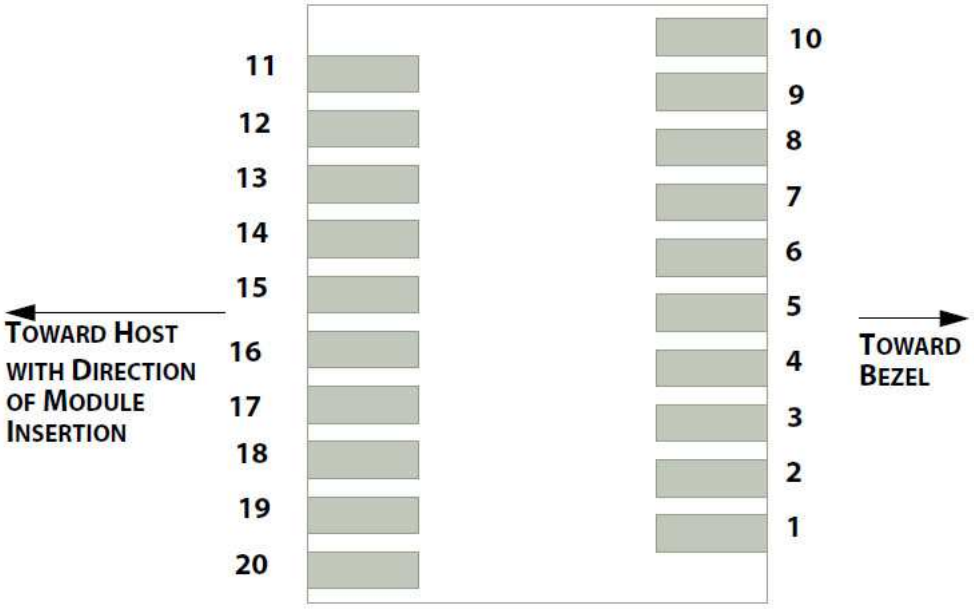


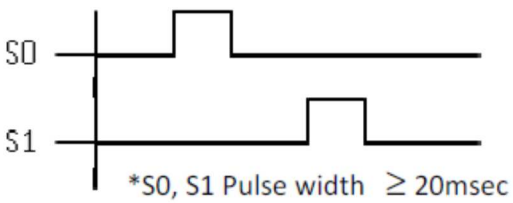
Figure: Module Interface to Host



Figure: Module Contact Assignment

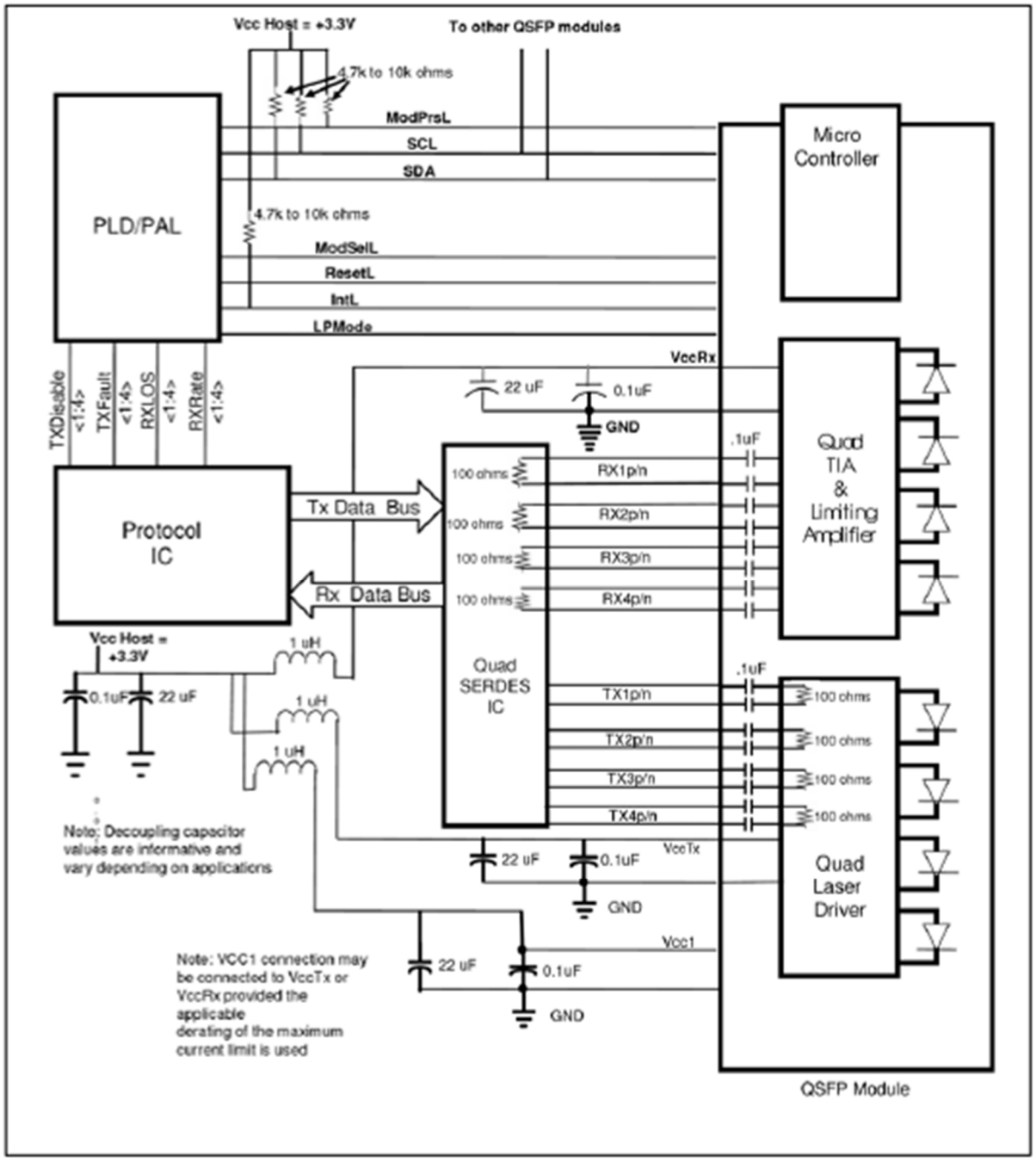
Control Board Pin Descriptions

Pin	Name	Pin Type	Description
1	GND	GND	Ground
2	MON1	Output/LVTTL	Status of Optical Switch 1
3	MON2	Output/LVTTL	Status of Optical Switch 2
4	MON3	Output/LVTTL	Status of Optical Switch 3
5	MON4	Output/LVTTL	Status of Optical Switch 4
6	MOD_ABS	Output/LVTTL	Module absent indicator. It is connected to the module ground. (0: Module present, 1: Module absent)
7	NC	NC	No Connection
8	S0	Input/LVTTL	Change the Optical Switch status
9	S1	Input/LVTTL	Change the Optical Switch status
10	GND	GND	Ground
11	GND	GND	Ground
12	LED1_CTL	Input/LVTTL	Control ON/OFF of LED1. (0:Turn ON, 1: Turn OFF)
13	LED2_CTL	Input/LVTTL	Control ON/OFF of LED2. (0:Turn ON, 1: Turn OFF)
14	LED3_CTL	Input/LVTTL	Control ON/OFF of LED3. (0:Turn ON, 1: Turn OFF)
15	VCC	PWR	3.3V power supply
16	VCC	PWR	3.3V power supply
17	LED4_CTL	Input/LVTTL	Control ON/OFF of LED4. (0:Turn ON, 1: Turn OFF)
18	LED5_CTL	Input/LVTTL	Control ON/OFF of LED5. (0:Turn ON, 1: Turn OFF)
19	NC	NC	No Connection
20	GND	GND	Ground

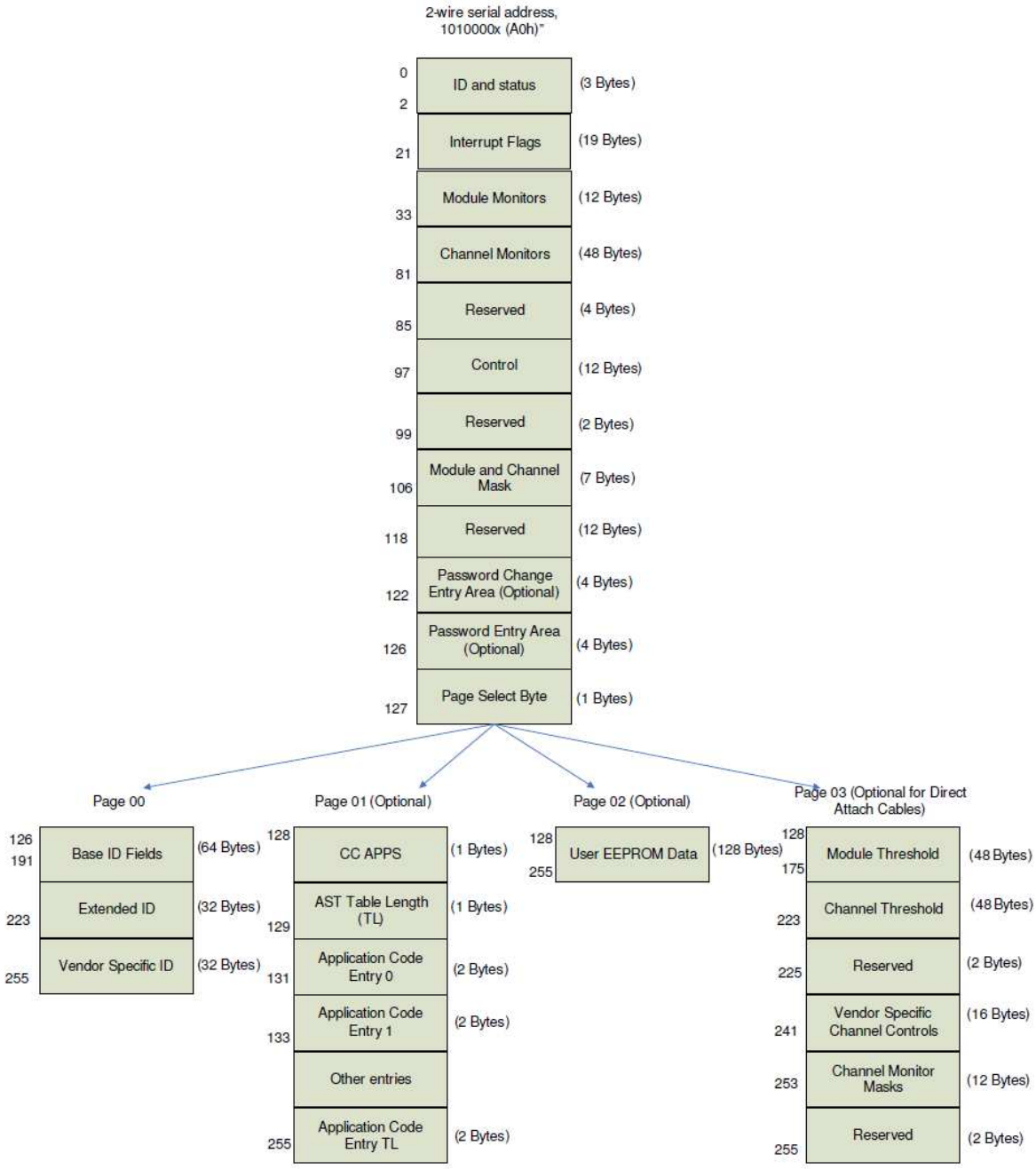


S0 = High, S1 = Low. To change the OSW state to ON state.
S0 = Low, S1 = High. To change the OSW state to OFF state.

Recommended Interface Circuit



Memory Map


2-wire serial address, 1010000x (A0h)"
0
ID and status
(3 Bytes)
2
21
Interrupt Flags
(19 Bytes)
Module Monitors
(12 Bytes)
33
Channel Monitors
(48 Bytes)
81
Reserved
(4 Bytes)
85
Control
(12 Bytes)
97
Reserved
(2 Bytes)
99
Module and Channel Mask
(7 Bytes)
106
Reserved
(12 Bytes)
118
Password Change Entry Area (Optional)
(4 Bytes)
122
Password Entry Area (Optional)
(4 Bytes)
126
Page Select Byte
(1 Bytes)
127
Page 00
Page 01 (Optional)
Page 02 (Optional)
Page 03 (Optional for Direct Attach Cables)
126
191
Base ID Fields
(64 Bytes)
Extended ID
(32 Bytes)
223
Vendor Specific ID
(32 Bytes)
255
128
CC APPS
(1 Bytes)
AST Table Length (TL)
(1 Bytes)
129
Application Code Entry 0
(2 Bytes)
131
Application Code Entry 1
(2 Bytes)
133
Other entries
Application Code Entry TL
(2 Bytes)
255
128
255
User EEPROM Data
(128 Bytes)
128
175
Module Threshold
(48 Bytes)
Channel Threshold
(48 Bytes)
223
Reserved
(2 Bytes)
225
Vendor Specific Channel Controls
(16 Bytes)
241
Channel Monitor Masks
(12 Bytes)
253
Reserved
(2 Bytes)
255

ESD

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Contact Information

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