AFBR-59F2Z

250MBd Compact 650nm Transceiver for Data communication over Polymer Optical Fiber (POF) cables with a bare fiber locking system

Data Sheet



Description

The Avago Technologies AFBR-59F2Z transceiver provides system designers with the ability to support serial communication with baud rates of up to 250MBd over 2.2mm jacketed standard polymer optical fiber (POF).

The innovative bare fiber locking mechanism of the transceiver allows connection of POF cable with a simple insert and lock system eliminating the need for connectors. This facilitates fast installation and maintenance.

The AFBR-59F2Z is Laser Class 1, lead-free and compliant with RoHS. The very compact design is similar to that of the well known RJ-45 connector.

Transmitter

The transmitter consists of a 650nm LED which is controlled by a fully integrated driver IC. The LED driver operates at 3.3V. It receives Low Voltage Differential Signaling (LVDS) electrical input, and converts it into a modulated current driving the LED. LED and driver IC are packaged in an optical subassembly.

The optimized lens system of the optical subassembly couples the emitted optical power very efficiently into 1mm core POF cable.

Receiver

The receiver utilizes a fully integrated single chip solution which provides excellent immunity to EMI and fast transient dV/dt rejection. The receiver directly converts light to a digital LVDS output signal and operates at 3.3V nominal supply. The integrated receiver is packaged in an optical subassembly, which couples optical power efficiently from POF to the receiving PIN.

The receiver features an analog monitor output of the incoming optical signal. The monitor output provides an analog voltage proportional to the average optical input power. In absence of receiver optical input signal, the receiver is in low power sleep mode and the differential output signal is pulled to ground. The receiver wakes up, when a valid optical input signal is detected.

Features

- Easy bare fiber termination solution for 2.2mm jacket POF
- EMI/ EMC robust
- Link lengths up to 40m POF
- LVDS interface compatible
- Operating temp. range -40°C to 85°C
- 3.3V power supply operation
- Analog monitor output (MON)
- Low power sleep mode

Applications

- Factory automation
- Power generation and distribution system
- Industrial vision system
- Solar panel tracking system
- Home/ Office Networking

Package

The transceiver package contains the two optical subassemblies which are mounted in the housing for bare fiber connection.

The metal shield on bare fiber clamp transceiver provides excellent immunity to EMI/ EMC

Pin description and recommended PCB footprint

The AFBR-597F2Z has ten active signal pins (including supply voltage and ground pins), two EMI shield solder posts, two additional ground pins and two mounting posts.

The EMI shield solder posts and the additional ground pins are isolated from transceiver internal circuit and should be connected to equipment chassis ground or signal ground. Connecting the two additional ground pins with ground provides EMI shielding to the front of the device. Grounding these pins will also provide a ground connection of the POF jacket in order to ground small leakage currents in high voltage applications such as in HVDC installations.

The mounting posts provide additional mechanical strength to hold the transceiver module on the application board.

Figure 1 shows the top view of the PCB footprint and Pin-out diagram.

Pin Descriptions

Pin No.	Name	Symbol	Pin No.	Name	Symbol
1	Data Input (Negative)	TD-	8	Monitor Output (IAVG)	MON
2	Data Input (Positive)	TD+	9	Data Output (Negative)	RD-
3	Ground Tx	GND	10	Data Output (Positive)	RD+
4	DC Supply Voltage Tx	Vdd	11	EMI Shield GND	-
5	(Optional) Ground Tx	GND	12	EMI Shield GND	-
6	DC Supply Voltage Rx	Vdd	13	Additional EMI GND	-
7	Ground Rx	GND	14	Additional EMI GND	-

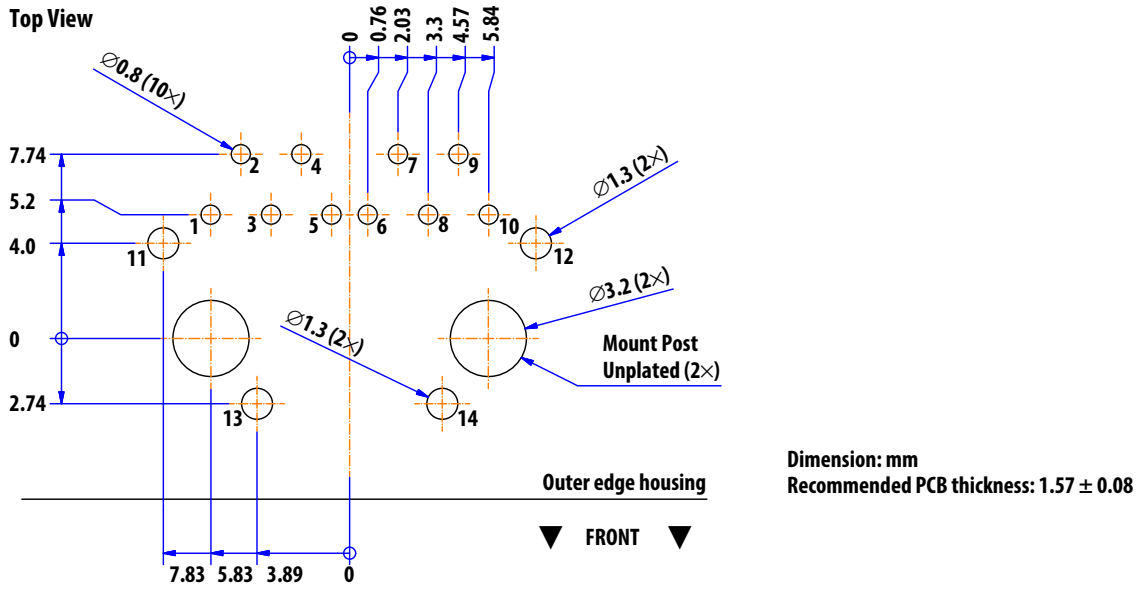


Figure 1. PCB footprint and Pin-out diagram

Recommended compliance table

Feature	Test Method	Performance
Electrostatic discharge (ESD) to the electrical Pins	JESD22-A114	Withstands up to 2kV HBM applied between the electrical pins.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 15V/m field swept from 8MHz to 1GHz applied to the transceiver when mounted on a circuit board without chassis enclosure.
Eye safety	EN 60825-1:52007	Laser Class 1 product (LED radiation only). TÜV certificate:R50217706. CAUTION – Use of controls or adjustments of performance or procedures other than those specified herein may result in hazardous radiation exposure.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	$V_{dd\ Max}$	-0.5	4.5	V
Storage Temperature	T_{STG}	-40	85	°C
Lead Soldering Temperature [1]	T_{sold}		260	°C
Lead Soldering Time [1]	t_{sold}		10	s
Electrostatic Voltage Capability [2]	ESD		2.0	kV
Installation Temperature [3]	T_I	0	50	°C

Notes:
1. The transceiver is Pb-free wave solderable. According to JEDEC J-STD-020D, the moisture sensitivity classification is MSL2a.
2. ESD Capability for all Pins HBM (human body model) according JESD22-A114B
3. Range over which fibers can be connected/ disconnected to/ from the bare fiber clamp.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	-40	25	85	°C
DC Supply Voltage	V_{dd}	3.0	3.3	3.6	V
Baud Rate [4]	BR	10		250	MBd

Note:
4. Data rate of 200 Mbps with 8b/10b coding.

All the data in this specification refer to the operating conditions above and over lifetime unless otherwise stated.

Mechanical Characteristics

Parameter	Min.	Typ.	Max.	Units	Temp. [°C]
Fiber/ Cable Retention Force [5]	-	30	-	N	25
	10	-	50	N	-40....85 [6]
Clamp opening force	-	20	-	N	25
	10	-	30	N	0....50 [6]
Clamp closing force	-	13	-	N	25
	5	-	20	N	0....50 [6]

Notes:
5. Measured with Avago's AFBR-HUDxxxZ (2.2mm duplex-fiber, PE-jacket, without connector) with 100mm/ min traction speed.
6. Range over which fibers can be connected/ disconnected to/ from the bare fiber clamp.

Transmitter Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Current Consumption	I_{dd}	-	29.0	40.0	mA
External Input Termination Impedance	Z_{IN}	-	100		Ω
LVDS Input Voltage Range to Circuit Common	V_{IN}	0.8	-	2.2	V
LVDS Differential Input Voltage	$V_{IN-DIIFF}$	200	-	1200	mV

Transmitter Optical Characteristics (with standard POF NA = 0.5)

Parameter	Symbol	Min.	Typ.	Max.	Units
Central Wavelength [1]	λ_C	635	650	675	nm
Spectral Bandwidth (RMS)	λ_W	-	-	17.0	nm
Average Output Power [1, 3]	P_O	-8.5	-	-2.0	dBm
Optical Rise Time (20% - 80%) [1]	t_r	-	1.2	3.0	ns
Optical Fall Time (80% - 20%) [1]	t_f	-	1.2	3.0	ns
Extinction Ratio [1]	R_E	10.0	12.0	-	dB
Duty Cycle Distortion [1]	DCD	-	-	1.0	ns
Random Jitter [1, 2]	RJ	-	-	0.7	ns
Data dependent Jitter [1]	DDJ	-	-	0.8	ns

Notes:
1. Measured at the end of 1m plastic optical fiber (POF) with PRBS 2^7-1 sequence
2. Peak to peak measurement, based on BER = 2.5×10^{-10}
3. Minimum average output power specification value includes 1dB degradation margin

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Current Consumption	I_{dd}	-	23.0	30.0	mA
LVDS Output Common Mode Voltage	V_{CM}	-	1.2	-	V
LVDS Output Differential Voltage Swing [4]	V_{O-DIFF}	250	-	400	mV
Output Rise Time (10% - 90%) [4]	t_f	-	1.1	3.0	ns
Output Fall Time (90% - 10%) [4]	t_f	-	1.1	3.0	ns
Duty Cycle Distortion [4]	DCD	-	-	1.0	ns
Random Jitter [4, 5, 6]	R_J	-	-	1.0	ns
Data Dependent Jitter [4]	DDJ	-	-	0.8	ns
Output Ratio for MON Pin (to use I_{AVG} output of the IC)	$I_{MON/P}$	-	0.5	-	µA/µW
Monitor Output Voltage Range	V_{MON}	0	-	V_{CC}-1.5	V
Wake up time after sleep state	T_{WKUP}			1.0	ms

Notes:
4. Differential output signal is measured with reference transmitter source, 0.5m POF cable, and PRBS 2^7-1 sequence.
5. Peak to peak measurement, based on BER = 2.5×10^{-10}
6. Maximum random jitter at -15dBm optical input power is 0.4ns.

Receiver Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Central Wavelength [7]	λ_C	635	650	675	nm
Minimum Receiver Input Power [7]	$P_{in\ Min}$	-21.0	-	-	dBm
Maximum Receiver Input Power [7]	$P_{in\ Max}$	-	-	-2.0	dBm

Note:
7. Average optical power, measured with a PRBS 2^7-1 sequence, BER = 2.5×10^{-10}

Analog Monitoring Voltage

Figure 2 shows the variation of analog monitoring voltage as a function of receiver optical input for industrial temperature range. The monitoring voltage is measured across 2K resistor as shown in Figure 3. The monitoring voltage varies linearly with optical input power and the variation over temperature is negligible.

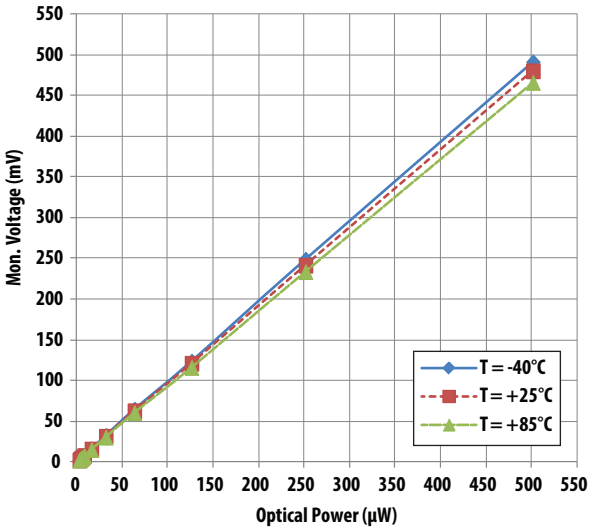


Figure 2. Analog monitoring voltage as a function of optical power

General LVDS Application Circuit

The recommended application circuit is shown in figure 3.

Board layout- Decoupling circuit and Ground Planes

To achieve optimum performance from the AFBR-59F2Z transceiver module it is important to take note of the following recommendations; A power supply decoupling circuit should be used to filter out noise and assure optical product performance; A contiguous signal ground plane should be provided directly beneath the transceiver module for low inductance ground to signal return current; The shield posts should be connected to chassis ground or signal ground to provide optimum EMI and ESD performance. These recommendations are in keeping with good high frequency board layout practices, however, the optimum grounding strategy will depend on the overall system architecture.

Figure 3 shows the minimum external circuitry between AFBR-59F2Z transceiver module and PHY chip. AC-coupling would be possible, if the common mode voltage and voltage swing at the data lines are within the recommended values. Please use the product information of the actual PHY Chip for connecting to the AFBR-59F2Z transceiver module.

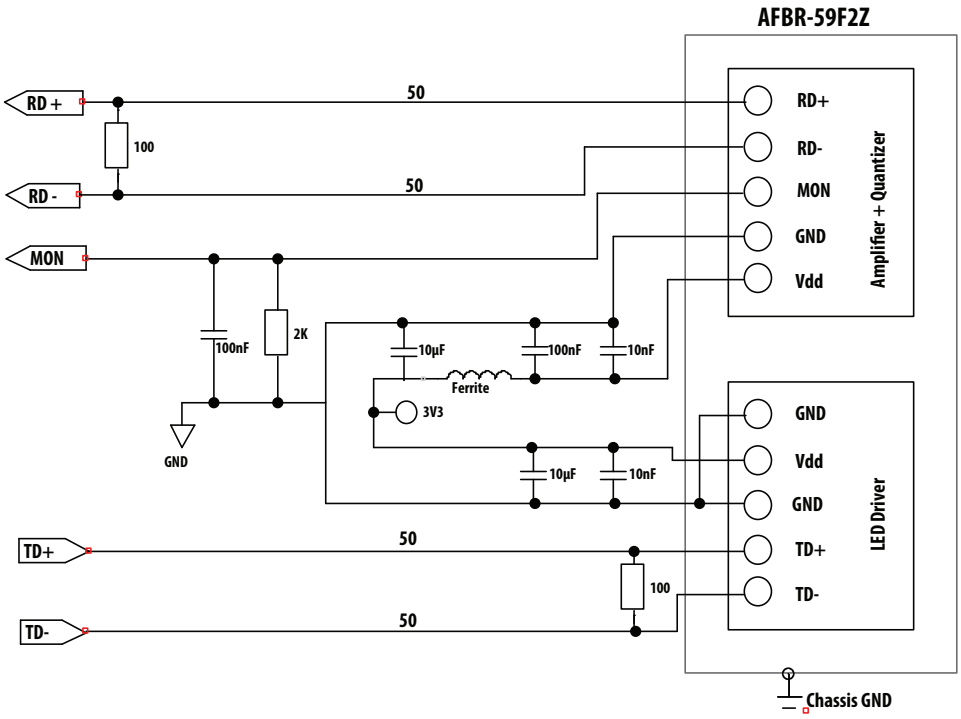
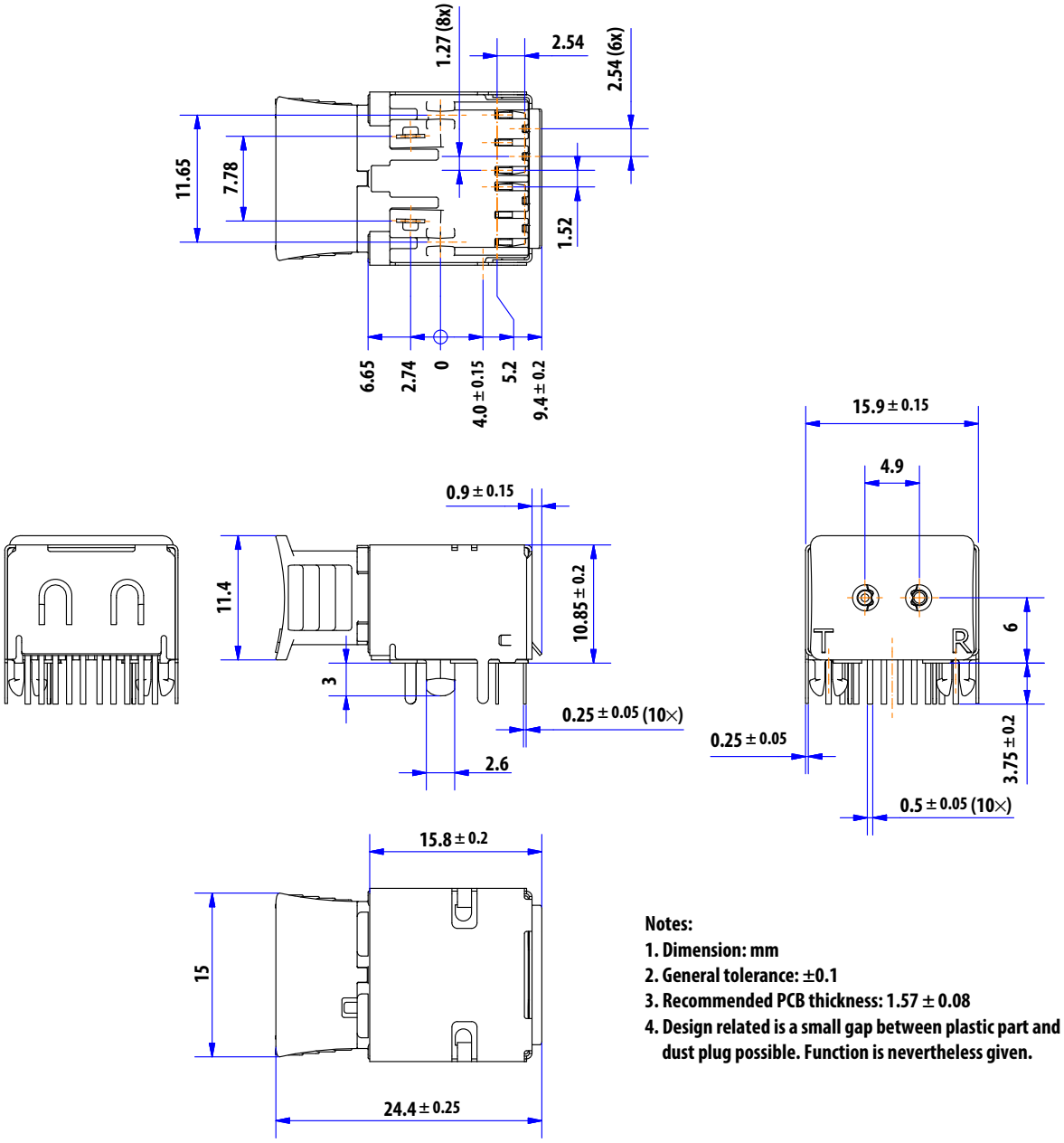


Figure 3. General Application Circuit for LVDS configuration

Mechanical Data - Package Outline



Notes:

1. Dimension: mm
2. General tolerance: ±0.1
3. Recommended PCB thickness: 1.57 ± 0.08
4. Design related is a small gap between plastic part and dust plug possible. Function is nevertheless given.

Clamp open

Clamp with Dust Plug

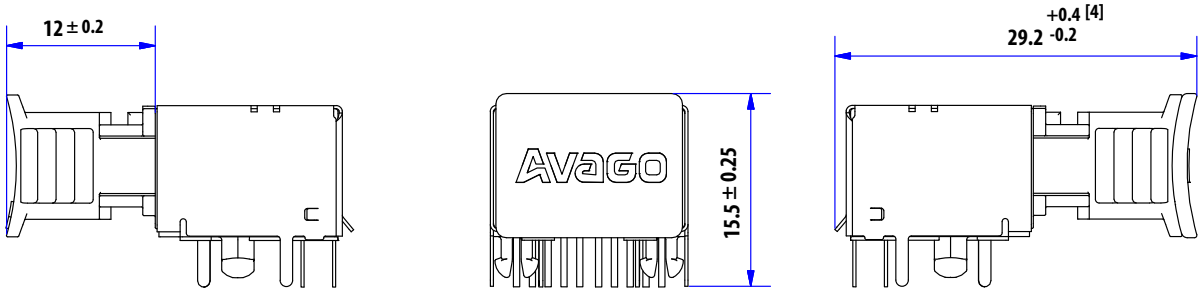


Figure 4. Package Outline Drawing

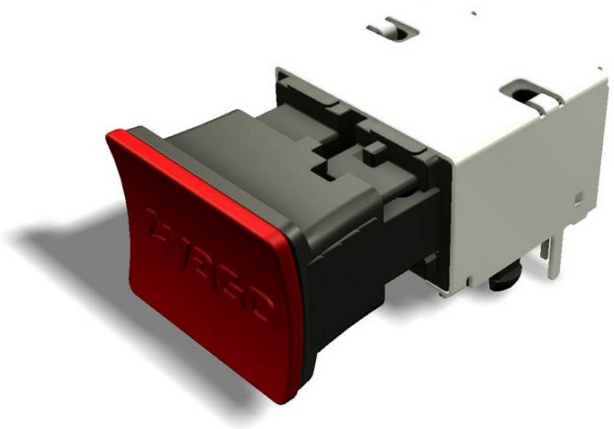


Figure 5. AFBR-59F2Z transceiver module with dust plug

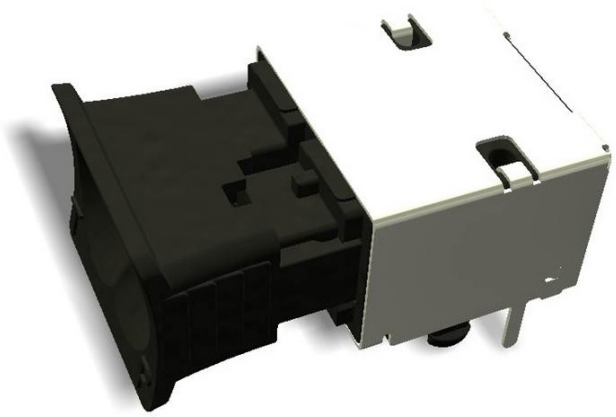


Figure 6. AFBR-59F2Z transceiver module without dust plug

DISCLAIMER: *Avago's products and software are not specifically designed, manufactured or authorized for sale as parts, components or assemblies for the planning, construction, maintenance or direct operation of a nuclear facility or for use in medical devices or applications. Customer is solely responsible, and waives all rights to make claims against Avago or its suppliers, for all loss, damage, expense or liability in connection with such use.*

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.
Data subject to change. Copyright © 2005-2015 Avago Technologies. All rights reserved.
AV02-4756EN - April 13, 2015