AFBR-79Q4Z, AFBR-79Q4Z-D

InfiniBand 4x QDR

QSFP Pluggable, Parallel Fiber-Optics Module

Data Sheet



Description

The Avago Technologies AFBR-79Q4Z is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP Transceiver for QDR InfiniBand and proprietary applications. This transceiver is a high performance module for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 40 Gbps aggregate bandwidth. Each lane can operate at 10 Gbps up to 100 m using OM3 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38-contact edge type connector. The optical interface uses an 8 or 12 fiber MTP® (MPO) connector. This module incorporates Avago Technologies proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Applications

- InfiniBand QDR (4 x 10G), DDR (4 x 5G) and SDR (4 x 2.5G) interconnects
- High Performance and High Productivity computer interconnects
- Data Aggregation, Backplane and Proprietary Density Applications
- PCI-Express, SAS/SATA, Fibre Channel compatible interconnect
- Datacom and Telecom switch and router backplane connections

Features

- Compliant to the InfiniBand Architecture Release 1.2.1 QDR Specification
- Compliant to the industry standard INF-8436i QSFP Transceiver Specification Revision 1.0
- High Channel Capacity: up to 40 Gbps per module, bi-directional operation
- Operates up to 10 Gbps with 8b/10b compatible coded data
- Backwards compatible to 5Gbps DDR IB and 2.5 Gbps SDR IB
- 0 to 70°C case temperature operating range
- Proven High Reliability 850 nm technology: Avago Technologies VCSEL array transmitter and Avago Technologies PIN array receiver
- High port density: 21mm horizontal port pitch
- Up to 100m links at 10G/channel using OM3 multimode fiber
- Four independent transmitter channels and 4 independent receiver channels per module
- Two Wire Serial (TWS) interface with maskable interrupt for expanded functionality including:
  - Individual channel functions: disable, squelch disable
  - A/D readback: module temperature and supply voltages, per channel laser current and laser power, or received power
  - Status: per channel Tx fault, electrical (transmitter) or optical (receiver) LOS, and alarm flags

Patent - www.avagotech.com/patents

Part Number Ordering Options

QDR 10G InfiniBand	AFBR-79Q4Z
QDR 10G InfiniBand With Full Digital Diagnostic Monitoring	AFBR-79Q4Z-D

Evaluation Board	AFBR-79Q4EKZ*
Evaluation Kit	AFBR-79Q2EKZ**

* Includes GUI and User Guide
** Includes GUI, User Guide, i-Port and Power Supply

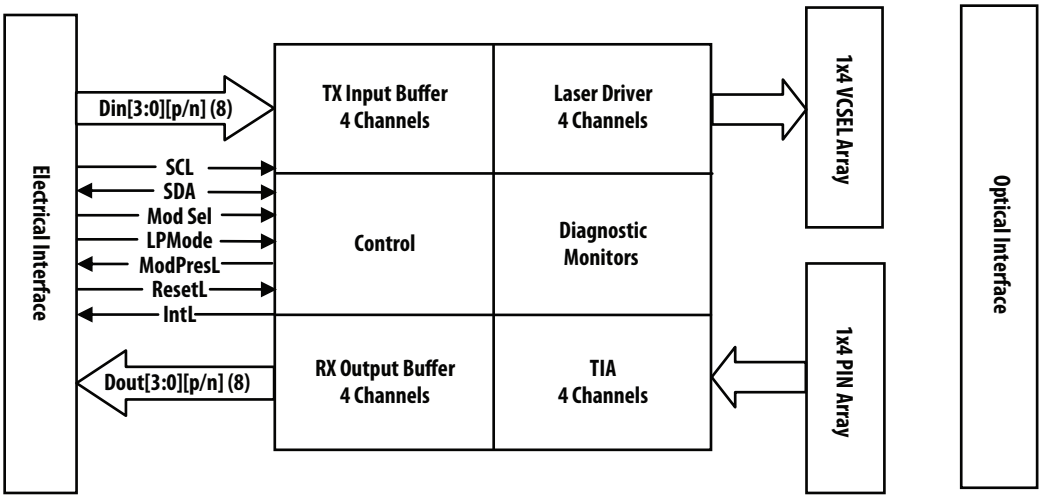


Figure 1. Transceiver Block Diagram

Transmitter

The optical transmitter portion of the transceiver (see Figure 1) incorporates a 4-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 4-channel input buffer and laser driver, diagnostic monitors, and control and bias blocks. The transmitter is designed for IEC-60825 and CDRH eye safety compliance; Class 1M out of the module. The Tx Input Buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 Ohms. AC coupling capacitors are located inside the QSFP module and are not required on the host board. For module control and interrogation, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals.

Modules with Full Digital Diagnostic Monitoring have monitors for VCSEL bias, light output (LOP), temperature, and power supply voltage implemented; results are available through the TWS interface. Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register.

The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm and fault information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of an alarm, LOS and/or Tx fault.

Receiver

The optical receiver portion of the transceiver (see Figure 1) incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, a 4 channel output buffer, diagnostic monitors, and control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ohms to AC ground and 100 Ohms differentially that should be differentially terminated with 100 Ohms. AC coupling capacitors are located inside the QSFP module and are not required on the host board.

Modules with Full Digital Diagnostic Monitoring have a monitor for optical input power; results are available through the TWS interface. Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds.

Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register.

The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm information are available via the TWS interface. To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of an alarm and/or LOS.

High Speed Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP module. For simplicity, only one channel is shown. As shown in Figure 2, the compliance points are on the host board side of the electrical connectors. Unused inputs and outputs should be terminated with 100 Ω differential loads.

QSFP compliance and reference points are as follows:

A: Host ASIC transmitter output at ASIC package contact on a DUT board – Reference point.

B: Host ASIC transmitter output across the Host Board and Host Edge Card connector at the Module Card Edge interface – Reference point.

B′: Host ASIC transmitter output across the Host Board at Host Edge Card Connector – Compliance point.

C: QSFP receiver output at the Module Card Edge Interface – Reference point.

C′: QSFP receiver output at Host Edge Card Connector – Compliance point.

D: QSFP receiver output at Host ASIC package receiver input contact on a DUT board – Reference point.

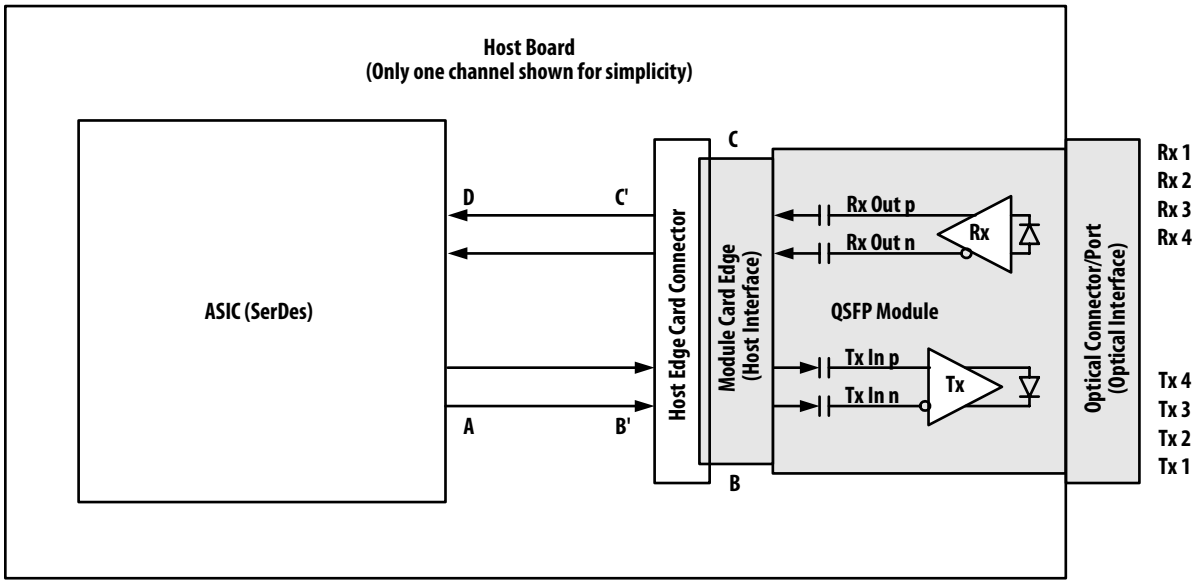


Figure 2. Application Reference Diagram

Control Signal Interface

The module has the following low speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, IntL. In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. The module is implemented as a slave device.

Signal and timing characteristics are further defined in the Control Interface section. The registers of the serial interface memory are defined in the Memory Map section and corresponding Avago Technologies QSFP Memory Map document.

Regulatory & Compliance Issues

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD and RoHS. See the Regulatory Section for details, including component recognition. Please note the transmitter module is a Class 1M laser product – DO NOT VIEW RADIATION DIRECTLY WITH OPTICAL INSTRUMENTS. See Regulatory Compliance Table for details. The AFBR-79Q4Z will support this table.

Package Outline

The module is designed to meet the package outline defined in the INF-8436i QSFP Transceiver Specification Revision 1.0 Multi-Source Agreement. See the package outline and host board footprint Figures 13-15 for details.

Handling and Cleaning

The transceiver module can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the optics remains clean and no addition cleaning should be needed. In the event of contamination, dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. The optical port features (e.g. guide pins) preclude use of a solid instrument. Liquids are also not advised.

Link Model and Reference Channel

Performance specifications for the AFBR-79Q4Z Transceiver are based on a reference channel model. A reference channel model provides the basis for inter-operability between independently produced transceiver modules. The reference model used for the AFBR-79Q4Z Transceiver is based on the industry standard 10GbE link model (10GEPBud3_1_16a.xls available at the IEEE P802.3ae 10Gb/s Ethernet Task Force Serial PMD Documents website: www.ieee802.org/3/ae/public/adhoc/serial_pmd/documents/).

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Reference
Storage Temperature	T_S	-40	100	°C	
3.3 V Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Data Input Voltage – Single Ended		-0.5	V_{CC}+0.5	V	
Data Input Voltage – Single Ended	$\|V_{DIP} - V_{DIN}\|$		1.0	V	1
Control Input Voltage	Vi	-0.5	V_{CC}+0.5, 3.6	V	
Control Output Current	Io	-20	20	mA	
Relative Humidity	RH	5	95	%	

Note:
1. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The equivalent input differential peak-to-peak voltage is twice this number.

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	Tc	0	40	70	°C	1
3.3 V Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Signal Rate per Channel		2.5		10.0	GBd	2
Control* Input Voltage High	Vih	2		Vcc+.3	V	
Control* Input Voltage Low	Vil	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate				400	kHz	
Power Supply Noise				50	mVpp	3
Receiver Differential Data Output Load			100		Ohms	
Fiber Length: 500 MHz·km 50μm MMF (OM2)		0.5		35	m	5
Fiber Length: 2000 MHz·km 50μm MMF (OM3)		0.5		100	m	

Notes:
* Control signals, LVTTL (3.3 V) compatible
1. The position of case temperature measurement is shown in Figure 5.
2. 8b10b coding is assumed
3. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 6 for recommended power supply filter.
4. Channel insertion loss includes 3.5 dB/km attenuation, 1.5 dB connector loss and 0.3 dB modal noise penalty allocations.

Transceiver Electrical Characteristics*

The following characteristics are defined over the recommended operating conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V.

Parameter	Symbols	Min	Typ	Max	Units	Reference
10G Transceiver Power Consumption			1.7	2	W	
10G Transceiver Power Supply Current			530	600	mA	
Transceiver Power On Initialization Time	$t_{pwr\ init}$			2000	ms	1

Notes:

1. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.

Transmitter Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V.

Parameter	Symbols	Min	Typ	Max	Units	Reference
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ PP\ LOS}$	50			mVpp	
LOS Hysteresis: Tx Data Input		0.5		4	dB	1
Test conditions for Optical Tx Characteristics:						
Data Input Differential Peak-to-Peak Voltage Swing	$\Delta V_{DI\ PP}$	175		1600	mVpp	2
Data Input Rise & Fall Times (20% – 80%)		30		42	ps	
Data Input Deterministic Jitter				15	ps	3
Data Input Total Jitter				30	ps	4
Eye Mask Coordinates: X1, X2, Y1, Y2 at TP6			0.15, 0.5 250, 600		UI mV	

Notes:

* For control signal timing including ModSelL, LPMode, ResetL, ModPrsL, IntL, SCL and SDA see Control Interface Section.

1. LOS Hysteresis is defined as 20 Log (LOS De-assert Level / LOS Assert Level).
2. This is a test condition and is not a required characteristic of the transceiver. It is a Tx Recommended Operating condition. Data inputs are CML compatible. Data Input Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DI\ pp} = \Delta V_{DIH} - \Delta V_{DIL}$ where ΔV_{DIH} = High State Differential Data Input Voltage and ΔV_{DIL} = Low State Differential Data Input Voltage.
3. This is a test condition and is not a required characteristic of the transceiver. It is a Tx Recommended Operating condition. Deterministic Jitter, DJ, conforms to the dual-Dirac model where TJ(BER) = DJ + 2Q(BER)RJrms and RJrms is the width of the Gaussian component. Here BER = 10^{-12}. DJ is measured with the same conditions as TJ. Effects of impairments in the test signal due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
4. This is a test condition and is not a required characteristic of the transceiver. It is a Tx Recommended Operating condition. Total Jitter, TJ, defined for a BER of 10^{-12}, is measured at the 50% signal level using a 10.0 GBd Pseudo Random Bit Sequence of length 2^7-1 (PRBS7), or equivalent, test pattern. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.

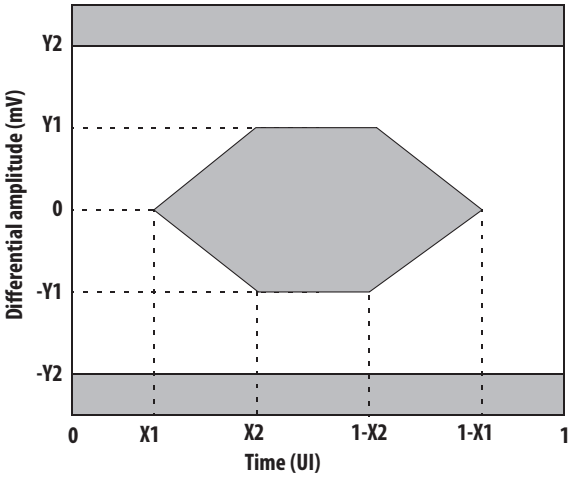


Figure 3. Electrical Eye Mask Coordinates at BER = 1 x 10^{-12}

Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Reference
Data Output Differential Peak-to-Peak Voltage Swing	$\Delta V_{DO\ pp}$	200		900	mVpp	1
Output Deterministic Jitter				40	ps	2
Output Total Jitter				72	ps	3
Eye Mask Coordinates: X1, X2, Y1, Y2			0.36, 0.5 100, 600		UI mV	

Notes:

1. Data outputs are CML compatible. Data Output Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DO\ pp} = \Delta V_{DOH} - \Delta V_{DOL}$ where ΔV_{DOH} = High State Differential Data Output Voltage and ΔV_{DOL} = Low State Differential Data Output Voltage. Impairments in measurements due to the test system are removed.
2. Deterministic Jitter, DJ, conforms to the dual-Dirac model where TJ(BER) = DJ + 2Q(BER)RJrms and RJrms is the width of the Gaussian component. Here BER = 10^{-12}. DJ is measured with the same conditions as TJ. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns at an input signal 6 dB above maximum Receiver Sensitivity.
3. Total Jitter, TJ, defined for a BER of 10^{-12}, is measured at the 50% signal level using a 10.0 GBd Pseudo Random Bit Sequence of length 2^7-1 (PRBS7), or equivalent, test pattern. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.

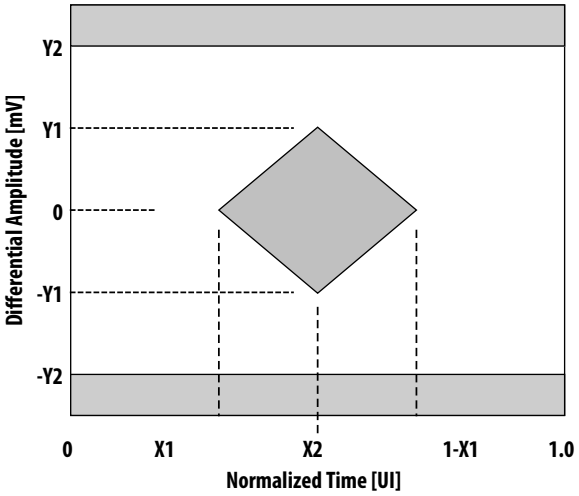


Figure 4. Rx Electrical Eye Mask Coordinates for BER = 1 x 10^{-12}

Transmitter Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Reference
Center Wavelength		840		860	nm	1
Spectral Width – rms				0.65	nm	
Output Optical Power: Average	$P_{O\ AVE}$			2.4	dBm	
Output Optical Modulation Amplitude, per lane		-6			dBm	2
Output OMA: Squelched				-27	dBm	
Launch power in OMA minus TDP, each lane		-6.9			dBm	
Transmitter and dispersion penalty (TDP), each lane				3.9	dB	
Extinction Ratio	ER	3			dB	
Output Optical Power: Disabled	$P_{O\ OFF}$			-30	dBm	
Transmitter Eye Mask X1, X2, X3, Y1, Y2, Y3		0.22, 0.37, 0.37, 0.31, 0.31, 0.4			UI	3

Notes:

1. The transmitter launch condition meets the requirements of 10 Gigabit Ethernet multimode fiber as detailed in TIA 492AAC.
2. Even if the TDP < 1 dB, the OMA (min) must exceed this value. A trade-off is permitted between TDP and OMA allowing lower values of OMA for low values of TDP. At maximum TDP of 3.9dB, the minimum OMA is -3dBm.
3. The transmitter eye mask test is absolute in terms of eye height (OMA) and relative in terms of time. It represents the minimum 1e-12 TX eye opening required to produce a 0.3 UI eye opening at TP4 of a compliant RX.

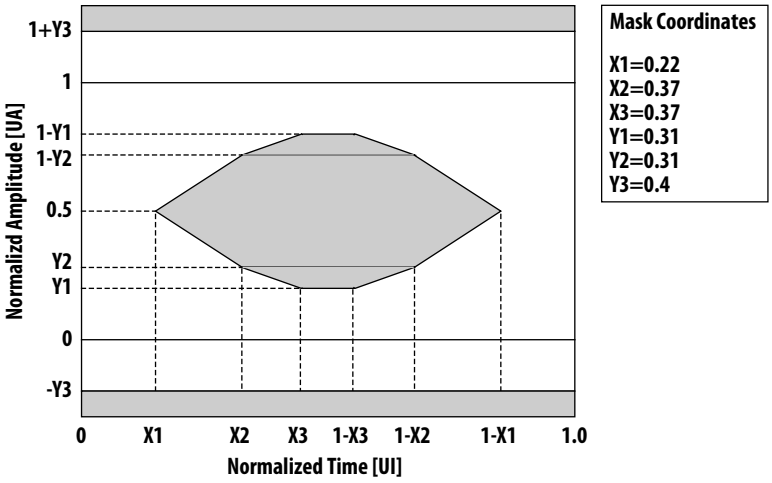


Figure 5. Transmitter Eye Mask – This eye mask is based up on a 5 e-5 hits per sample

Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Input Optical Power Saturation	$P_{SAT\ AVE}$	2.4			dBm	
Operating Center Wavelength		840		860	nm	
Return Loss		12			dB	
LOS Asserted Threshold – OMA	$P_{LOS\ OMA}$	-26			dBm	
LOS De-asserted – OMA				-10	dBm	
LOS Hysteresis		0.5			dB	
Stressed receiver sensitivity in OMA, each lane[1]				-5.5	dBm	

Notes:

1. Measured with conformance test signal at TP3 for BER = 10e-12; Conditions of stressed receiver sensitivity: Vertical Eye Closure Penalty, each lane = 2.2dB; Stressed eye J2 Jitter, each lane = 0.38 UI; Stressed eye J9 Jitter, each lane 0.51 UI

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	Transceiver module withstands 1000V
	JEDEC Charge Device Model (CDM) (JESD22-C101D)	Transceiver module withstands 500V
Electrostatic Discharge (ESD) to Optical Connector Receptacle	Variation of IEC 61000-4-2	Typically withstands at least 6 kV air discharge with module biased
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	Typically passes with 10 dB margin. Actual performance dependent on enclosure design
Immunity	Variation of IEC 61000-4-3	Typically minimum effect from a 10V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure
Laser Eye Safety and Equipment Type Testing	IEC 60825-1 Amendment 2 CFR 21 Section 1040	Pout: IEC AEL & US FDA CDRH Class 1M
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Compliance	BS EN 1122:2001 Mtd B by ICP for Cadmium, EPA Method 3051A by ICP for Lead and Mercury, EPA Method 3060A & 7196A by UV/Vis Spectrophotometry for Hexavalent Chromium. EPA Method 3540C/3550B by GC/MS for PPB and PBDE BS EN method by ICP and EPA methods by ICP, UV/Vis Spectrophotometry and GC/MS.	Less than 100 ppm of cadmium, Less than 1000 ppm of lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.

QSFP Transceiver Pad Layout

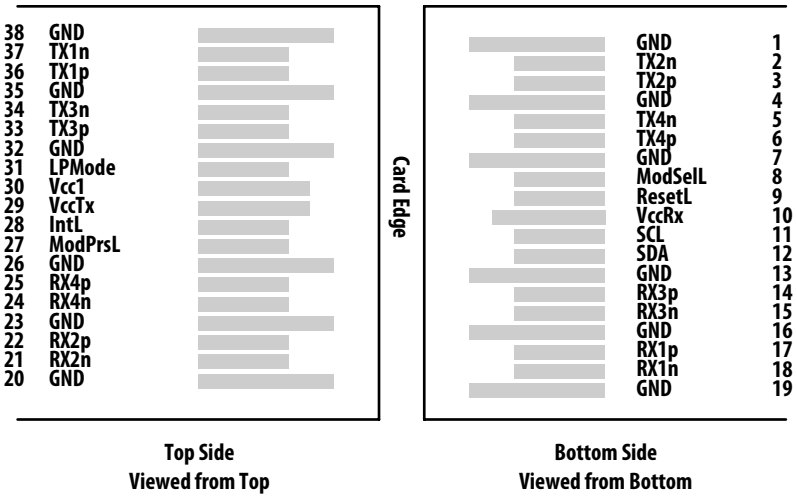


Figure 6. Host Board Pattern for QSFP Transceiver – Top View

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14		Rx3p	Receiver Non-Inverted Data Input	3	
15	CML-O	Rx3n	Receiver Inverted Data Input	3	
16	CML-O	GND	Ground	1	1
17		Rx1p	Receiver Non-Inverted Data Input	3	
18	CML-O	Rx1n	Receiver Inverted Data Input	3	
19	CML-O	GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Input	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Input	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Input	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Input	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal supply (power) common for the QSFP module. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

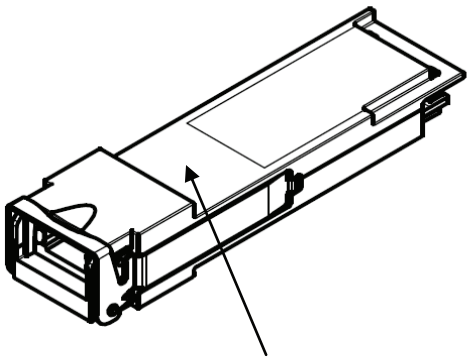


Figure 7. Case Temperature Measurement Point

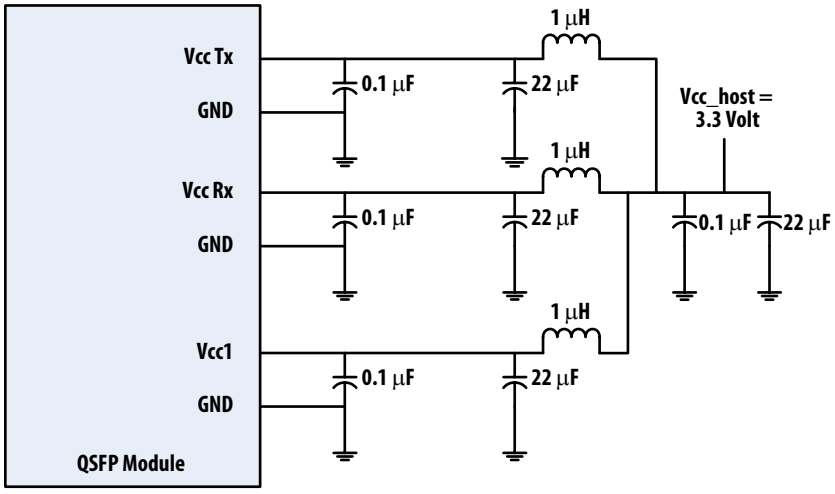


Figure 8. Recommended Power Supply Filter

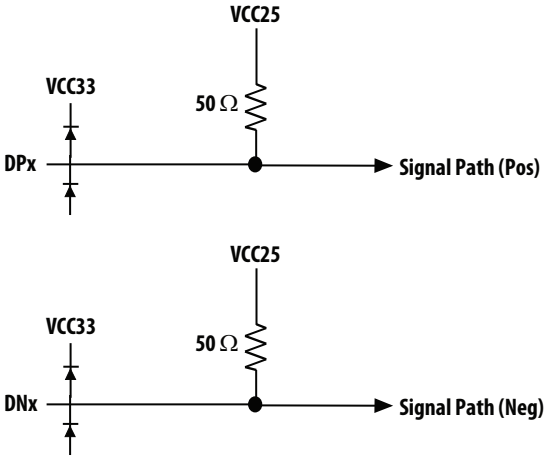


Figure 9. Transmitter Data Input Equivalent Circuit

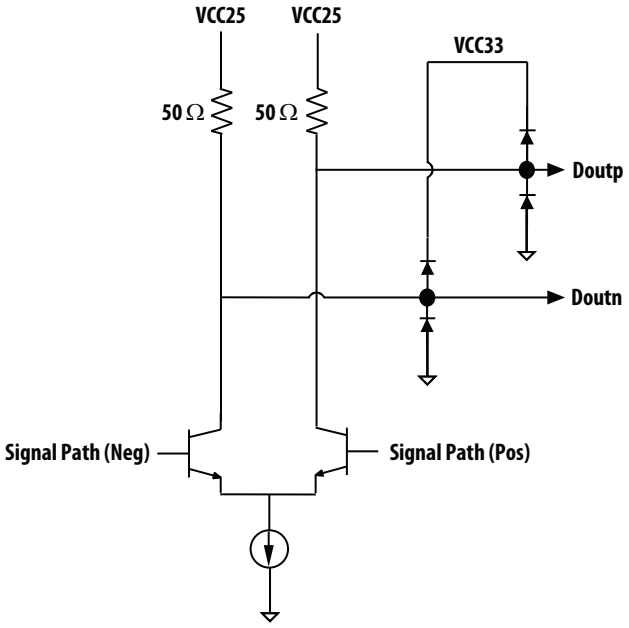


Figure 10. Receiver Data Output Equivalent Circuit

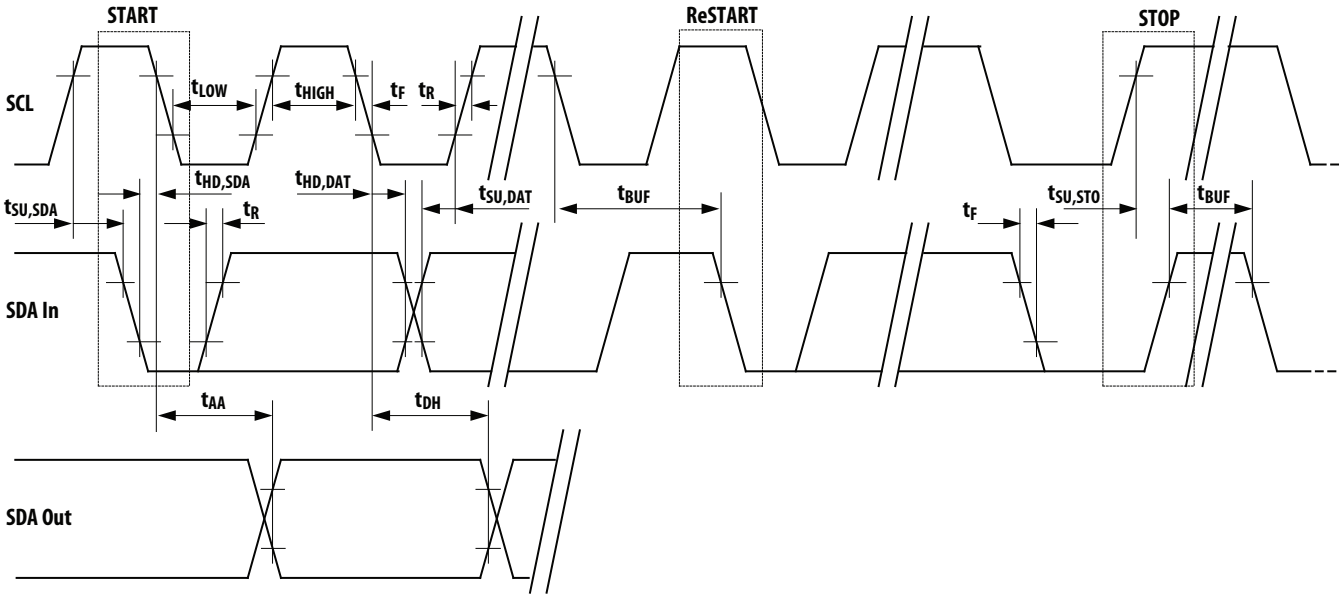


Figure 11. TWS Interface Bus Timing

Package Outline, Host PCB Footprint and Bezel Design

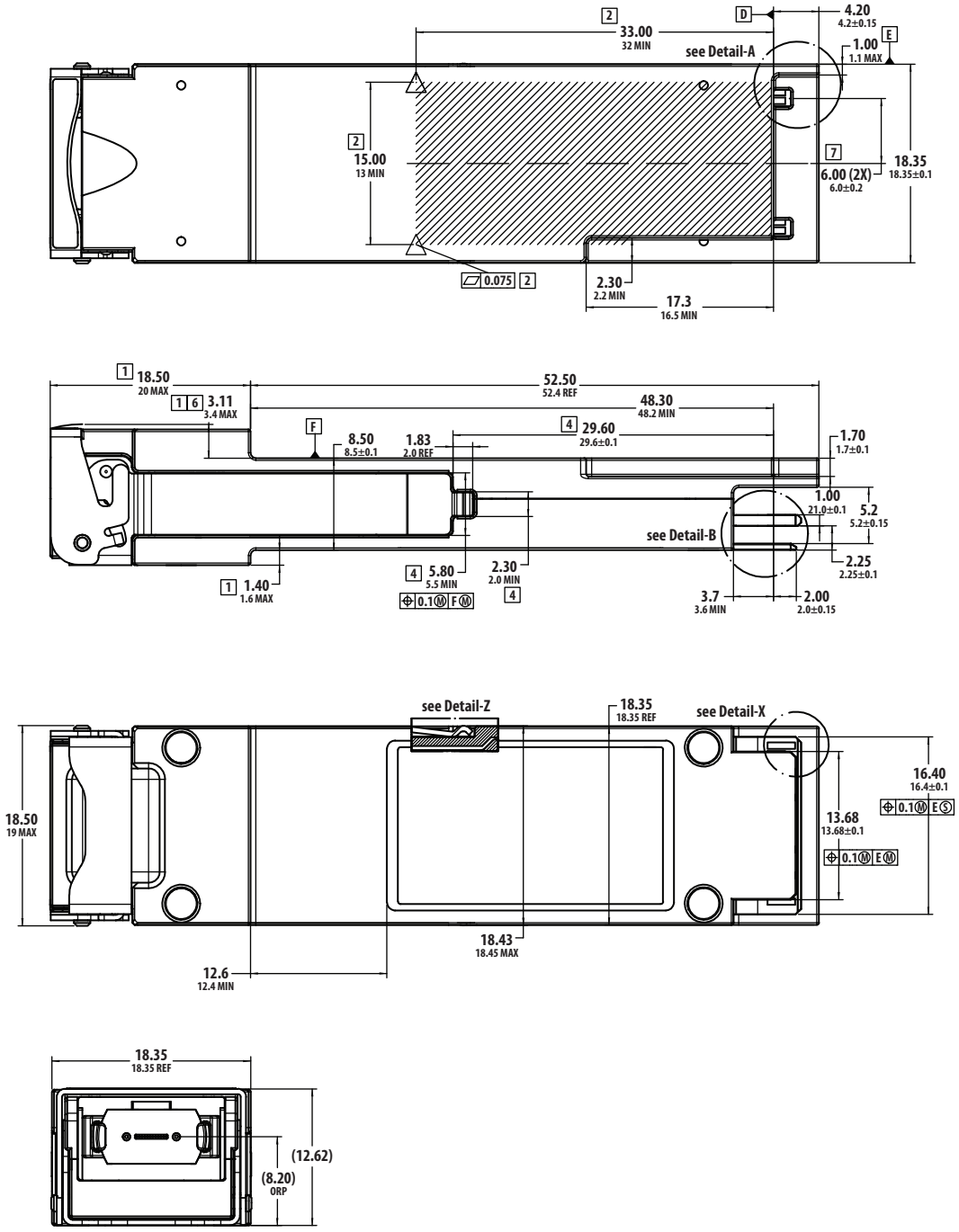


Figure 12. Mechanical Package Outline

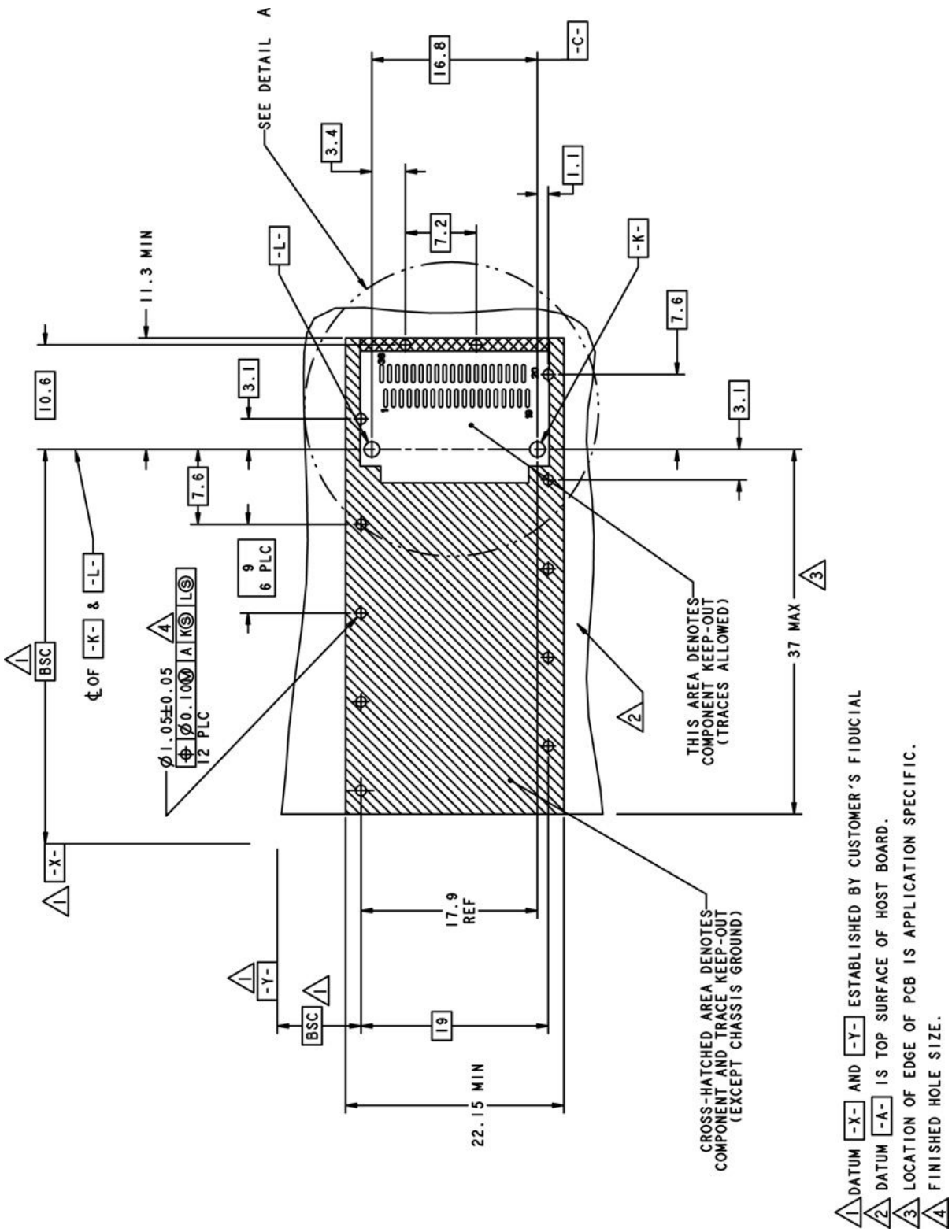


Figure 13. QSFP Host Board Mechanical Footprint

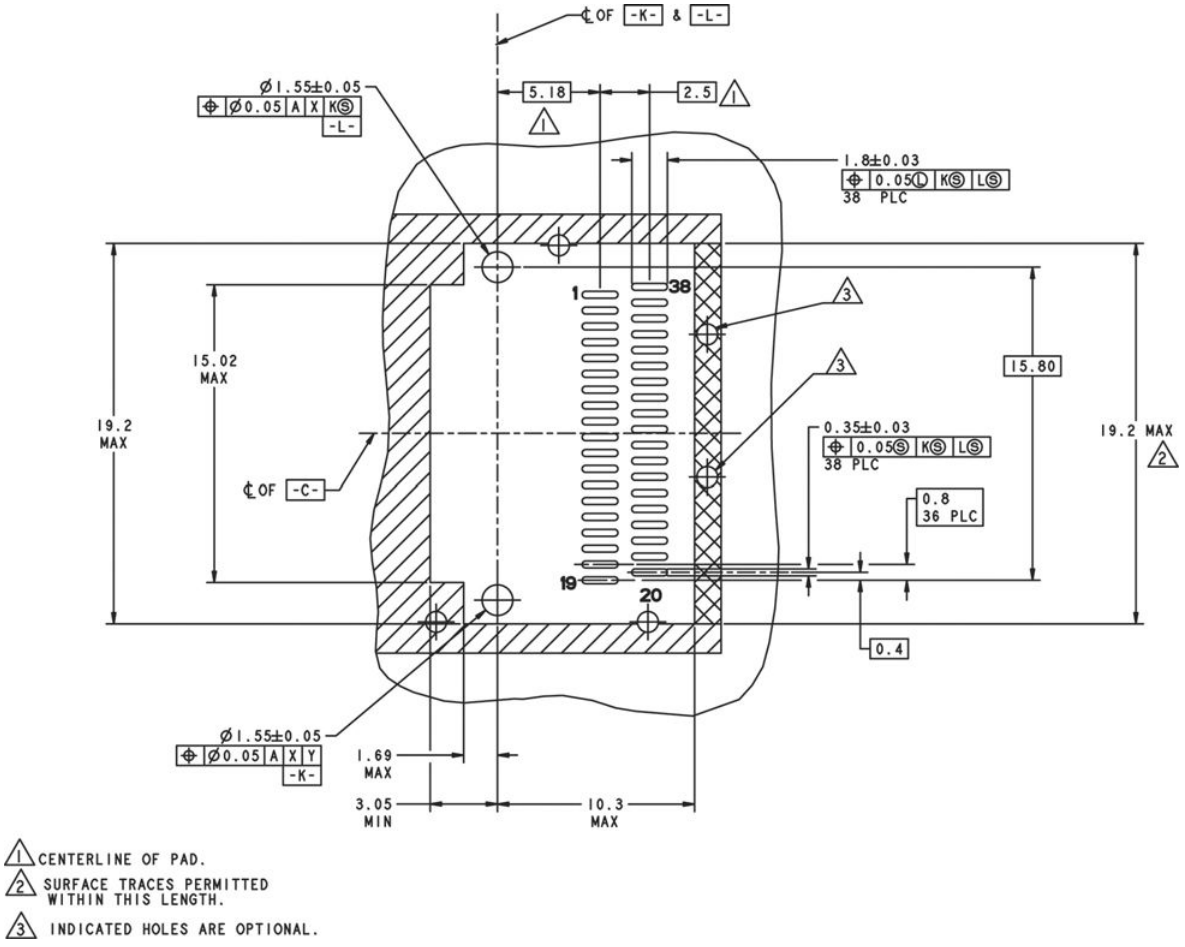


Figure 14. QSFP Host Board Mechanical Footprint Detail

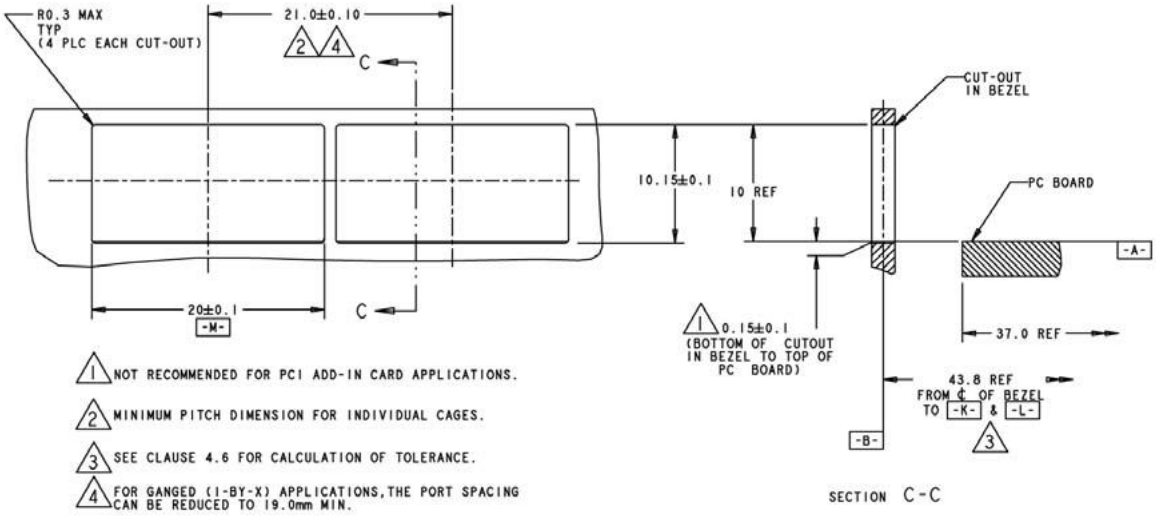


Figure 15. Host Board Bezel Design

Control Interface

The control interface combines dedicated signal lines for ModSelL, LPMode, ResetL, ModPrsL, IntL and two-wire serial (TWS) interface clock (SCL) and data (SDA) signals to provide users rich functionality over an efficient interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3 volt LVTTL. Outputs are high-Z in the high state to support busing of these signals. Signal and timing characteristics are further defined in the Control I/O Characteristics section. In general, TWS bus timing and protocols follow the implementation popularized in Atmel Two-wire Serial EEPROMs. For additional details see, e.g., Atmel AT24C01A.

ModSelL

The ModSelL is an input signal. When held low by the host, the module responds to Two-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single Two-wire interface bus. When the ModSelL is "High", the module will not respond to or acknowledge any Two-wire interface communication from the host. ModSelL signal input node is biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt Two-wire interface communications within the ModSelL de-assert time after any QSFP modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal is pulled to Vcc in the QSFP module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode

Low power mode. When held high by host, the module is held at low power mode. When held low by host, the module operates in the normal mode.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL

IntL is an output signal. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the Two-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board.

Modules with Full Digital Diagnostic Monitoring allow the user can read the present value of the various diagnostic monitors. For transmitters and receivers, internal module temperature and supply voltages are reported. For transmitters, monitors are provide for each channel laser bias current and laser light output power (LOP). For receivers, input power (Pave) is monitored for each channel. All monitor items are two-byte fields and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted.

A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, Tx fault and monitor flag. Entries in the mask fields are volatile.

I/O Timing for Control and Status Functions

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C, Vcc = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Reference
Initialization Time	t_init			2000		Time from power on, hot plug or rising edge of Reset until the module is fully functional. This time does not apply to non Power level 0 modules in the Low Power state
LPMode Assert Time	ton_LPMode			100	ms	Time from assertion of LPMode until the module power consumption enters power level 1
Interrupt Assert Time	ton_IntL			200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
Interrupt De-assert Time	Toff_IntL			500	μs	Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for RX LOS, TX Fault and other flag bits
Reset Init Assert Time	t_reset_init			2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Reset Assert Time	t_reset			2000	ms	Time from rising edge on the ResetL pin until the module is fully functional
Serial Bus Hardware Ready Time	t_serial			2000	ms	Time from power on until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data			2000	ms	Time from power on to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
RX LOS Assert Time	ton_los			100	ms	Time from RX LOS state to RX LOS bit set and IntL asserted
TX Fault Assert Time	ton_Txfault			200	ms	Time from TX Fault state to TX fault bit set and IntL asserted
Flag Assert Time	ton_Flag			220	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted.
Mask Assert Time	ton_Mask			100	ms	Time from mask bit set until associated IntL assertion is inhibited
Mask Deassert Time	toff_Mask			100	ms	Time from mask bit cleared until associated IntL operation resumes
Rate Select Change Time	t_ratesel			100	ms	Time from change of state of Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification
Power Set Assert Time	ton_Pdown			100	ms	Time from P_Down but set until module power consumption enters power level 1
Power Set Deassert Time	toff_Pdown			300	ms	Time from P_Down bit cleared until the module is fully functional
RX Squelch Assert Time	ton_Rxsq			80	μs	Time from loss of RX input signal until the squelched output condition is reached
RX Squelch Deassert Time	toff_Rxsq			80	μs	Time from resumption of RX input signals until normal RX output condition is reached
TX Squelch Assert Time	ton_Txsq			400	ms	Time from loss of TX input signal until the squelched output condition is reached
TX Squelch Deassert Time	toff_Txsq			400	ms	Time from resumption of TX input signals until nominal TX output condition is reached
TX Disable Assert Time	ton_txdis			100	ms	Time from TX Disable bit set until optical output falls below 10% of nominal
TX Disable Deassert Time	toff_txdis			400	ms	Time from TX Disable bit cleared until optical output rises above 90% of nominal
RX Output Disable Assert Time	ton_rxdis			100	ms	Time from RX Output Disable bit set until RX output falls below 10% of nominal
RX Output Disable Deassert Time	toff_rxdis			100	ms	Time from RX Output Disable bit cleared until RX output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis			100	ms	This applies to RX and TX Squelch and is the time from bit set until squelch functionality is disabled
Squelch Disable Deassert Time	toff_sqdis			100	ms	This applies to RX and TX Squelch and is the time from bit cleared until squelch functionality is enabled

Memory Map

The memory is structured as a single address, multiple page approach. The address is given as A0xh. The structure of the memory is shown in Figure 16. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. For a more detailed description of the QSFP memory map see the INF-8436i QSFP Transceiver Specification Revision 1.0 or the Avago Technologies QSFP Memory Map document.

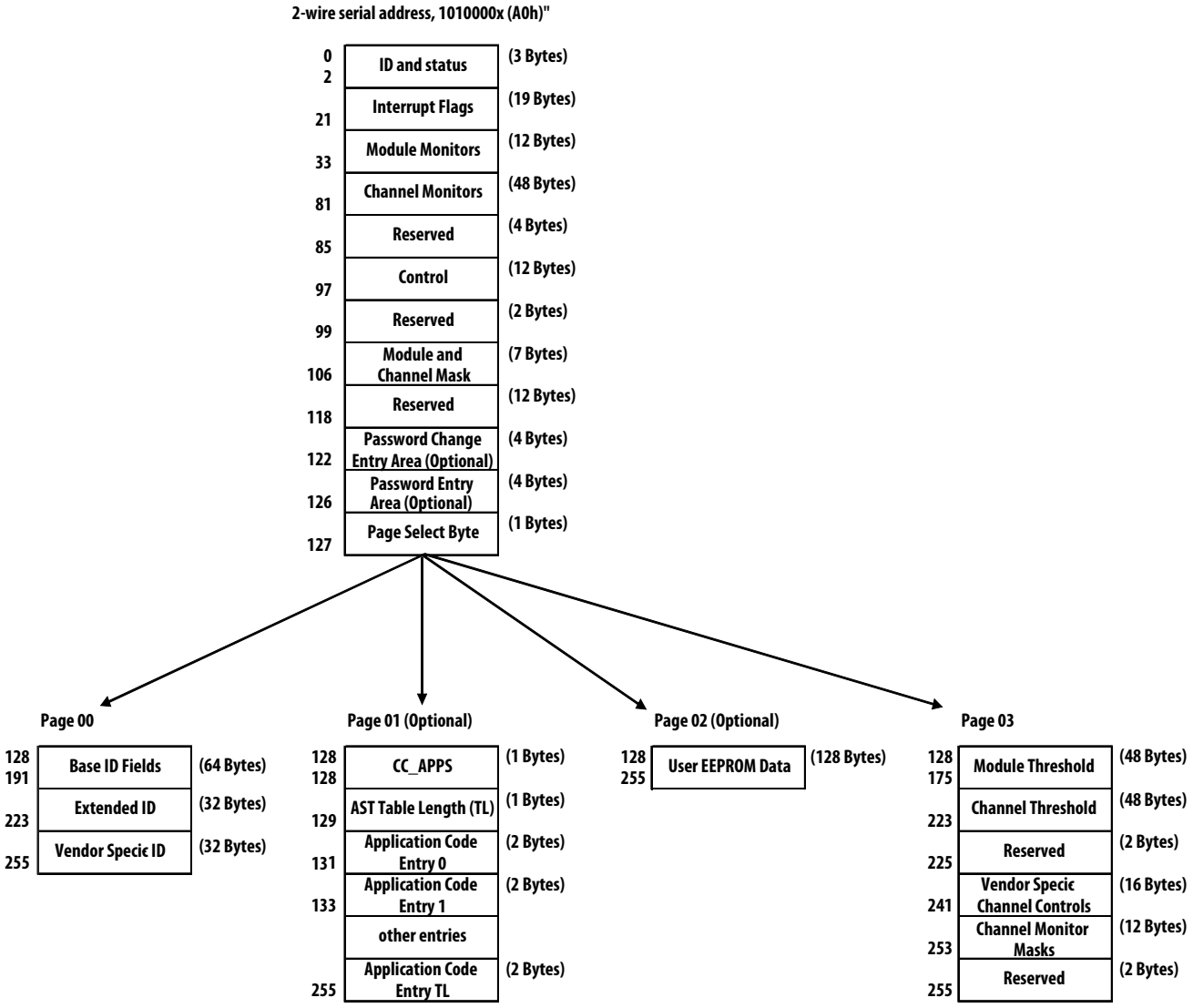


Figure 16. Two-Wire Serial Address A0xh Page Structure

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AV02-2162EN - January 28, 2013

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