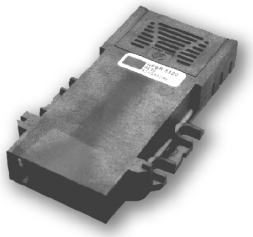
HFBR-5320Z
200 MBd RoHS Compliant SBCON
Multimode Fiber Transceiver

Data Sheet



Description
The HFBR-5320Z SBCON transceiver from Avago provides system designers with a product to implement a range of solutions compliant with the IBM® Enterprise System Connection (ESCON)® architecture.

Transmitter Section
The transmitter section of the HFBR-5320Z utilizes 1300 nm Surface Emitting InGaAsP LED. The LED is packaged in an optical sub-assembly within the transmitter section. The LED is driven by a custom silicon IC which converts differential PECL logic signals [ECL referenced (shifted) to a +5 Volt supply] into an analog LED drive current.

Receiver Section
The receiver section of the HFBR-5320Z utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. This PIN/preamplifier combination is coupled to a custom quantizer IC which provides the final pulse shaping for the logic Data Output and Status Flag function. The Data and Status Flag Outputs are differential PECL compatible [ECL referenced (shifted) to a +5 Volt power supply] logic outputs.

Package
The overall package concept for the Avago transceiver consists of the following basic elements: two optical sub-assemblies, an electrical sub-assembly and the housing with an integral duplex SBCON connector receptacle. This is illustrated in Figure 1.

The package outline and pin-out are shown in Figures 2 and 3. The package includes internal shields for the electrical and optical sub-assemblies to ensure low EMI emissions and high immunity to EMI fields.

Features
- Compliant with IBM® Enterprise Systems Connection (ESCON)® architecture
- Compliant to SBCON draft specification (dpANS X3.xxx-199x rev 2.2)
- Low radiated emissions and high immunity to conducted noise
- Multi-sourced 4 x 7 package style with ESCON® duplex connector interface
- Wave solder and aqueous wash process compatible
- Manufactured in an ISO 9001 certified facility
- 1300 nm LED-based transceiver
- Fully RoHS compliant

Applications
- Interconnection with IBM® compatible processors, directors, and channel attachment units
  - Disk and tape drives
  - Communication controllers
- Data communication equipment
  - Local area networks
  - Point-to-point communication

Note:
IBM, Enterprise System Connection Architecture, ESCON, are registered trademarks of International Business Machines Corporation.

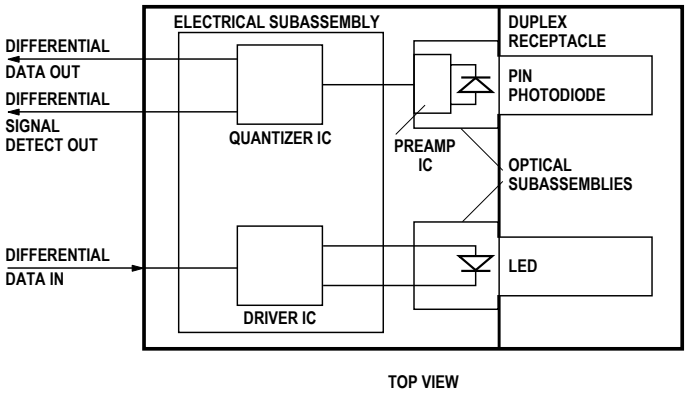


Figure 1. Block diagram.

The optical sub-assemblies utilize a high-volume assembly process together with low-cost lens elements which result in a cost-effective building block.

The electrical subassembly consists of a high-volume multi-layer printed circuit board on which the IC circuits and various surface-mount passive circuit elements are attached.

The outer housing, including the SBCON-compliant duplex connector receptacle, is molded of filled, non-conductive UL 94V-0 flame retardant Ultem® plastic (U.L. File E121562) to provide mechanical strength and electrical isolation.

The transceiver is attached to a printed circuit board with 28 signal pins (4 rows of 7 pins) and with the four slots on the flanges which are located on the package sides. These four slots on the flanges provide the primary mechanical strength to withstand the loads imposed by the duplex connectored fiber cables.

Applications Information

The Applications Engineering group in the Avago Optical Communications Division is available to assist you with the technical understanding associated with this transceiver. You can contact them through your local Avago sales representative.

Avago LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The Avago LED will normally experience less than half this amount of aging over normal, commercial equipment mission-life periods. Contact your local Avago sales representatives for additional details.

Recommended Handling Precautions

It is advised that normal, anti-static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The HFBR-5320Z transceiver meets Mil-Std-883C Method 3015.4 Class 2.

Care should be used to avoid shorting the receiver Data or Status Flag Outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceiver is delivered with a protective process plug inserted into the duplex SBCON connector receptacle. This process plug protects the optical sub-assemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping. These transceivers are compatible with either industry standard wave or hand soldering processes. The process plug part number is HFBR-5002.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Board Layout - Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from the transceiver. Figure 3 provides a good example of a schematic for a power supply decoupling circuit that works well with this part. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductive ground for signal return current. This recommendation is in keeping with good high-frequency board layout practices.

Note:
Ultem is a registered trademark of General Electric Corporation.

Regulatory Compliance

This transceiver product is intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your local Avago sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the SBCON-compatible duplex connector receptacle is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing this high-speed transceiver from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

This device is suitable for a variety of applications utilizing the IBM® ESCON® / SBCON architecture.

Immunity

Equipment utilizing this transceiver will be subject to radio-frequency electromagnetic fields in some environments. This transceiver has a high immunity to such fields.

Ordering Information

The HFBR-5320Z 1300 nm SBCON-compatible transceiver is available for production orders through the Avago Component Field Sales Offices and Authorized Distributors worldwide.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Meets Class 2 (2000 to 3999 Volts). Withstands up to 2200 V applied between electrical pins.
Electrostatic Discharge (ESD) to the Duplex SBCON Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the Duplex SBCON Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Typically provide a 20 dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers.

All HFBR-5320Z LED transmitters are classified as IEC-825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	−40		100	°C	
Lead Soldering Temperature	T_{SOLD}			260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	−0.5		7.0	V	
Data Input Voltage	V_I	−0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		70	°C	
Supply Voltage	V_{CC}	4.75		5.25	V	
Data Input Voltage - Low	V_{IL} - V_{CC}	−1.890		−1.475	V	
Data Input Voltage - High	V_{IH} - V_{CC}	−1.165		−0.810	V	
Data and Status Flag Output Load	R_L		50		Ω	Note 2

Transmitter Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		145	185	mA	Note 3
Power Dissipation	P_{DISS}		0.76	0.97	W	
Data Input Current - Low	I_{IL}	−350			µA	
Data Input Current - High	I_{IH}			350	µA	
Threshold Voltage	V_{BB} - V_{CC}	−1.42	−1.3	−1.24	V	Note 21

Receiver Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		100	125	mA	Note 4
Power Dissipation	P_{DISS}		0.5	0.66	W	Note 5
Data Output Voltage - Low	V_{OL} - V_{CC}	−1.890		−1.620	V	Note 6
Data Output Voltage - High	V_{OH} - V_{CC}	−1.060		−0.810	V	Note 6
Data Output Rise Time	t_r	0.35		1.3	ns	Note 7
Data Output Fall Time	t_f	0.35		1.3	ns	Note 7
Status Flag Output Voltage - Low	V_{OL} - V_{CC}	−1.890		−1.620	V	Note 6
Status Flag Output Voltage - High	V_{OH} - V_{CC}	−1.060		−0.810	V	Note 6
Status Flag Output Rise Time	t_r	0.35		2.2	ns	Note 7
Status Flag Output Fall Time	t_f	0.35		2.2	ns	Note 7

Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Max.	Unit	Reference
Output Optical Power 62.5 / 125 µm, NA = 0.275 Fiber	$P_{O\ BOL}$ $P_{O\ EOL}$	–20.5 –21.5	–15.0	dBm avg.	Note 9
Optical Extinction Ratio		8		dB	Note 22
Center Wavelength	λ_C	1280	1380	nm	
Spectral Width - FWHM	$\Delta\lambda$		175	nm	Note 11
Optical Rise Time	T_r		1.7	ns	Note 10, 12
Optical Fall Time	t_f		1.7	ns	Note 10, 12
Output Optical Systematic Jitter	t_{SJ}		0.8	ns p-p	Note 13

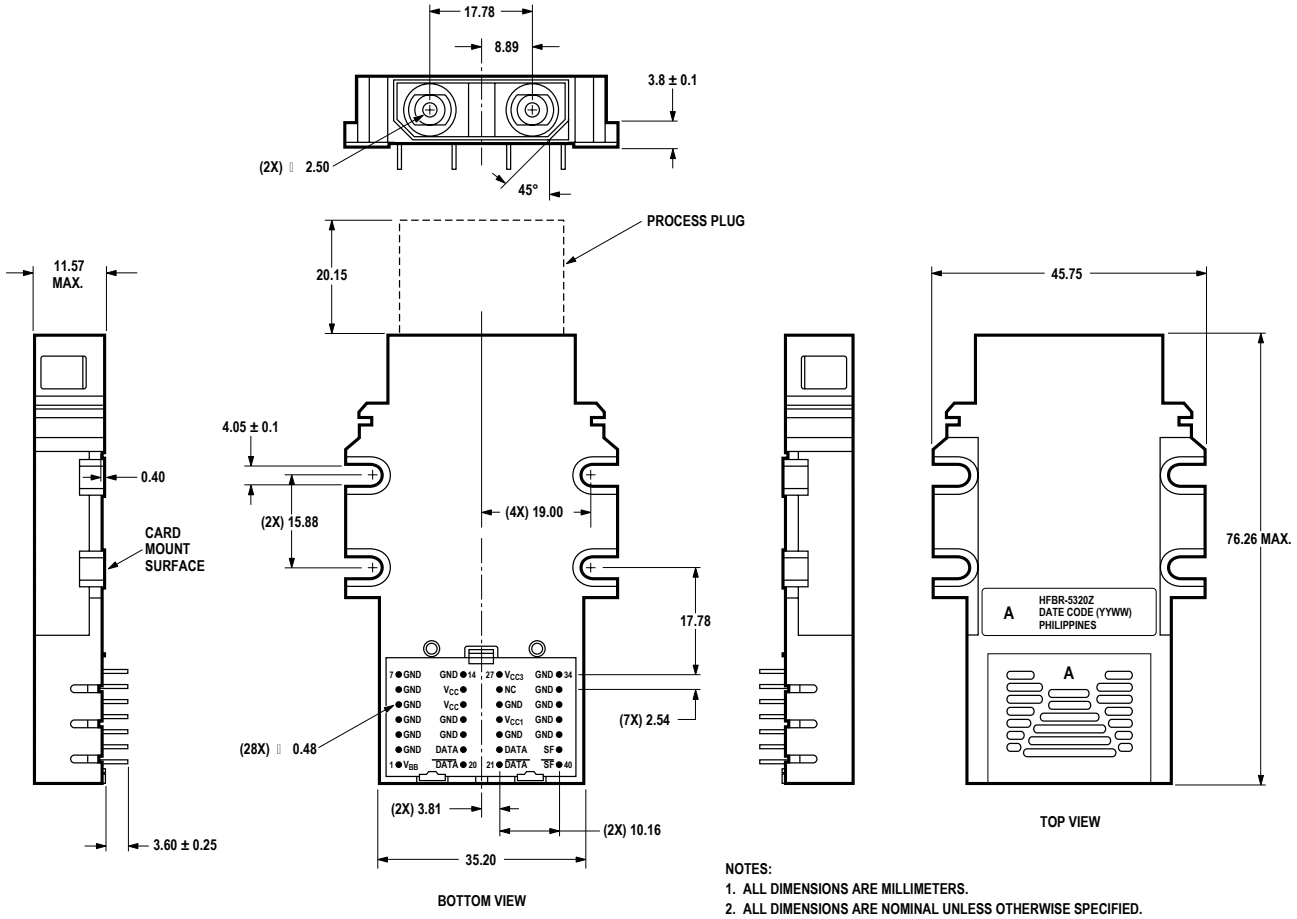
Receiver Optical and Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	P_{IN} Min. (W)		P_{IN} Min. (C) + 1.0 dB	dBm avg.	Note 14
Input Optical Power Minimum at Eye Center	P_{IN} Min. (C)		–29.0	dBm avg.	Note 15
Input Optical Power Maximum	P_{IN} Max.	–14.0		dBm avg.	Note 14
Operating Wavelength	λ	1280	1380	nm	
Systematic Jitter	SJ		1.0	ns p-p	Note 16
Eyewidth	t_{ew}	1.4		ns	Note 8
Status Flag - Asserted	P_A	–44.5	–35.5	dBm avg.	Note 17
Status Flag - Deasserted	P_D	–45	–36	dBm avg.	Note 17
Status Flag - Hysteresis	P_A - P_D	0.5		dB	Note 18
Status Flag Assert Time (off-to-on)	t_A	3	500	µs	Note 1
Signal Detect Deassert Time (off-to-on)	t_D	3	500	µs	Note 20

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to V_{CC} – 2V.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This value is measured with the outputs terminated into 50 Ω connected to V_{CC} – 2V and an Input Optical Power Level of –14.5 dBm average.
5. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
6. This value is measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} – 2V.
7. The output rise time and fall times are measured between 20% and 80% levels with the output connected to V_{CC} – 2V through 50 Ω.
8. Eye-width specified defines the minimum clock time-position range, centered around the center of the 5 ns baud interval, at which the BER must be 10^{-12} or better. Test data pattern is PRBS 2^7 – 1. The maximum change in input optical power to open the eye to 1.4 nsec from a closed eye is 1.0 dB.
9. These optical power values are measured with the following conditions:
   - The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is assumed to be 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in normal commercial environments will be <1.0 dB with Avago's 1300 nm LED products.
   - Over the specified operating voltage and temperature ranges.
   - Input Signal: 2^7 – 1 data pattern PseudoRandom Bit-Stream, 200 Mbit/sec NRZ code.
10. Input conditions: 100 MHz, square wave signal, input voltages are in the range specified for V_{IL} and V_{IH}.
11. From an assumed Gaussian-shaped wavelength distribution, the relationship between FWHM and RMS values for Spectral Width is 2.35 x RMS = FWHM.
12. Measured with electrical input signal rise and fall time of 0.35 to 1.3 ns (20-80%) at the transmitter input pins. Optical output rise and fall times are measured between 20% and 80% levels.
13. Transmitter Systematic Jitter is equal to the sum of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ). DCD is equivalent to Pulse-Width Distortion (PWD). Systematic Jitter is measured at the 50% signal level with 200 MBd, PRBS 2^7 – 1 electrical input data pattern.
14. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following conditions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 10^{-15}.
   - At the Beginning of Life (BOL).
   - Over the specified operating temperature and voltage ranges.
   - Receiver data window time-width is 1.4 ns or greater and centered at mid-symbol.
   - Input signal is 200 MBd, PseudoRandom-Bit-Stream 2^7 – 1 data pattern.
   - Transmitter cross-talk effects have been included in Receiver sensitivity. Transmitter should be running at 50% duty cycle (nominal) between 8 - 200 Mbps, while Receiver sensitivity is measured.
15. All conditions of note 14 apply except that the measurement is made at the center of the symbol with no window time-width.
16. The receiver systematic jitter specification applies to optical powers between –14.5 dBm avg. to –27.0 dBm avg. at the receiver. Receiver Systematic Jitter is equal to the sum of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ). DCD is equivalent to Pulse-Width Distortion (PWD). Systematic Jitter is measured at the 50% signal level with 200 MBd, PRBS 2^7 – 1 electrical output data pattern.
17. Status Flag switching thresholds: Direction of decreasing optical power If Power >–36.0 dBm avg., then SF = 1 (high)
    If Power <–45.0 dBm avg., then SF = 0 (low)
    Direction of increasing optical power:
    If Power <–45.5 dBm avg., then SF = 0 (low)
    If Power >–35.5 dBm avg., then SF = 1 (high)
18. Status Flag Hysteresis is the difference in low-to-high and high-to-low switching thresholds. Thresholds must lie within optical power limits specified. The Hysteresis is desired to avoid Status Flag chatter when the optical input is near the threshold.
19. The Status Flag output shall be asserted with 500 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power <–45.5 dBm avg., to >–35.5 dBm avg.
20. Status Flag output shall be de-asserted within 500 µs after a step decrease in the Input Optical Power. The Step will be from a high Input Optical Power >–36.0 dBm avg. to <–45.0 dBm avg.
21. This value is measured with an output load of R_L = 10 kΩ.
22. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical and expressed in decibels. With the transmitter driven by a HALT Line State (12.5 Mhz square-wave) signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The Extinction Ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed in decibels.



NOTES:

1. ALL DIMENSIONS ARE MILLIMETERS.
2. ALL DIMENSIONS ARE NOMINAL UNLESS OTHERWISE SPECIFIED.
3. IO PINS ARE MADE UP OF PHOSPHORBRONZE BASE WITH AN INTERMEDIATE NI PLATE AND A FINAL LAYER OF 100% MATTE TIN.
4. LABEL INFORMATION REFER TO Ð05.

Figure 2. Package outline drawing.

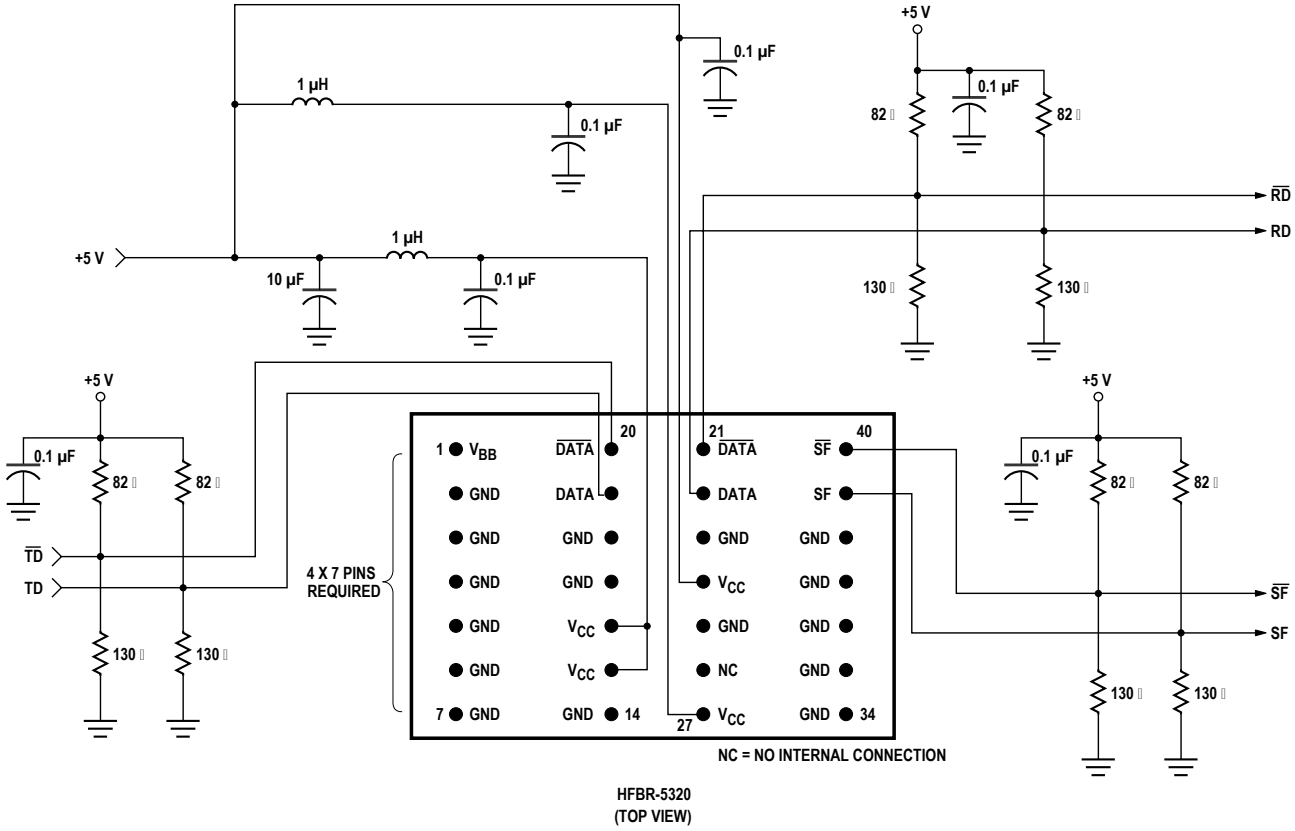


Figure 3.

Notes:

1. Resistance is in Ohms. Capacitance is in microfarads. Inductance is in microhenries.
2. Terminal transmitter input Data and Data-bar at the transmitter input pins. Terminate the receiver Output Data, Data-bar, Status Flag, and Status Flag-bar at the follow-on device input pins. For lower power dissipation in the Status Flag termination circuitry with small compromise to the signal quality, each Status Flag output can be loaded with 510 Ohms to ground instead of the two resistor, split -load PECL termination shown in the Figure 3 schematic.
3. Make differential signal paths short and same length with equal termination impedance.
4. Signal traces should be 50 Ohms microstrip or stripline transmission lines. Use multilayer, ground-plane printed circuit board for best high-frequency performance.
5. Use high-frequency, monolithic ceramic bypass capacitors and low series dc resistance inductors. Recommend use of surface-mount coil inductors and capacitors. In low noise power supply systems, ferrite bead inductors can be substituted for coil inductors. Locate power supply filter components close to their respective power supply pins.
6. Device ground pin should be directly and individually connected to ground.
7. Caution: Do not directly connect the fiber-optic module PECL outputs (Data, Data-bar, Status flag, Status Flag-bar, V_{BB}) to ground without proper current limiting impedance.

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies Limited in the United States and other countries.
Data subject to change. Copyright © 2008 Avago Technologies Limited. All rights reserved. Obsoletes AV01-0189EN
AV02-0607EN - January 21, 2008