AFBR-5302Z

Fibre Channel 266 MBd Transceiver in 1x9 Package Style

Data Sheet

Description

The AFBR-5302Z Fibre Channel Transceivers from Avago Technologies provide the system designer with products to implement Fibre Channel designs for use in multimode fiber (MMF) applications. This includes the 25 MB/sec, 25-M6-LE-I interface for 1300 nm LED links.

The products are produced in the industry standard 1x9 SIP package style with a duplex SC connector interface as defined in the Fiber Channel ANSI FC-PH standard document.

The AFBR-5302Z is a 1300 nm transceiver specified for use in 266 MBd, 25 MB/s, 25-M6-LE-I Fibre Channel interfaces to either 62.5/125 mm or 50/125 mm multimode fiber-optic cables.

Features

- Fully RoHS Compliant
- Full Compliance with ANSI X3T11 Fibre Channel Physical and Signaling Interface
- Multisourced 1x9 Package Style with Duplex SC Connector
- Wave Solder and Aqueous Wash Process Compatibility
- Compatible with Various Manufacturers FC-0 and FC-1 Circuits

Applications

- Fibre Channel 25 MB/s 25-M6-LE-I Interfaces for 1300 nm LED Links to 1500 m

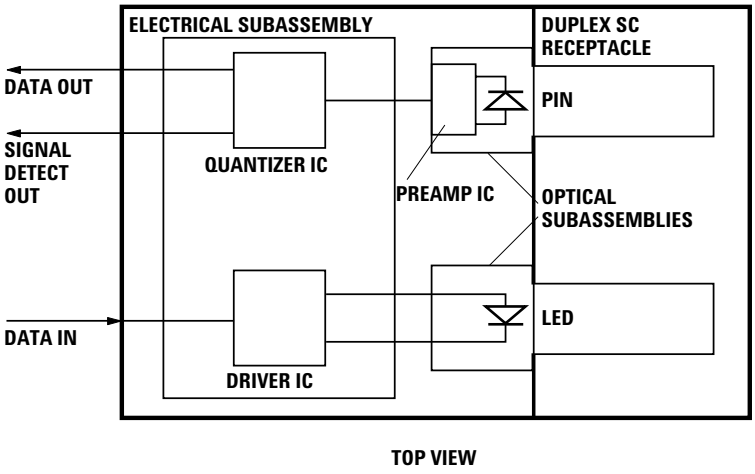


Figure 1. Block Diagram.

Transmitter Sections

The transmitter section of the AFBR-5302Z utilizes 1300 nm InGaAsP LEDs. These LEDs are packaged in the optical subassembly portion of the transmitter section. They are driven by a custom silicon IC which converts PECL logic signals, into an analog LED drive current.

Receiver Sections

The receiver section of the AFBR-5302Z utilizes InGaAs PIN photo diodes coupled to a custom silicon transimpedance preamplifier IC.

These are packaged in the optical subassembly portion of the receiver.

These PIN/preamplifier combinations are coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. The Data output is differential. The Signal Detect output is single-ended. Both data and signal detect outputs are PECL compatible, ECL referenced (shifted) to a +5 volt power supply.

Package

The overall package concept for the Avago Technologies Fibre Channel transceiver consists of three basic elements; the two optical subassemblies, an electrical subassembly and the housing with integral duplex SC connector interface. This is illustrated in the block diagram in Figure 1.

The package outline drawing and pin out are shown in Figures 2 and 3. The details of this package outline and pin out are compliant with the multisource definition of the 1x9 single in-line package (SIP). The low profile of the Avago Technologies transceiver design complies with the maximum height allowed for the duplex SC connector over the entire length of the package.

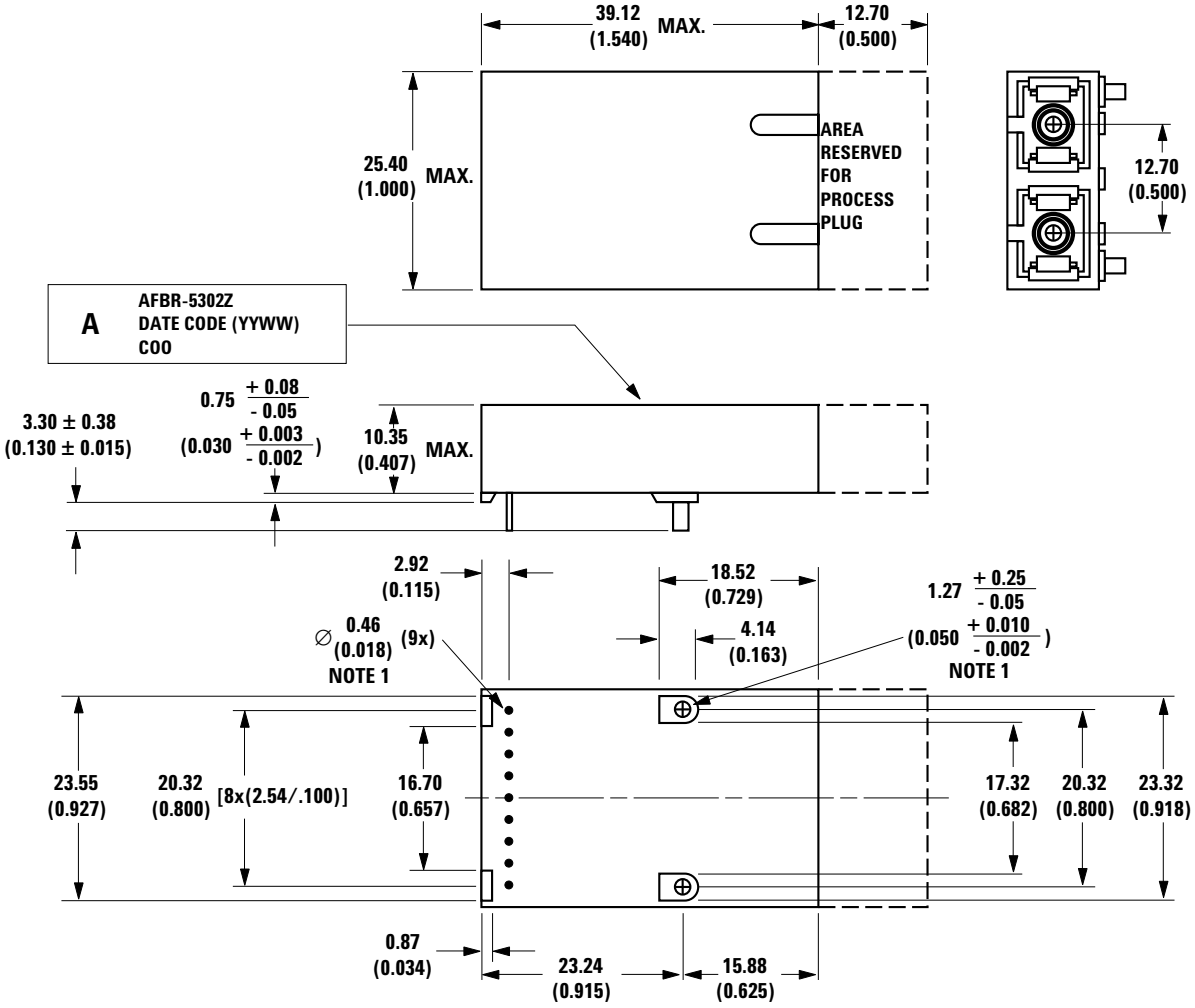
The optical subassemblies utilize a high volume assembly process together with low cost lens elements which result in a cost effective building block. The electrical subassembly consists of a high volume multilayer printed circuit board to which the IC chips and various surfacemount passive circuit elements are attached.

The package includes internal shields for the electrical and optical subassemblies to insure high immunity to external EMI fields and low EMI emissions. The outer housing, including the duplex SC connector, is molded of filled non-conductive plastic to provide mechanical strength and electrical isolation. The solder posts are isolated from the circuit design of the transceiver, while they can be connected to a ground plane on the circuit board, doing so will have no impact on circuit performance.

The transceiver is attached to a printed circuit board with the nine signal pins and the two solder posts which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with the duplex SC connectored fiber cables.

Application Information

The Applications Engineering group in the Avago Technologies Fiber Optic Products Division is available to assist with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your local Avago Technologiessales representative. The following information is provided to answer some of the most common questions about the use of these parts.



DIMENSIONS ARE IN MILLIMETERS (INCHES).

Figure 2. Package Outline Drawing.

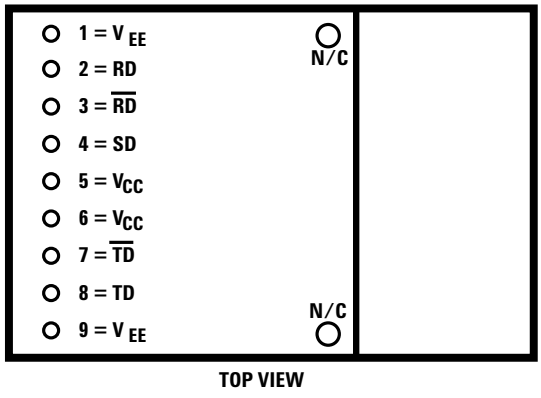


Figure 3. Pinout Diagram.

Compatibility with Fibre Channel FC-0/1 Chip Sets

The AFBR-5302Z transceivers are compatible with various manufacturers FC-0 and FC-1 integrated circuits. Evaluation boards, which include the Avago Technologies transceivers, are available from these manufacturers. The Applications Engineering group in the Avago Technologies Fiber Optic Products Division is available to assist you with implementation details.

Transceiver Optical Power Budget vs. Link Length

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair. Figure 4 illustrates the predicted OPB associated with the two transceivers specified in this data sheet at the Beginning of Life (BOL). These curves represent the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125 mm and 50/125 mm fiber cables only. The area under the curves represents the remaining OPB at any link length, which is available for overcoming non-fiber cable losses.

Avago Technologies LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The Avago Technologies LEDs will experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Avago Technologies sales representative for additional details.

Figure 4 was generated with an Avago Technologies fiber optic link model containing the current industry conventions for fiber cable specifications and the Fibre Channel optical parameters. These parameters are reflected in the specified performance of the transceiver in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI X3T9.5 committee, to establish the optical performance requirements for various fiber-optic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

Transceiver Signaling Operating Rate Range and BER Performance

For purposes of definition, the symbol rate (Baud), also called signaling rate, is the reciprocal of the symbol time. Data rate (bits/ sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit). The specifications in this data sheet have all been measured using the standard Fibre Channel symbol rates of 266 MBd.

The transceivers may be used for other applications at signaling rates different than specified in this data sheet. Depending on the actual signaling rate, there may be some differences in optical power budget to do this. This is primarily caused by a change of receiver sensitivity.

These transceivers can also be used for applications which require different Bit Error Rate (BER) performance. Figure 5 illustrates the typical trade-off between link BER and the receivers input optical power level.

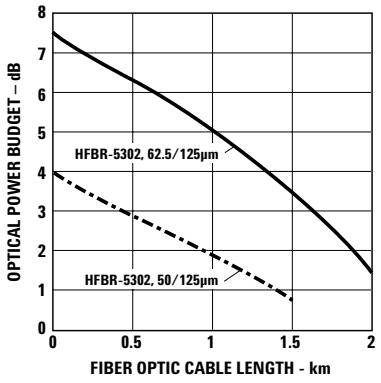


Figure 4. Optical Power Budget vs. Fiber Optic Cable Length.

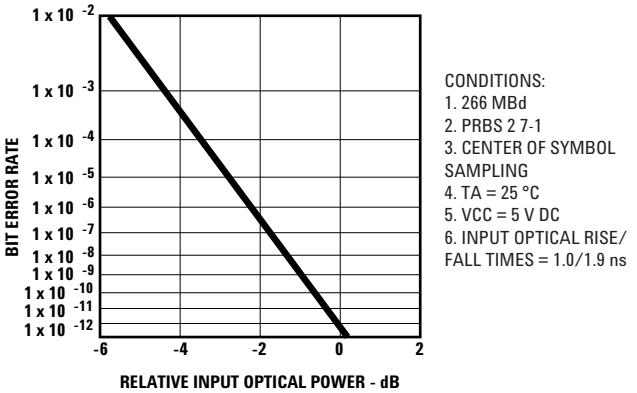


Figure 5. AFBR-5302Z Bit Error Rate vs. Relative Receiver Input Optical Power.

Transceiver Jitter Performance

The Avago Technologies 1300 nm transceivers are designed to operate per the system jitter allocations stated in FC-PH Annex A.4.3 and A.4.4. The Avago Technologies 1300 nm transmitters will tolerate the worst case input electrical jitter allowed, without violating the worst case output optical jitter requirements. The Avago Technologies 1300 nm receivers will tolerate the worst case input optical jitter allowed without violating the worst case output electrical jitter allowed.

The jitter specifications stated in the following tables are derived from the values in FC-PH Annex A.4.3 and A.4.4. They represent the worst case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the allowed allocation. In practice, the typical contribution of the Avago Technologies transceivers is below these maximum allowed amounts.

Recommended Handling Precautions

Avago Technologies recommends that normal static precautions be taken in handling and assembly of these transceivers to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD). These transceivers are certified as MIL-STD- 883C Method 3015.4 Class 2 devices.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground.

Solder and Wash Process Compatibility

The transceivers are delivered with a protective process plug inserted into the duplex SC connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping.

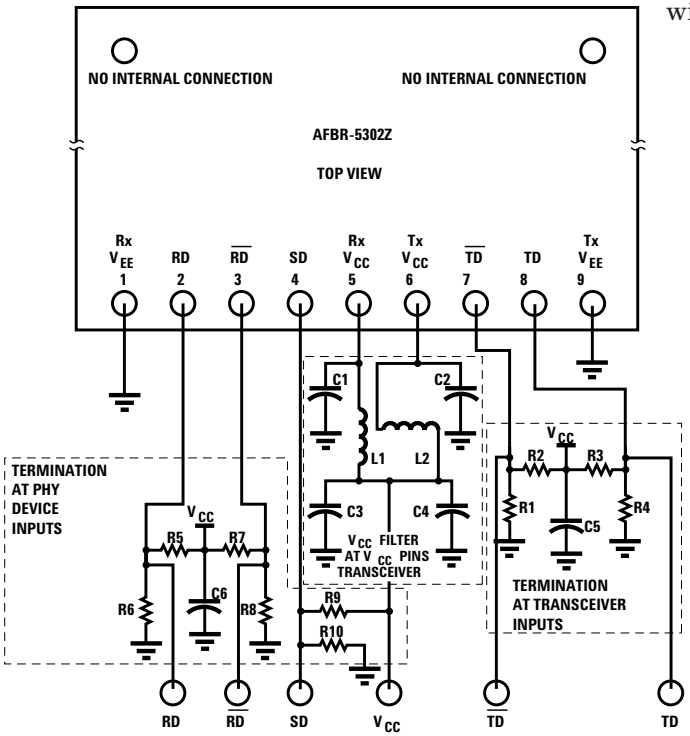
These transceivers are compatible with industry standard wave and hand solder processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Board Layout – Decoupling Circuit and Ground Planes

You should take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 6 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. Avago Technologies further recommends that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR ECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE ECL SIGNALS. RECOMMEND 4-LAYER PRINTED CIRCUIT BOARD WITH 50 OHM MICROSTRIP SIGNAL PATHS BE USED.
R1 = R4 = R6 = R8 = R10 = 130 ohms.
R2 = R3 = R5 = R7 = R9 = 82 ohms.
C1 = C2 = C3 = C5 = C6 = 0.1 µF.
C4 = 10 µF.
L1 = L2 = 1 µH COIL OR FERRITE INDUCTOR.

Figure 6. Recommended Decoupling and Termination Circuits.

Board Layout - Hole Pattern

The Avago Technologies transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement for the 1x9 pin package style. This drawing is reproduced in Figure 7 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board.

Regulatory Compliance

These transceiver products are intended to enable system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago Technologies will need to meet the requirements of the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The AFBR-5302Z is suitable for use in designs ranging from a single transceiver in a desktop computer to large quantities of transceivers in a hub, switch or concentrator.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. You should use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the transceiver duplex SC connector is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Immunity

Equipment utilizing these transceivers will be subject to radiofrequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields (see AN1075, "Testing and Measuring Electromagnetic Compatibility Performance of the HFBR-510X/ 520X Fiber-Optic Transceivers," 5963- 3358E).

Transceiver Reliability and Performance Qualification Data

The 1x9 transceivers have passed Avago Technologies reliability and performance qualification testing and are undergoing ongoing quality monitoring. Details are available from your Avago Technologies sales representative.

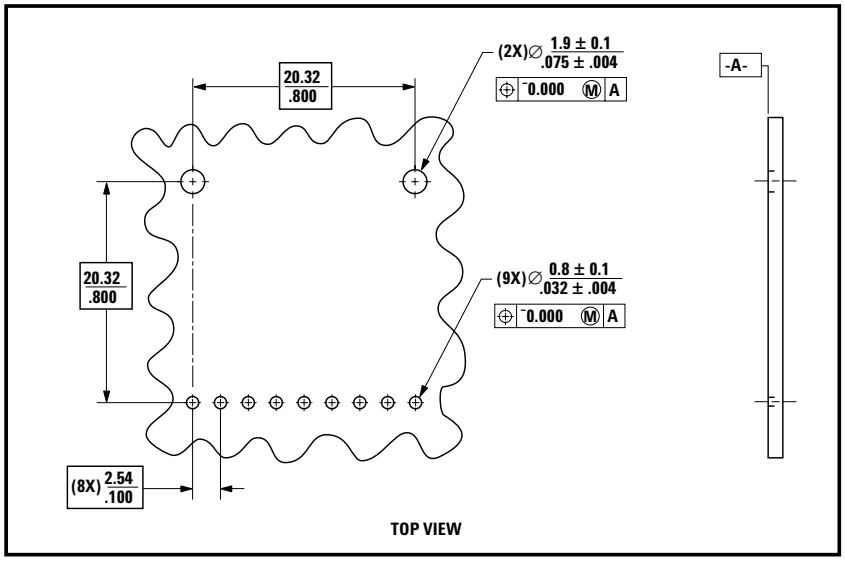
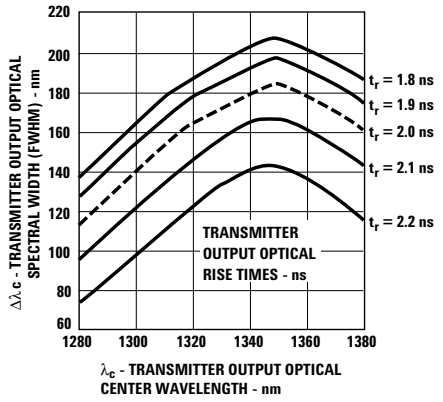


Figure 7. Recommended Board Layout Hole Pattern.

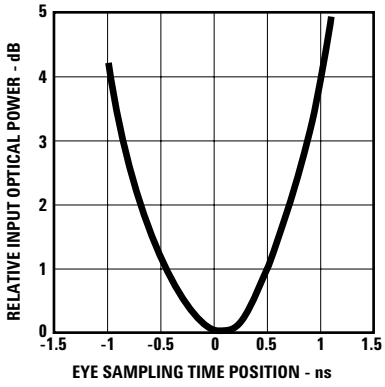
Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	Mil-STD-883C Method 3015.7	Class 2 (2000 to 3999 Volts) Withstand up to 2200 V applied between electrical pins.
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the Duplex SC Connector Receptacle is contacted by a Human Body Model Probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Transceivers typically provide a 7 dB margin at 266 MBd to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers.



AFBR-5302Z Typical Transmitter test results of λc, Δλ and tr are correlated and comply with the allowed spectral width as a function of center wavelength for various rise and fall times.

Figure 8. Typical Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.



CONDITIONS:
1. T A = 25 °C
2. V CC = 5 V DC
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/1.9 ns
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL
5. NOTES 11 AND 12 APPLY

Figure 9. AFBR-5302Z, Relative Input Optical Power vs. Eye Sampling Time Position.

Ordering Information

The AFBR-5302Z 1300 nm product is available for production orders through the Avago Technologies Component Sales Offices and Authorized Distributors world wide.

Applications Support Materials

Contact your local Avago Technologies Component Field Sales Office for information on how to obtain Test fixtures for the 1x9 transceivers.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Lead Soldering Temperature	T_{SOLD}			260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature - Ambient	T_A	0		70	°C	
Supply Voltage	V_{CC}	4.75		5.25	V	
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 3

Receiver Electrical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{cc}		100	165	mA	Note 15
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 16
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 17
Data Output Voltage - High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 17
Data Output Rise Time	t_r	0.35		2.2	ns	Note 18
Data Output Fall Time	t_f	0.35		2.2	ns	Note 18
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 17
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 17
Signal Detect Output Rise Time	t_r	0.35		2.2	ns	Note 18
Signal Detect Output Fall Time	t_f	0.35		2.2	ns	Note 18
Signal Detect Assert Time (off to on)	AS_Max	0	55	100	µs	Note 19
Signal Detect Deassert Time (off to on)	ANS_Max	0	110	350	µs	Note 20

Transmitter Electrical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		165	205	mA	Note 4
Power Dissipation	P_{DISS}		0.86	1.1	W	Note 4
Data Input Current - Low	I_{IL}	-350	0		µA	
Data Input Current - High	I_{IH}		14	350	µA	

Transmitter Optical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 μm, NA = 0.275 Fiber	P_O, BOL P_O, EOL	-19 -20		-14 -14	dBm avg. dBm avg.	Note 5
Output Optical Power 50/125 μm, NA = 0.20 Fiber	P_O, BOL	-22.5		-14	dBm avg.	Note 5
Optical Extinction Ratio				0.03 -35	% dB	Note 6
Center Wavelength	λ_C	1280	1308	1380	nm	Note 7 Figure 8
Spectral Width - FWHM	$\Delta\lambda$		137		nm	Note 7 Figure 8
Optical Rise Time	t_r	0.6		2.0	ns	Note 8 Figure 8
Optical Fall Time	t_f	0.6		2.2	ns	Note 8 Figure 8
Deterministic Jitter Contribution of Transmitter	DJ_C			0.08T 0.30	 ns p-p	Note 9
Random Jitter Contribution of Transmitter	RJ_C			0.03T 0.11	 ns p-p	Note 10

Receiver Optical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min.}$ (W)			-26	dBm avg.	Note 11 Figure 9
Input Optical Power Minimum at Eye Center	$P_{IN\ Min.}$ (C)			-28	dBm avg.	Note 12 Figure 9
Input Optical Power Maximum	$P_{IN\ MAX}$	-14			dBm avg.	Note 11
Operating Wavelength	λ	1270		1380	nm	
Signal Detect - Asserted	P_A	P_D +1.5dB		-27	dBm avg.	Note 13, 19
Signal Detect - Deasserted	P_D	-45			dBm avg.	Note 14, 20
Signal Detect - Hysteresis	P_A - P_D	1.5	2.4		dB	

Receiver Electrical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Deterministic Jitter Contributed by the Receiver	DJ_c			0.24T 0.90	 ns p-p	Note 9, 11
Random Jitter Contributed by the Receiver	RJ_C			0.26T 0.97	 ns p-p	Note 10, 11

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. When component testing these products do not short the receiver data or signal detect outputs directly to ground to avoid damage to the part.
3. The outputs are terminated with 50 Ω connected to V_{CC} - 2 V.
4. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
5. These optical power values are measured as follows:
   • The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Avago Technologies' 1300 nm LED products is < 1 dB as specified in this data sheet.
   • Over the specified operating voltage and temperature ranges.
   • With 25 MBd (12.5 MHz squarewave) input signal.
   • At the end of one meter of noted optical fiber with cladding modes removed.
   The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.
6. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a 12.5 MHz square-wave signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The extinction ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed as a percentage or in decibels.
7. This parameter complies with the requirements for the tradeoffs between center wave-length, spectral width, and rise/fall times shown in Figure 8.
8. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by a 25 MBd (12.5 MHz square-wave) input signal. This parameter complies with the requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 8.
9. Deterministic Jitter is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Deterministic Jitter is measured with a test pattern consisting of repeating K28.5 (00111110101100000101) data bytes and evaluated per the method in FC-PH Annex A.4.3.
10. Random Jitter is specified with a sequence of K28.7 (square wave of alternating 5 ones and 5 zeros) data bytes and evaluated at a Bit Error Ratio (BER) of 1 x 10-12 per the method in FC-PH Annex A.4.4.
11. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is specified to provide output data with a Bit Error Rate (BER) better than or equal to 1 x 10-12.
    • At the Beginning of Life (BOL)
    • Over the specified operating temperature and voltage ranges.
    • Input is a 266 MBd, 2E7 – 1 psuedorandom data pattern.
    • Receiver data window time-width is ± 0.94 ns or greater and centered at mid-symbol. This data window time width is calculated to simulate the effect of worst case input jitter per FC-PH Annex J and clock recovery sampling position in order to insure good operation with the various FC-0 receiver circuits.
    • The integral transmitter is operating with a 266 MBd square-wave, input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
    • The maximum total jitter added by the receiver and the maximum total jitter presented to the clock recovery circuit comply with the maximum limits listed in Annex J, but the allocations of the Rx added jitter between deterministic jitter and random jitter are different than in Annex J.
12. All conditions of Note 11 apply except that the measurement is made at the center of the symbol with no window time-width.
13. This value is measured during the transition from low to high levels of input optical power.
14. This value is measured during the transition from high to low levels of input optical power.
15. These values are measured with the outputs terminated into 50 Ω connected to V_{CC} - 2 V and an input optical power level of -14 dBm average.
16. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and supply current, minus the sum of the products of the output voltages and currents.
17. These values are measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} - 2 V.
18. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} - 2 V through 50 Ω.
19. The Signal Detect output shall be asserted within 100 μs after a step increase of the Input Optical Power.
20. Signal detect output shall be deasserted within 350 μs after a step decrease in the Input Optical Power.

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