HFBR-5805/5805T/5805A/5805AT

ATM Transceivers for SONET OC-3/SDH STM-1 in Low Cost 1 x 9 Package Style

Data Sheet



Description

The HFBR-5800 family of transceivers from Avago Technologies provide the system designer with products to implement a range of solutions for multimode fiber SONET OC-3 (SDH STM-1) physical layers for ATM and other services.

The transceivers are all supplied in the industry standard 1 x 9 SIP package style with either a duplex SC or a duplex ST* connector interface.

ATM 2 km Backbone Links

The HFBR-5805/-5805T are 1300 nm products with optical performance compliant with the SONET STS-3c (OC-3) Physical Layer Interface Specification. This physical layer is defined in the ATM Forum User-Network Interface (UNI) Specification Version 3.0. This document references the ANSI T1E1.2 specification for the details of the interface for 2 km multimode fiber backbone links.

The ATM 100 Mb/s-125 MBd Physical Layer interface is best implemented with the HFBR-5803 family of Fast Ethernet and FDDI Transceivers which are specified for use in this 4B/5B encoded physical layer per the FDDI PMD standard.

Transmitter Sections

The transmitter section of the HFBR-5803 and HFBR-5805 series utilize 1300 nm InGaAsP LEDs. These LEDs are packaged in the optical subassembly portion of the transmitter section. They are driven by a custom silicon IC which converts differential PECL logic signals, ECL referenced (shifted) to a +3.3 V or +5.0 V supply, into an analog LED drive current.

Receiver Sections

The receiver section of the HFBR-5803 and HFBR-5805 series utilize InGaAs PIN photodiodes coupled to a custom silicon transimpedance preamplifier IC. These are packaged in the optical subassembly portion of the receiver.

These PIN/preamplifier combinations are coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. The data output is dif-ferential. The signal detect output is single-ended. Both data and signal detect outputs are PECL compatible, ECL referenced (shifted) to a 3.3 V or +5.0 V power supply.

Features

- Full compliance with ATM forum UNI SONET OC-3 multimode fiber physical layer specification
- Multisourced 1 x 9 package style with choice of duplex SC or
  duplex ST* receptacle
- Wave solder and aqueous wash process compatibility
- Manufactured in an ISO 9002 certified facility
- Single +3.3 V or +5.0 V power supply

Applications

- Multimode fiber ATM backbone links
- Multimode fiber ATM wiring closet to desktop links

Ordering Information

The HFBR-5805/5805T/5805A/5805AT 1300 nm products are available for production orders through the Avago Technologies Component Field Sales Offices and Authorized Distributors world wide.

0 °C to +70 °C

HFBR-5805/5805T

-10 °C to +85 °C

HFBR-5805A/5805AT

*ST is a registered trademark of AT&T Lightguide Cable Connectors.

Note: The "T" in the product numbers indicates a transceiver with a duplex ST connector receptacle.

Product numbers without a "T" indicate transceivers with a duplex SC connector receptacle.

Package

The overall package concept for the Avago Technologies transceivers consists of three basic elements; the two optical subassemblies, an electrical subassembly and the housing as illustrated in Figure 1 and Figure 1a.

The package outline drawing and pin out are shown in Figures 2, 2a and 3. The details of this package outline and pin out are compliant with the multisource definition of the 1 x 9 SIP. The low profile of the Avago Technologies transceiver design complies with the maximum height allowed for the duplex SC connector over the entire length of the package.

The optical subassemblies utilize a high volume assembly process together with low cost lens elements which result in a cost effective building block.

The electrical subassembly consists of a high volume multilayer printed circuit board on which the IC chips and various surface-mounted passive circuit elements are attached.

The package includes internal shields for the electrical and optical subassemblies to ensure low EMI emissions and high immunity to external EMI fields.

The outer housing including the duplex SC connector or the duplex ST ports is molded of filled nonconductive plastic to provide mechanical strength and electrical isolation. The solder posts of the Avago Technologies design are isolated from the circuit design of the transceiver and do not require connection to a ground plane on the circuit board.

The transceiver is attached to a printed circuit board with the nine signal pins and the two solder posts which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with duplex or simplex SC or ST connectored fiber cables.

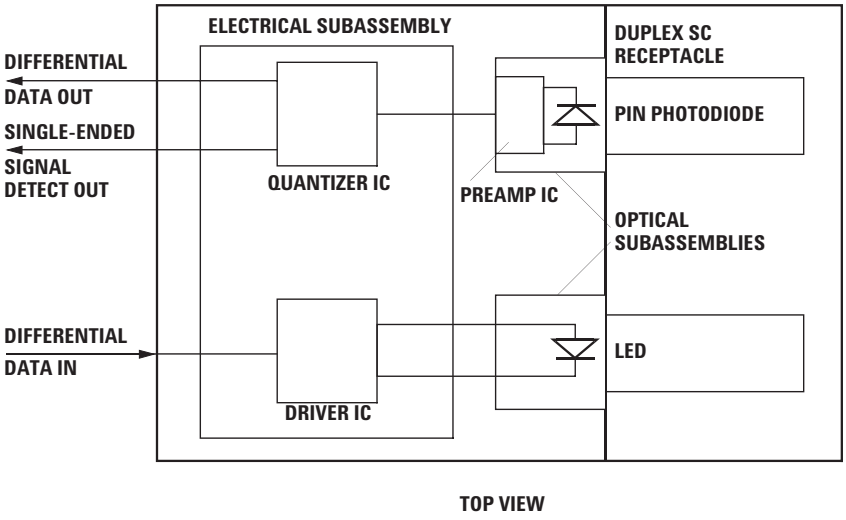


Figure 1. SC Connector Block Diagram

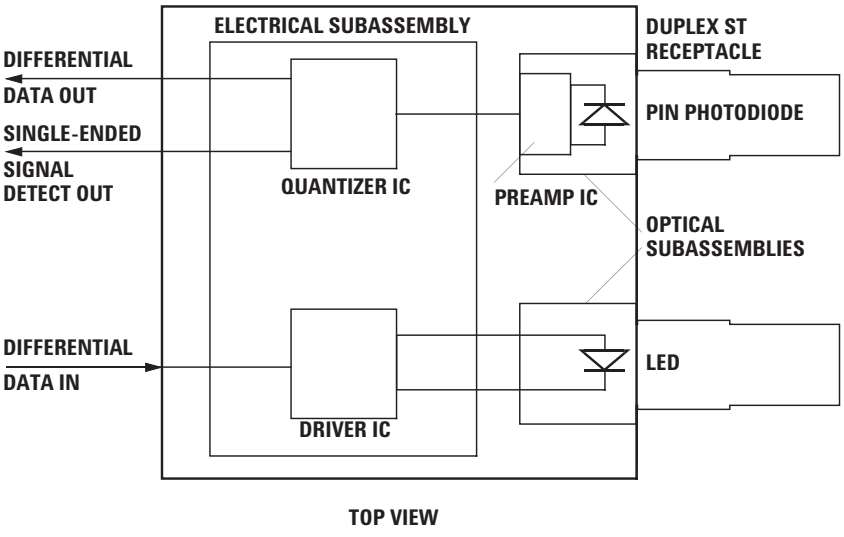
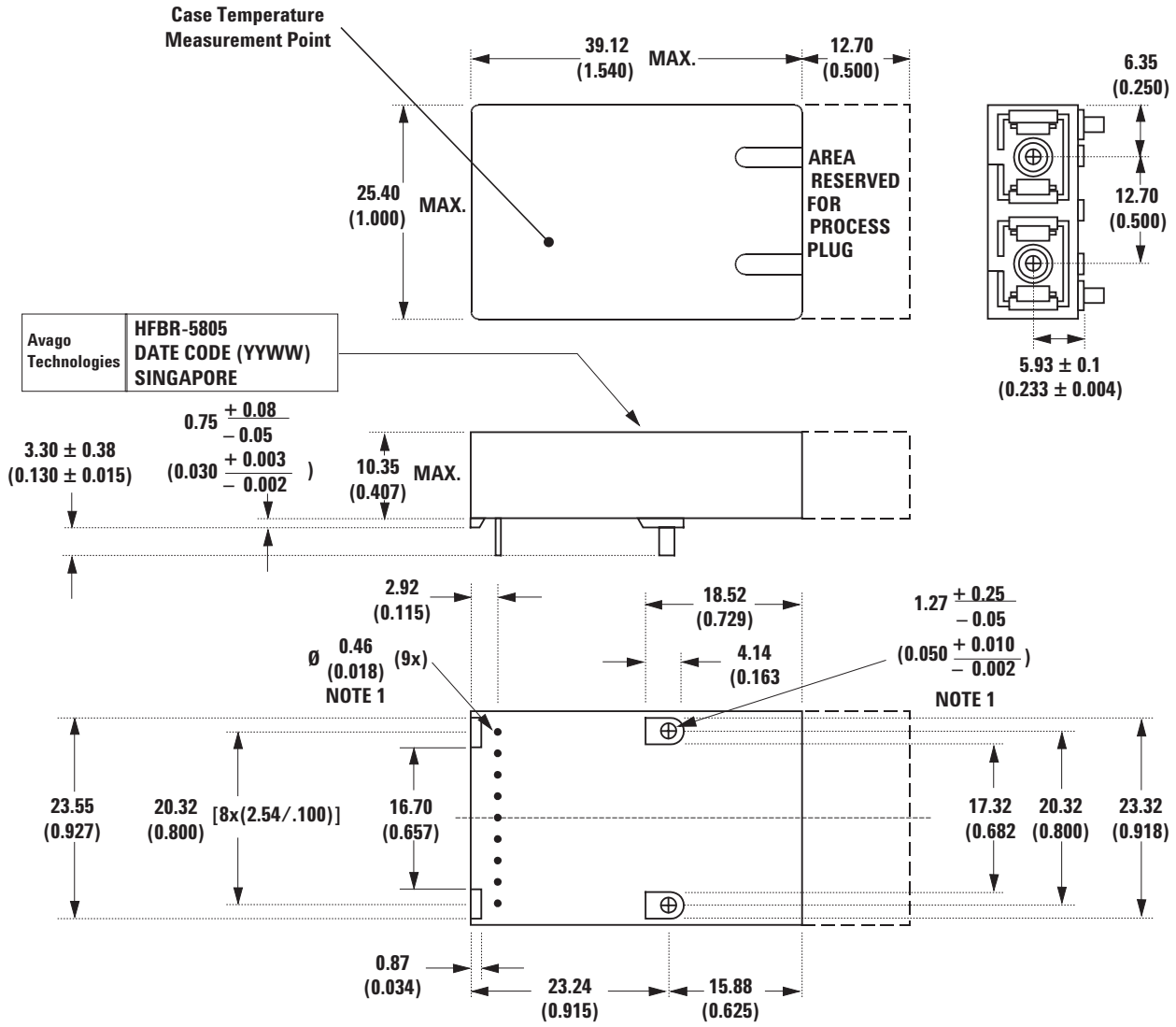


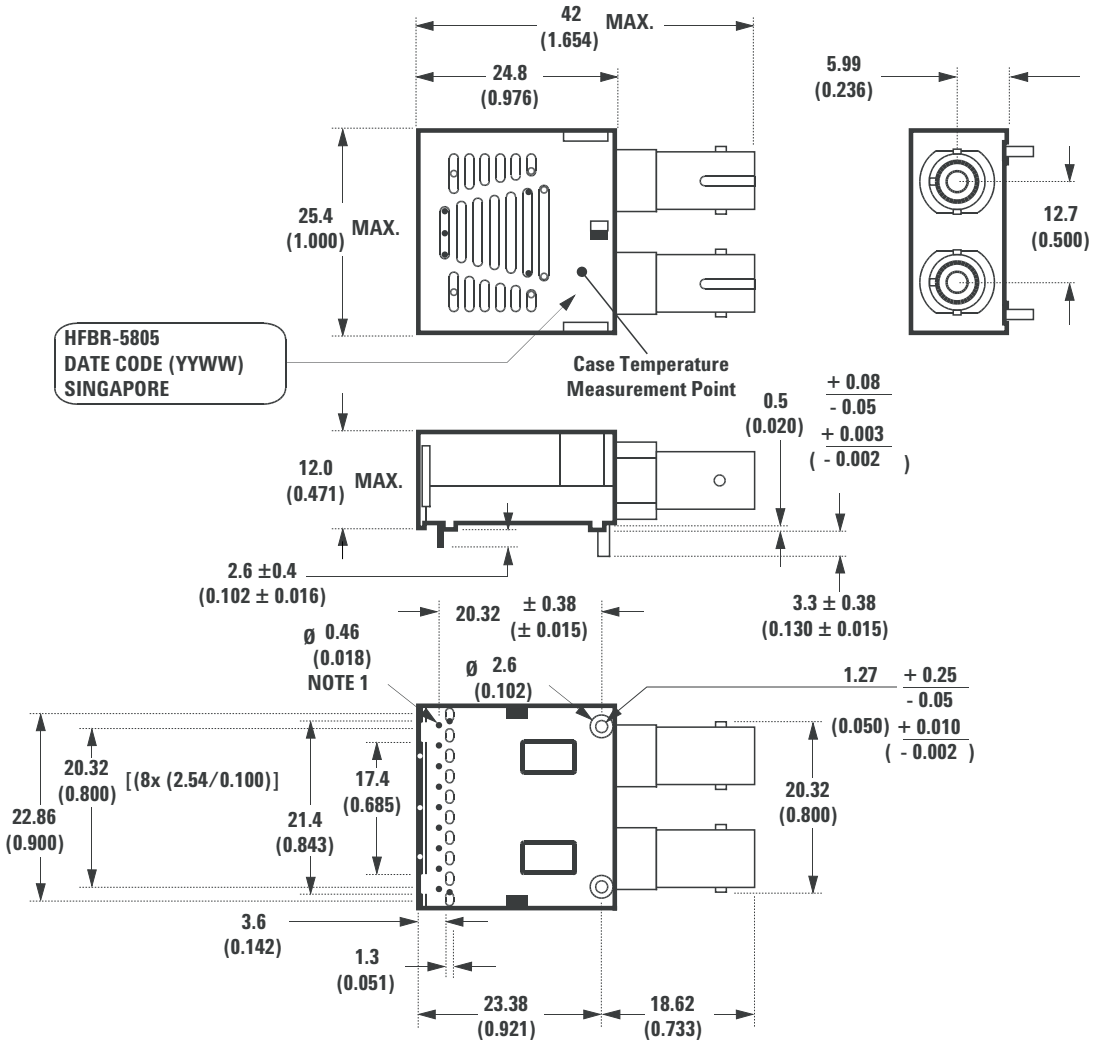
Figure 1a. ST Connector Block Diagram.



NOTE 1: THE SOLDER POSTS AND ELECTRICAL PINS ARE PHOSPHOR BRONZE WITH TIN LEAD OVER NICKEL PLATING.

DIMENSIONS ARE IN MILLIMETERS (INCHES).

Figure 2. Package Outline Drawing



Note 1: Phosphor bronze is the base material for the posts & pins. For lead-free soldering, the solder posts have Tin Copper over Nickel plating, and the electrical pins have pure Tin over Nickel plating.

DIMENSIONS IN MILLIMETERS (INCHES).

Figure 2a. ST Package Outline Drawing

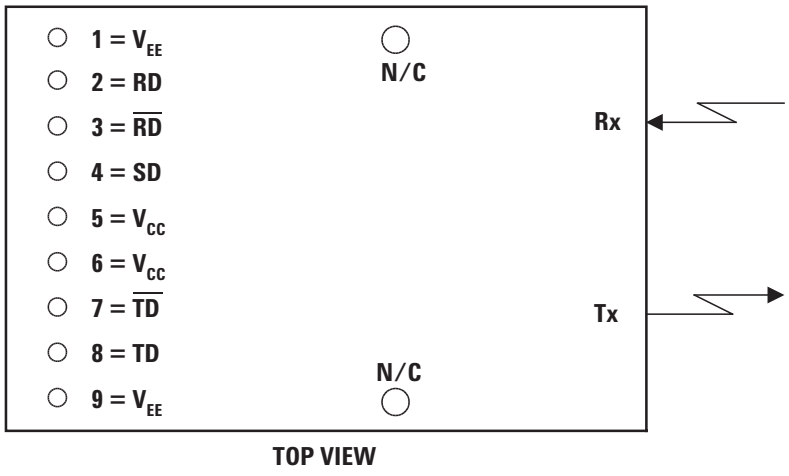


Figure 3. Pin Out Diagram.

Application Information

The Applications Engineering group in the Avago Technologies' Fiber Optics Communication Division is available to assist you with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your Avago Techologies sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 4 illustrates the predicted OPB associated with the transceiver series specified in this data sheet at the Beginning of Life (BOL). These curves represent the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125 µm and 50/125 µm fiber cables only. The area under the curves represents the remaining OPB at any link length, which is available for overcoming non-fiber cable related losses.

Avago Technologies' LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The Avago Technologies 1300 nm LEDs are specified to experience less than 1 dB of aging over normal commerical equipment mission life periods. Contact your Avago Technologies sales representative for additional details.

Figure 4 was generated for the 1300 nm transceivers with a Avago Technologies' fiber optic link model containing the current industry conventions for fiber cable specifications and the draft ANSI T1E1.2. These optical parameters are reflected in the guaranteed performance of the transceiver specifications in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI T1E1.2 committee, to establish the optical performance requirements for various fiber optic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

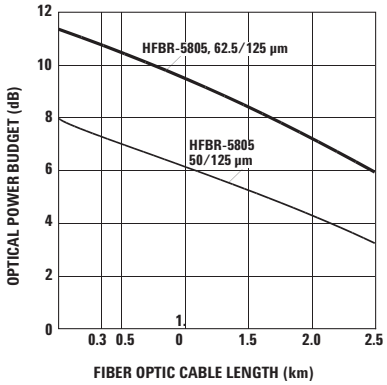


Figure 4. Optical Power Budget at BOL versus Fiber Optic Cable Length.

Transceiver Signaling Operating Rate Range and BER Performance

For purposes of definition, the symbol (Baud) rate, also called signaling rate, is the reciprocal of the symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).

When used in 155 Mb/s SONET OC-3 applications the performance of the 1300 nm transceivers, HFBR-5805 is guaranteed to the full conditions listed in product specification tables.

The transceivers may be used for other applications at signaling rates different than 155 Mb/s with some variation in the link optical power budget. Figure 5 gives an indication of the typical performance of these products at different rates.

These transceivers can also be used for applications which require different Bit Error Rate (BER) performance. Figure 6 illustrates the typical trade-off between link BER and the receivers input optical power level.

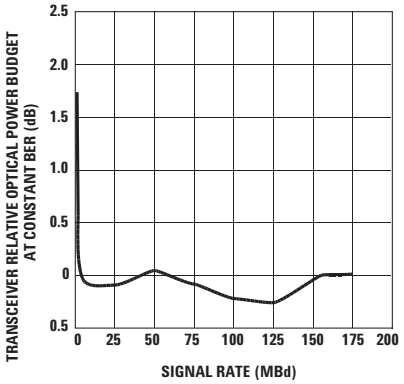
Transceiver Jitter Performance

The Avago Technologies 1300 nm transceivers are designed to operate per the system jitter allocations stated in Table B1 of Annex B of the draft ANSI T1E1.2 Revision 3 standard.

The Avago Technologies 1300 nm transmitters will tolerate the worst case input electrical jitter allowed in Annex B without violating the worst case output jitter requirements.

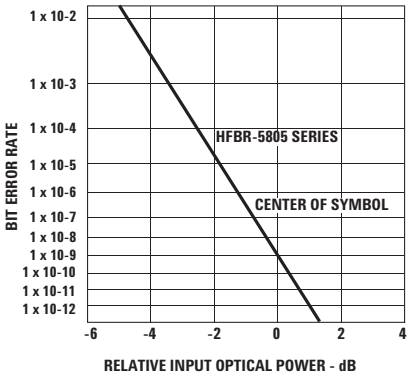
The Avago Technologies 1300 nm receivers will tolerate the worst case input optical jitter allowed in Annex B without violating the worst case output electrical jitter allowed.

The jitter specifications stated in the following 1300 nm transceiver specification tables are derived from the values in Tables B1 of Annex B. They represent the worst case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the Annex B allocation example. In practice the typical contribution of the Avago Technologies transceivers is well below these maximum allowed amounts.



CONDITIONS:
1. PRBS 2^7-1
2. DATA SAMPLED AT CENTER OF DATA SYMBOL.
3. BER = 10^{-6}
4. T_A = +25° C
5. V_{CC} = 3.3 V to 5 V dc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 5. Transceiver Relative Optical Power Budget at Constant BER vs. Signaling Rate.



CONDITIONS:
1. 155 MBd
2. PRBS 2^7-1
3. CENTER OF SYMBOL SAMPLING
4. T_A = +25°C
5. V_{CC} = 3.3 V to 5 V dc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 6. Bit Error Rate vs. Relative Receiver Input Optical Power.

Recommended Handling Precautions

Avago Technologies recommends that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The HFBR-5800 series of transceivers meet MIL-STD-883C Method 3015.4 Class 2 products.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

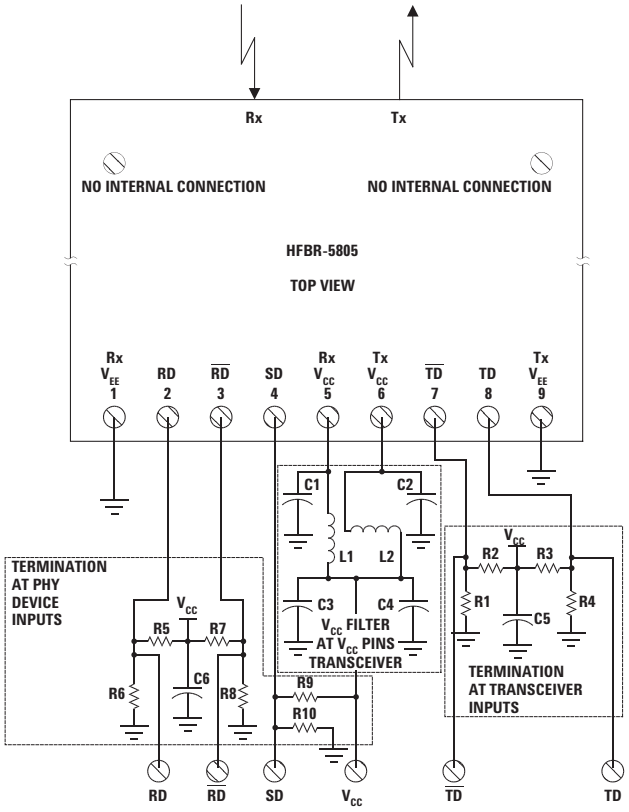
Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the duplex SC or duplex ST connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping.

These transceivers are compatible with either industry standard wave or hand solder processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR ECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE ECL SIGNALS. RECOMMEND 4-LAYER PRINTED CIRCUIT BOARD WITH 50 OHM MICROSTRIP SIGNAL PATHS BE USED.
R1 = R4 = R6 = R8 = R10 = 130 OHMS FOR +5.0 V OPERATION, 82 OHMS FOR +3.3 V OPERATION.
R2 = R3 = R5 = R7 = R9 = 82 OHMS FOR +5.0 V OPERATION, 130 OHMS FOR +3.3 V OPERATION.
C1 = C2 = C3 = C5 = C6 = 0.1 µF.
C4 = 10 µF.
L1 = L2 = 1 µH COIL OR FERRITE INDUCTOR.

Figure 7. Recommended Decoupling and Termination Circuits

Board Layout - Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 7 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.

Board Layout - Hole Pattern

The Avago Technologies transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement which defined the 1 x 9 package style. This drawing is reproduced in Figure 8 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board.

Board Layout - Art Work

The Applications Engineering group has developed Gerber file artwork for a multilayer printed circuit board layout incorporating the recommendations above. Contact your local Avago Technologies sales representative for details.

Board Layout - Mechanical

For applications interested in providing a choice of either a duplex SC or a duplex ST connector interface, while utilizing the same pinout on the printed circuit board, the ST port needs to protrude from the chassis panel a minimum of 9.53 mm for sufficient clearance to install the ST connector.

Please refer to Figure 8a for a mechanical layout detailing the recommended location of the duplex SC and duplex ST transceiver packages in relation to the chassis panel.

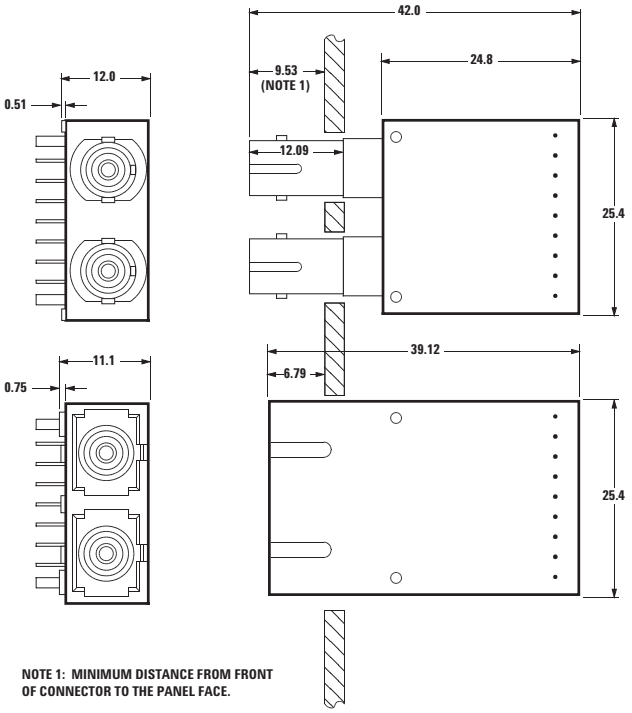


Figure 8a. Recommended Common Mechanical Layout for SC and ST 1 x 9 Connectored Transceivers.

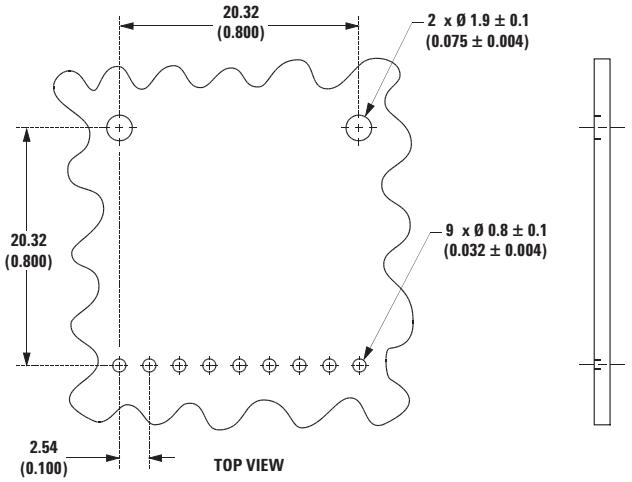


Figure 8. Recommended Board Layout Hole Pattern

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Avago Technologies sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high speed transceivers from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

These products are suitable for use in designs ranging from a desktop computer with a single transceiver to a concentrator or switch product with large number of transceivers.

In all well-designed chassis, the two 0.5" holes required for ST connectors to protrude through will provide 4.6 dB more shielding than one 1.2" duplex SC rectangular cutout. Thus, in a well-designed chassis, the duplex ST 1 x 9 transceiver emissions will be identical to the duplex SC 1 x 9 transceiver emissions.

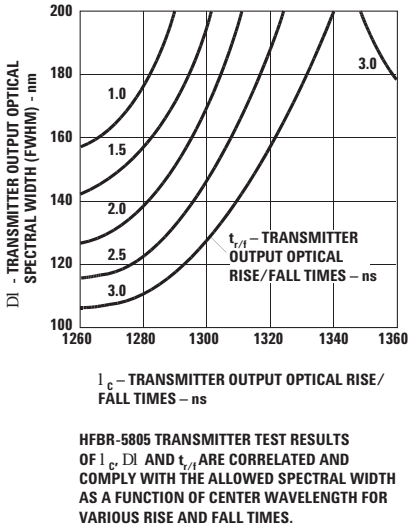


Figure 9. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Meets Class 1 (<1999 Volts). Withstand up to 1500 V applied between electrical pins.
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the Duplex SC Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 Class B (CISPR 22B) VCCI Class 2	Transceivers typically provide a 13 dB margin (with duplex SC receptacle) or a 9 dB margin (with duplex ST receptacles) to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

For additional information regarding EMI, susceptibility, ESD and conducted noise testing procedures and results on the 1 x 9 Transceiver family, please refer to Applications Note 1075, *Testing and Measuring Electromagnetic Compatibility Performance of the HFBR-510X/-520X Fiber Optic Transceivers.*

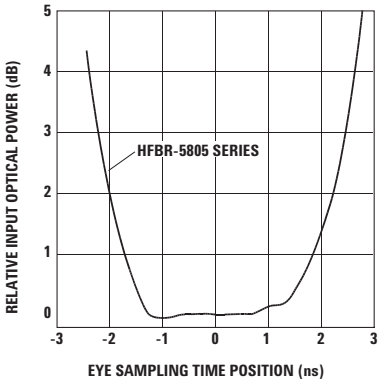
Transceiver Reliability and Performance Qualification Data

The 1 x 9 transceivers have passed Avago Technologies' reliability and performance qualification testing and are undergoing ongoing quality monitoring. Details are available from your Avago Technologies sales representative.

These transceivers are manufactured at the Avago Technologies Singapore location which is an ISO 9002 certified facility.

Ordering Information

The HFBR-5805/-5805T 1300 nm products are available for production orders through the Avago Technologies Component Field Sales Offices and Authorized Distributors world wide.



CONDITIONS:
1. T_A = +25° C
2. V_{CC} = 3.3 V to 5 V dc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 16 AND 17 APPLY.

Figure 10. Relative Input Optical Power vs. Eye Sampling Time Position.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		+100	°C	
Lead Soldering Temperature	T_{SOLD}			+260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature						
HFBR-5805/5805T	T_A	0		+70	°C	Note A
HFBR-5805A/5805AT	T_A	-10		+85	°C	Note B
Supply Voltage	V_{CC}	3.135		3.5	V	
	V_{CC}	4.75		5.25	V	
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.810		-1.475	V	
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		W	Note 2

Notes:

A. Ambient Operating Temperature corresponds to transceiver case temperature of 0°C mininum to +85 °C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 2.

B. Ambient Operating Temperature corresponds to transceiver case temperature of -10 °C mininum to +100 °C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 2.

Transmitter Electrical Characteristics

(HFBR-5805/5805T: T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V)

(HFBR-5805A/5805AT: T_A = -10°C to +85°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current		I_{CC}		135	175	mA	Note 3
Power Dissipation	at V_{CC} = 3.3 V	P_{DISS}		0.45	0.6	W	
	at V_{CC} = 5.0 V	P_{DISS}		0.67	0.9	W	
Data Input Current - Low		I_{IL}	-350	-2		µA	
Data Input Current - High		I_{IH}		18	350	µA	

Receiver Electrical Characteristics

(HFBR-5805/5805T: T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V)

(HFBR-5805A/5805AT: T_A = -10°C to +85°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V

Parameter		Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current		I_{CC}		87	120	mA	Note 4
Power Dissipation	at V_{CC} = 3.3 V	P_{DISS}		0.15	0.25	W	Note 5
	at V_{CC} = 5.0 V	P_{DISS}		0.3	0.45	W	
Data Output Voltage - Low		V_{OL} - V_{CC}	-1.840		-1.620	V	Note 6
Data Output Voltage - High		V_{OH} - V_{CC}	-1.045		-0.880	V	Note 6
Data Output Rise Time		t_r	0.35		2.2	ns	Note 7
Data Output Fall Time		t_f	0.35		2.2	ns	Note 7
Signal Detect Output Voltage - Low		V_{OL} - V_{CC}	-1.840		-1.620	V	Note 6
Signal Detect Output Voltage - High		V_{OH} - V_{CC}	-1.045		-0.880	V	Note 6
Signal Detect Output Rise Time		t_r	0.35		2.2	ns	Note 7
Signal Detect Output Fall Time		t_f	0.35		2.2	ns	Note 7

Transmitter Optical Characteristics

(HFBR-5805/5805T: T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V)

(HFBR-5805A/5805AT: T_A = -10°C to +85°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	BOL EOL	P_O	-19 -20		-14	dBm avg.	Note 8
Output Optical Power 50/125 µm, NA = 0.20 Fiber	BOL EOL	P_O	-22.5 -23.5		-14	dBm avg.	Note 8
Optical Extinction Ratio				0.05	0.2	%	Note 9
Output Optical Power at Logic "0" State		P_O ("0")			-45	dBm avg.	Note 10
Center Wavelength		l_C	1270	1310	1380	nm	Note 22
Spectral Width - FWHM		Dl		137		nm	Note 22
Optical Rise Time		t_r	0.6	1.9	3.0	ns	Note 11, 22 Figure 9
Optical Fall Time		t_f	0.6	1.6	3.0	ns	Note 11, 22 Figure 9
Systematic Jitter Contributed by the Transmitter		SJ			1.2	ns p-p	Note 12
Random Jitter Contributed by the Transmitter		RJ			0.69	ns p-p	Note 13

Receiver Optical and Electrical Characteristics

(HFBR-5805/5805T: T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V)

(HFBR-5805A/5805AT: T_A = -10°C to +85°C, V_{CC} = 3.135 V to 3.5 V or 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min.}$ (W)		-34	-30	dBm avg.	Note 14 Figure 10
Input Optical Power Minimum at Eye Center	$P_{IN\ Min.}$ (C)		-35	-31	dBm avg.	Note 15 Figure 10
Input Optical Power Maximum	$P_{IN\ Max.}$	-14			dBm avg.	Note 14
Operating Wavelength	l	1270		1380	nm	
Systematic Jitter Contributed by the Receiver	SJ			1.2	ns p-p	Note 16
Random Jitter Contributed by the Receiver	RJ			1.91	ns p-p	Note 17
Signal Detect - Asserted	P_A	P_D +1.5 dB		-31	dBm avg.	Note 18
Signal Detect - Deasserted	P_D	-45			dBm avg.	Note 19
Signal Detect - Hysteresis	P_A - P_D	1.5			dB	
Signal Detect Assert Time (off to on)		0	2	100	µs	Note 20
Signal Detect Deassert Time (on to off)		0	8	350	µs	Note 21

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to V_{CC} -2 V.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This value is measured with the outputs terminated into 50 W connected to V_{CC} - 2 V and an Input Optical Power level of -14 dBm average.
5. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
6. This value is measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} - 2 V.
7. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} -2 V through 50 Ω.
8. These optical power values are measured with the following conditions:
   - The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Avago Technologies' 1300 nm LED products is < 1 dB, as specified in this data sheet.
   - Over the specified operating voltage and temperature ranges.
   - With 25 MBd (12.5 MHz square-wave), input signal.
   - At the end of one meter of noted optical fiber with cladding modes removed.

   The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.
9. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a 25 MBd (12.5 MHz square-wave) input signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The extinction ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed as a percentage or in decibels.
10. The transmitter will provide this low level of Output Optical Power when driven by a logic "0" input. This can be useful in link troubleshooting.
11. The relationship between Full Width Half Maximum and RMS values for Spectral Width is derived from the assumption of a Gaussian shaped spectrum which results in a 2.35 X RMS = FWHM relationship. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by a 25 MBd (12.5 MHz square-wave) input signal. The ANSI T1E1.2 committee has designated the possibility of defining an eye pattern mask for the transmitter optical output as an item for further study. Avago Technologies will incorporate this requirement into the specifications for these products if it is defined. The HFBR-5805 products typically comply with the template requirements of CCITT (now ITU-T) G.957 Section 3.2.5, Figure 2 for the STM-1 rate, excluding the optical receiver filter normally associated with single mode fiber measurements which is the likely source for the ANSI T1E1.2 committee to follow in this matter.
12. Systematic Jitter contributed by the transmitter is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Systematic Jitter is measured at 50% threshold using a 155.52 MBd (77.5 MHz square-wave), 2^7 -1 psuedo random data pattern input signal.
13. Random Jitter contributed by the transmitter is specified with a 155.52 MBd (77.5 MHz square-wave) input signal.
14. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 1 x 10^{-10}.
   - At the Beginning of Life (BOL)
   - Over the specified operating temperature and voltage ranges
   - Input is a 155.52 MBd, 2^{23} - 1 PRBS data pattern with 72 "1"s and 72 "0"s inserted per the CCITT (now ITU-T) recommendation G.958 Appendix I.
   - Receiver data window time-width is 1.23 ns or greater for the clock recovery circuit to operate in. The actual test data window time-width is set to simulate the effect of worst case optical input jitter based on the transmitter jitter values from the specification tables. The test window time-width is HFBR-5805 3.32 ns.
   - Transmitter operating with a 155.52 MBd, 77.5 MHz square-wave, input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
15. All conditions of Note 14 apply except that the measurement is made at the center of the symbol with no window time-width.
16. Systematic Jitter contributed by the receiver is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Systematic Jitter is measured at 50% threshold using a 155.52 MBd (77.5 MHz square-wave), 2^7 - 1 psuedo random data pattern input signal.
17. Random Jitter contributed by the receiver is specified with a 155.52 MBd (77.5 MHz square-wave) input signal.
18. This value is measured during the transition from low to high levels of input optical power.
19. This value is measured during the transition from high to low levels of input optical power.
20. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power.
21. Signal detect output shall be de-asserted within 350 µs after a step decrease in the Input Optical Power.
22. The HFBR-5805 transceiver complies with the requirements for the trade-offs between center wavelength, spectral width, and rise/fall times shown in Figure 9. This figure is derived from the FDDI PMD standard (ISO/IEC 9314-3 : 1990 and ANSI X3.166 - 1990) per the description in ANSI T1E1.2 Revision 3. The interpretation of this figure is that values of Center Wavelength and Spectral Width must lie along the appropriate Optical Rise/Fall Time curve.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies, Pte. in the United States and other countries.
Data subject to change. Copyright © 2006 Avago Technologies Pte. All rights reserved.
5989-3435EN - April 28, 2006

AVAGO
TECHNOLOGIES