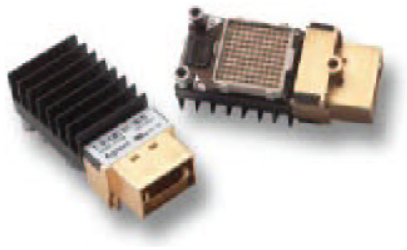
HFBR-7924WZ

Four-Channel Pluggable Parallel Fiber Optic Transceiver

Part of the Avago Technologies METRAK family

Data Sheet



Description

The HFBR-7924WZ transceiver is a high performance fiber optic module for parallel optical data communication applications. It incorporates 8 independent data channels (4 for transmit and 4 for receive) operating from 1 to 2.7 Gb/s per channel providing a cost effective solution for very short reach applications requiring 10.8 Gb/s aggregate bandwidth. The module is designed to operate on multimode fiber systems at a nominal wavelength of 850 nm. It incorporates high performance, highly reliable, short wavelength optical devices coupled with proven circuit technology to provide long life and consistent service.

The HFBR-7924WZ transceiver module incorporates a 4 channel VCSEL (Vertical Cavity Surface Emitting Laser) array together with a custom 4 channel laser driver integrated circuit providing IEC-825 and CDRH Class 1M laser eye safety. It also contains a 4 channel PIN photodiode array coupled with a custom preamplifier / post amplifier integrated circuit.

Operating on 3.3 V power supply this module provides LVTTL/LVCMOS control interfaces and CML compatible high speed data lines which simplify external circuitry. The transceiver is housed in MTP®/MPO receptacled package with integral finned heatsink. Electrical connections to the device are achieved by means of a pluggable 10x10 connector array.

Applications

- Telecom and Datacom Switch/Router Rack-to-Rack Connections
- OC-192 Very Short Reach (VSR), OIF-VSR4-03.0, Interconnects
- Computer Cluster Interconnects

Features

- RoHS Compliant
- Four Transmit and Four Receive Channels; 1 to 2.7 GBd per channel
- Compatible with SONET scrambled and 8B10B encoded data formats
- 850 nm VCSEL array source
- Conforms to "POP4" Four-Channel Pluggable Optical Transceiver Multisource Agreement
- 50/125 µm multimode fiber operation
  - Distance up to 300 m with 500 MHz.km fiber at 2.5 Gb/s
  - Distance up to 600 m with 2000 MHz.km fiber at 2.5 Gb/s
- Pluggable package
- Outputs (Tx & Rx) are squelched for loss of signal
- Control I/O is compatible with LVTTL and LVCMOS
- Standard MTP® MPO ribbon fiber connector interface
- Integrated heat sink
- Manufactured in an ISO 9002 certified facility
- Rx Signal Detect

Ordering Information

The HFBR-7924WZ product is available for production orders through the Avago Technologies Component Field Sales Office.

HFBR-7924WZ	No EMI Nose Shield
HFBR-7924EWZ	With Extended EMI Nose Shield
HFBR-7924HWZ	No heatsink, No EMI Nose Shield
HFBR-7924EHWZ	No heatsink, with EMI Nose Shield

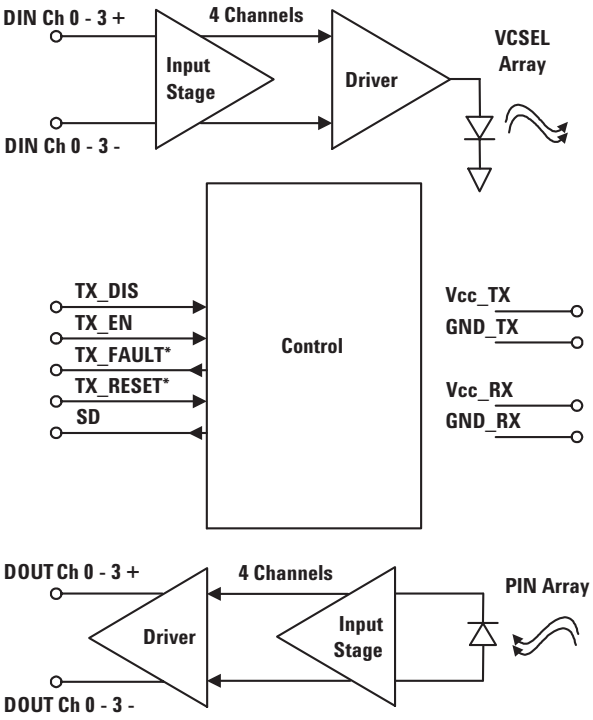


Figure 1 - Block Diagram (dimensions in mm)

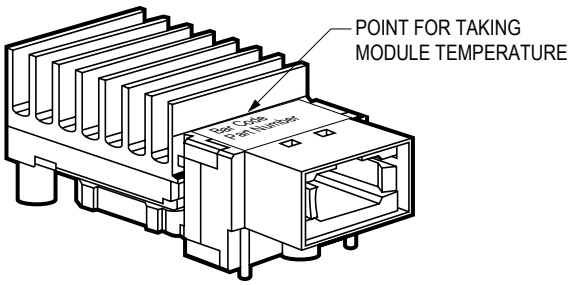


Figure 2 - Case temperature measurement

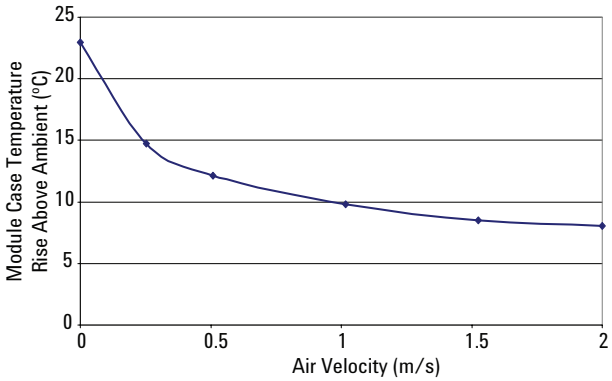
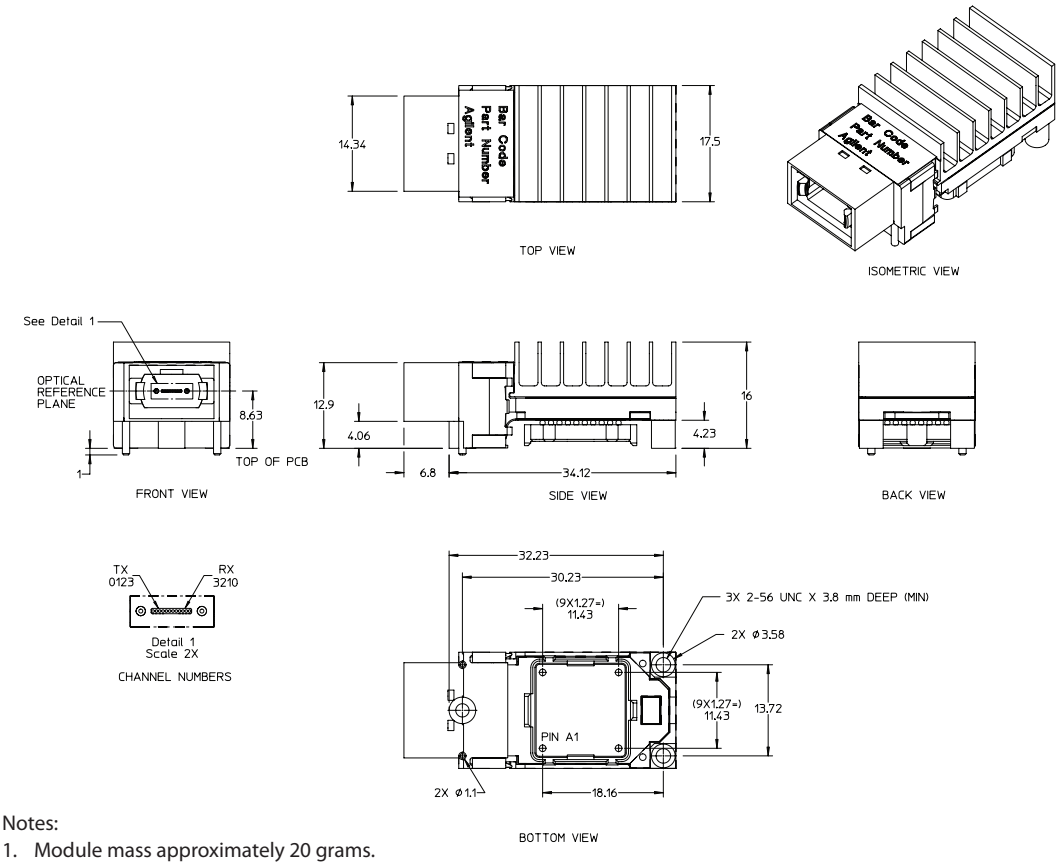


Figure 3 - Ambient air temperature and air flow for T_C = +80 °C

Package Dimensions



Notes:

1. Module mass approximately 20 grams.

Figure 4A - HFBR-7924WZ Package dimensions (dimensions in mm)

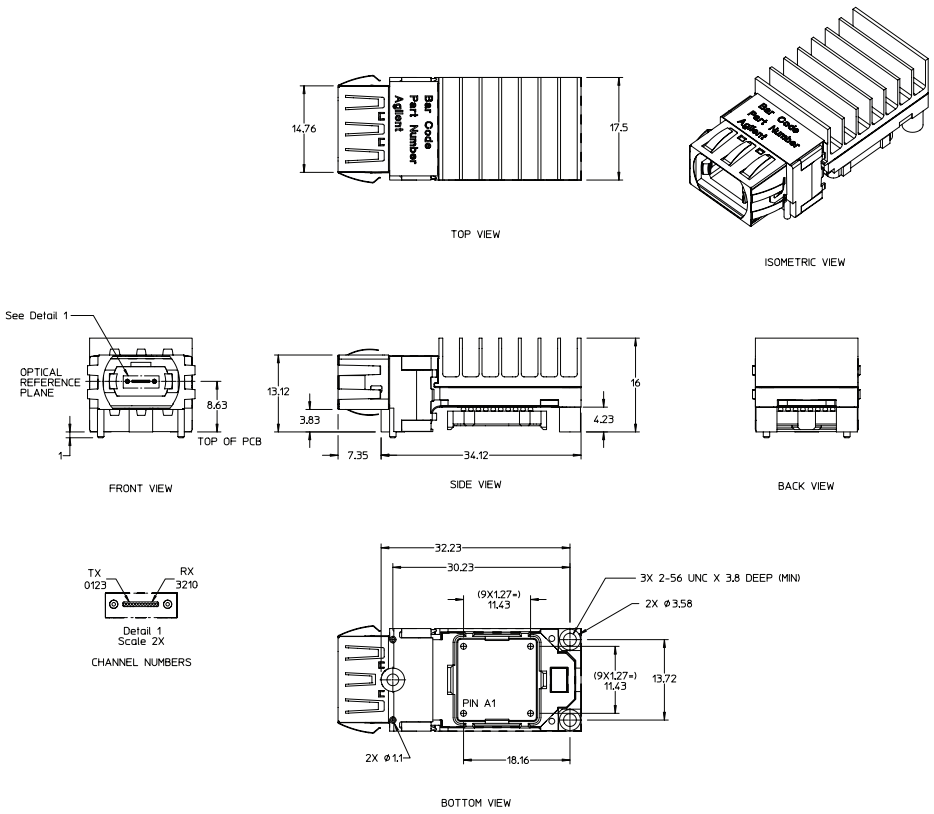


Figure 4B - HFBZ-7492EWZ Package dimensions (dimensions in mm)

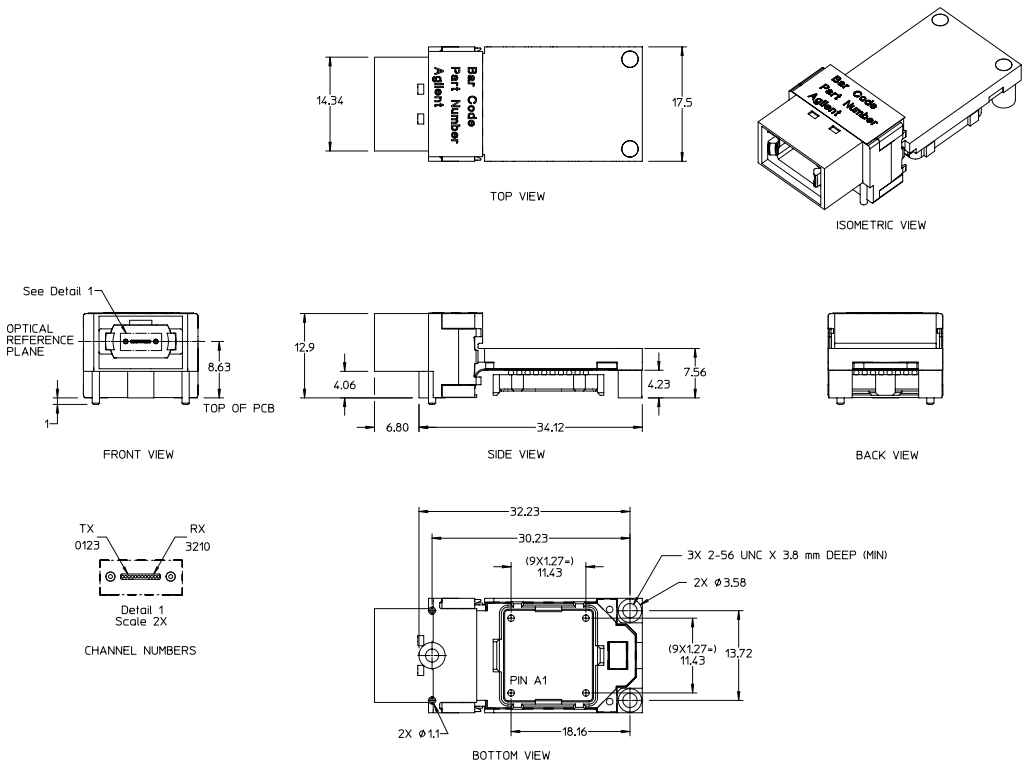


Figure 5A - HFBZ-7492HWZ Package Dimensions (dimensions in mm)

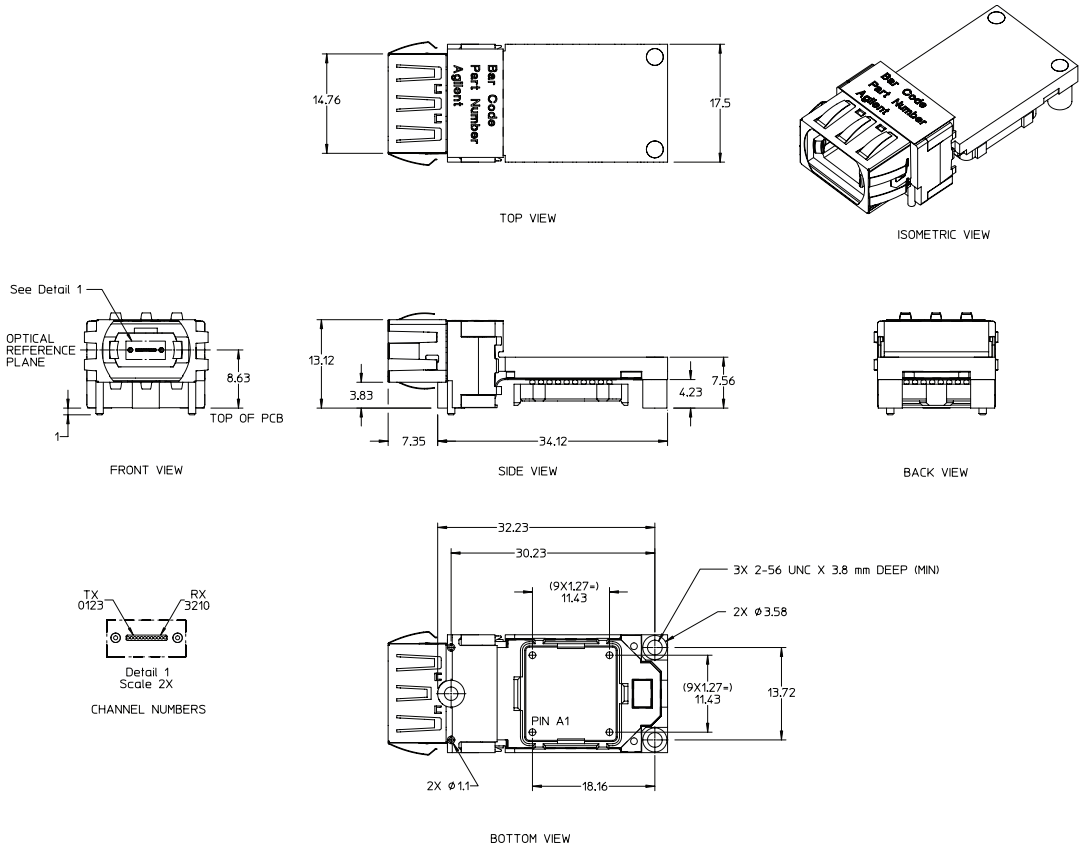
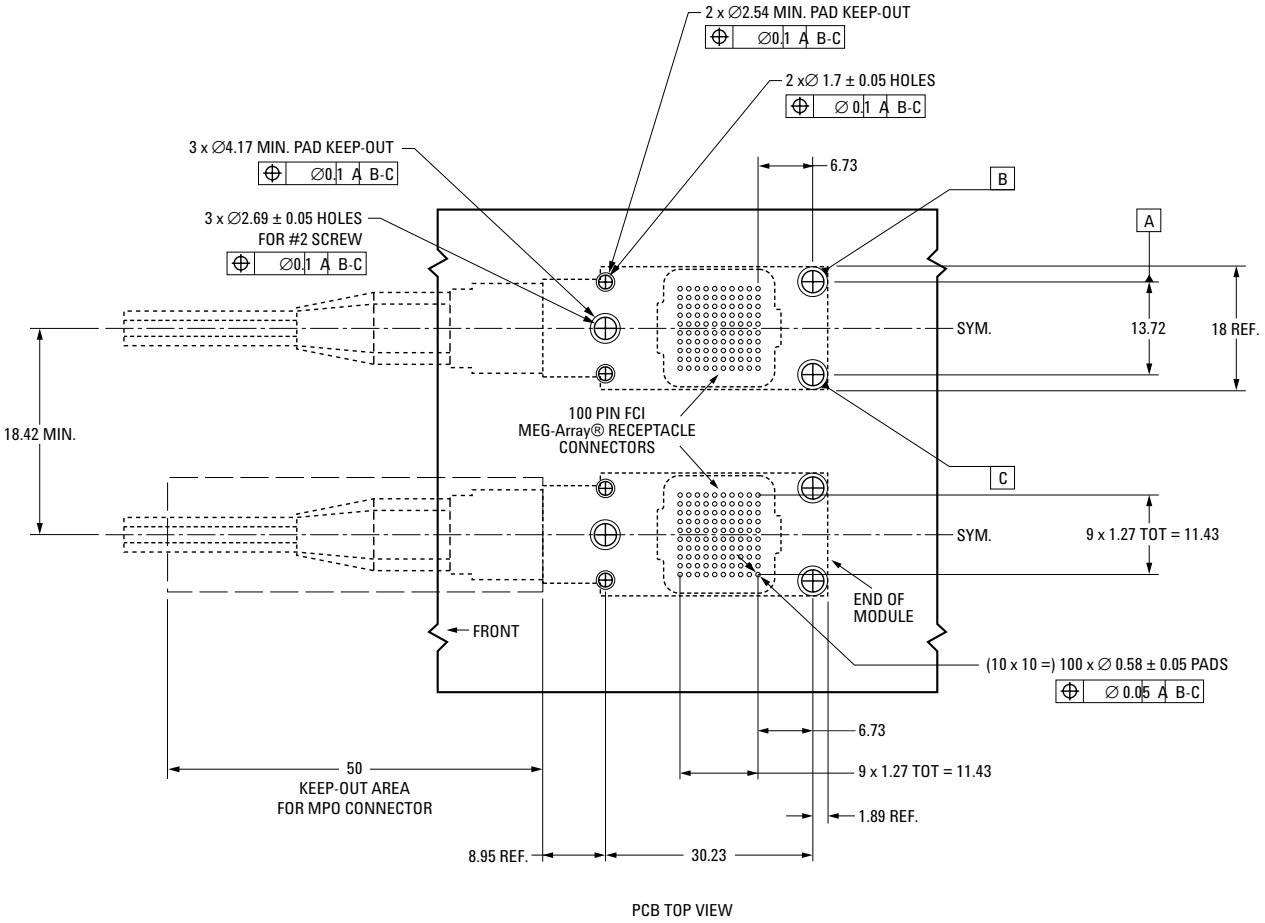


Figure 5B - HFBZ-7492EHWZ Package Dimensions (dimensions in mm)



PCB TOP VIEW

NOTE: The host electrical connector attached to the PCB must be a 100-position FCI Meg-Array® Pao-Ann to provide changes or equiva-

Figure 6 - Package Board Footprint (dimensions in mm)

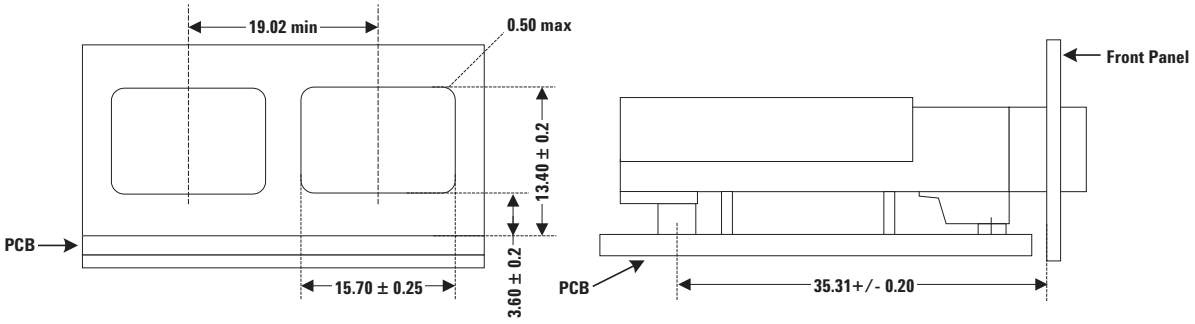


Figure 7 - Host Frontplate Layout (dimensions in mm)

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit	Reference
Storage Temperature	T_S	-40	+100	°C	
Supply Voltage	V_{CC}	-0.5	4.6	V	
Data/Control Signal Input Voltage	V_I	-0.5	V_{CC} + 0.5	V	
Transmitter Differential Input Voltage	$\lvert V_D \rvert$		2	V	1
Output Current (dc)	I_D		25	mA	
Relative Humidity (Non Condensing)	RH	5	95	%	

Recommended Operating Conditions

Recommended Operating Conditions specify conditions for which the optical and electrical characteristics hold. Optical and electrical characteristics are not specified for operation beyond the Recommended Operating Conditions, reliability is not implied and damage to the device may occur for such operation over an extended time period.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Case Temperature	T_C	0		+80	°C	2, Figures 2,
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	Figure 8
Signaling Rate/Channel		1		2.7	GBd	
Data Input Differential Peak-to-PeakVoltage Swing	ΔV_{DINP-P}	175		1600	mV_{P-P}	3, Figures 11,12
Data Input Rise & Fall Time (20-80%)	t_r, t_f			160	ps	
Control Input Voltage High	V_{IH}	2.0		V_{CC}	V	
Control Input Voltage Low	V_{IL}	V_{EE}		0.8	V	
Power Supply Noise	N_P			200	mV_{P-P}	4, Figure 8
Data I/O Coupling Capacitors	C_{AC}		0.1		µF	5, Figure 9
Receiver Differential Data Output Load	R_{DL}		100		Ω	Figure 9

Notes:

1. This is the maximum voltage that can be applied across the Transmitter Differential Data Inputs without damaging the input circuit.
2. Case Temperature is measured as indicated in Figure 2.
3. Data inputs are CML compatible. Coupling capacitors are required to block dc. $\Delta V_{DIN\ p-p} = \Delta V_{DINH} - \Delta V_{DINL}$, where ΔV_{DINH} = High State Differential Data Input Voltage and ΔV_{DINL} = Low State Differential Data Input Voltage.
4. Power Supply Noise is defined at the supply side of the recommended filter for all V_{CC} supplies over the frequency range from 500 Hz to 2700 MHz with the recommended power supply filter in place.
5. For data patterns with restricted run lengths, e.g. 8B10B encoded data, smaller value capacitors may provide acceptable results.

Transmitter Electrical Characteristics

(Over recommended operating conditions: Tc= 0°C to +80°C, Vcc=3.3V ± 5%)

Parameter		Symbol	Minimum	Typical	Maximum	Unit	Reference
Differential Input Impedance		Z_{in}	80	100	120	Ω	6, Figure 9
FAULT* Assert time		T_{OFF}			100	µs	Figure 13
RESET* Assert time		T_{OFF}			7.5	µs	Figure 14
RESET* De-assert time		T_{ON}			18	ms	Figure 14
Transmit Enable (TX_EN) Assert time		T_{ON}			18	ms	Figure 15
Transmit Enable (TX_EN) De-assert time		T_{OFF}			7.5	µs	Figure 15
Transmit Disable (TX_DIS) Assert time		T_{OFF}			7.5	µs	Figure 15
Transmit Disable (TX_DIS) De-assert time		T_{ON}			18	ms	Figure 15
Power-On Initiation Time				21		ms	Figure 17
Control I/Os TX _DIS, TX_EN,TX_ FAULT*,TX_RESET*	Input Current High	$\lvert I_{IH} \rvert$			0.5	mA	$2.0\ V \leq V_{IH} \leq V_{CC}$
	Input Current Low	$\lvert I_{IL} \rvert$			0.5	mA	$V_{EE} \leq V_{IH} \leq 0.8\ V$
	Output Voltage Low	V_{OL}	V_{EE}		0.4	V	I_{OL} = 4.0 mA
	Output Voltage High	V_{OH}	2.4		V_{CC}	V	I_{OH} = -0.5 mA

Transmitter Optical Characteristics

(Over recommended operating conditions: Tc= 0°C to +80°C, Vcc=3.3V ± 5%)

Parameter		Symbol	Minimum	Typical	Maximum	Unit	Reference
Output Optical Power 50/125 µm, Fiber NA = 0.2		P_{OUT}	-8.0	-4.5	-2.0	dBm avg.	7
Extinction Ratio		ER	6	7.5		dB	8
Center Wavelength		λ_C	830	850	860	nm	
Spectral Width - rms		σ			0.85	nm rms	
Rise, Fall Time		t_r, t_f		60	150	ps	9
Inter-channel Skew				50	100	ps	10
Relative Intensity Noise		RIN		-127	-121	dB/Hz	
Jitter Contribution	Deterministic	DJ		20	50	ps_{p-p}	11
	Total	TJ		45	120	ps_{p-p}	12

Notes:

6. Differential impedance is measured between D_{IN}+ and D_{IN}- over the range 4 MHz to 2 GHz.
7. The specified optical output power, measured at the output of a 2 meter test cable, will be compliant with IEC 60825-1 Amendment 2, Class 1M Accessible Emission Limits, AEL Regulatory Compliance section.
8. Extinction Ratio is defined as the ratio of the average output optical power of the transmitter in the high ("1") state to the low ("0") state and is expressed in decibels (dB) by the relationship $10\log(P_{high}\ avg/P_{low}\ avg)$. The transmitter is driven with a 550 MBd, 101010 pattern.
9. These are unfiltered 20% - 80% values measured with a 550 MBd 101010 pattern.
10. Inter-channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.
11. Deterministic Jitter (DJ) is defined as the combination of Duty Cycle Distortion (Pulse-Width Distortion) and Data Dependent Jitter. Deterministic Jitter is measured at the 50% signal threshold level using a 2500 MBd Pseudo Random Bit Sequence of length 2^{23}-1 (PRBS-23), or equivalent, test pattern with zero skew between the differential data input signals.
12. Total Jitter (TJ) includes Deterministic Jitter and Random Jitter (RJ). Total Jitter is specified at a BER of 10^{-12} for the same 2.5 GBd test pattern as for DJ and is measured with all channels operating.

Receiver Electrical Characteristics

(Over recommended operating conditions: Tc= 0°C to +80°C, Vcc=3.3V ± 5%)

Parameter		Symbol	Minimum	Typical	Maximum	Unit	Reference
Differential Output Impedance		Z_{OUT}		100		Ω	13, Figure 9
Data Output Differential Peak-to-Peak Voltage Swing		$\Delta V_{DOUTP-P}$	500	650	800	mV_{P-P}	14, Figure 10
Inter-channel Skew				50	100	ps	15
Data Output Rise, Fall Time		t_r, t_f		120	150	ps	16
Control I/O Signal Detect LVTTL & LVCMOS Compatible	Output Voltage Low	V_{OL}	V_{EE}		0.4	V	I_{OL} = 4.0 mA
	Output Voltage High	V_{OH}	2.4		V_{CC}	V	I_{OH} = -0.5 mA
	Assert Time (OFF-to-ON)	t_{SDA}		50		µs	17
	De-assert Time (ON-to-OFF)	t_{SDD}		50		µs	18

Receiver Optical Characteristics

(Over recommended operating conditions: Tc= 0°C to +80°C, Vcc=3.3V ± 5%)

Parameter		Symbol	Minimum	Typical	Maximum	Unit	Reference
Input Optical Power - Sensitivity		$P_{IN\ MIN}$		-18	-16.0	dBm avg.	19
Input Optical Power - Saturation		$P_{IN\ MAX}$	-2.0			dBm avg.	
Operating Center Wavelength		λ_C	830		860	nm	
Stressed Receiver Sensitivity					-11.7	dBm	20
Stressed Receiver Eye Opening			111			ps	21
Return Loss			12			dB	22
Signal Detect	Asserted	P_A		-22	-17	dBm avg.	23
	Deasserted	P_D	-31	-27		dBm avg.	
	Hysteresis	$P_A - P_D$	0.5	1.0		dB	

Notes:

13. Measured over the range 4 MHz to 2 GHz.
14. $\Delta V_{DoutP-P} = \Delta V_{DoutH} - \Delta V_{DoutL}$, where ΔV_{DoutH} = High State Differential Data Output Voltage and ΔV_{DoutL} = Low State Differential Data Output Voltage. ΔV_{DoutH} and $\Delta V_{DoutL} = V_{Dout+} - V_{Dout-}$, measured with a 100 Ω differential load connected with the recommended coupling capacitors and with a 2500 MBd, 101010 pattern.
15. Inter-channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.
16. Rise and Fall Times are measured between the 20% and 80% levels using a 550 MHd square wave signal.
17. The Signal Detect output will change from logic "0" (Low) to "1" (High) within the specified assert time for a step transition in optical input power from the deasserted condition to the specified asserted optical power level.
18. The Signal Detect output will change from logic "1" (High) to "0" (Low) within the specified de-assert time for a step transition in optical input power from the specified asserted optical power level to the deasserted condition.
19. Sensitivity is defined as the average input power with the worst case, minimum, Extinction Ratio necessary to produce a BER $\leq 10^{-12}$ at the center of the Baud interval. For this parameter, input power is equivalent to that provided by an ideal source, i.e. one with RIN and switching attributes that do not degrade the sensitivity measurement. All channels not under test are operating receiving data with an average input power of up to 6 dB above $P_{IN\ MIN}$. Sensitivity at signal rates from 1 to 2.7 GBd is defined for a PRBS 2^{23}-1 test pattern.
20. The stressed receiver sensitivity is measured using 2.6 dB Inter-Symbol Interference, ISI, (min), 30 ps Duty Cycle Dependent Deterministic Jitter, DCD DJ (min) and 6 dB ER (ER Penalty = 2.23 dB). All channels not under test are operating receiving data with an average input power of up to 6 dB, above $P_{IN\ MIN}$.
21. The stressed receiver eye opening is measured using 2.6 dB ISI (min), 30 ps DCD DJ (min), 6 dB ER (ER Penalty = 2.23 dB) and an average input optical power of -11.7 dBm. All channels not under test are operating receiving data with an average input power of up to 6 dB above $P_{IN\ MIN}$.
22. Return loss is defined as the ratio, in dB, of the received optical power to the optical power reflected back down the fiber.
23. Signal Detect assertion requires all optical inputs to exhibit a minimum 6 dB Extinction Ratio at P_A = -17 dBm. All channels not under test are operating with PRBS 2^{23}-1patterns, asynchronous with the channel under test, and average input power of up to 6 dB above the specified $P_{IN\ MIN}$.

General/Control Electrical Characteristics

(Over recommended operating conditions: Tc= 0ºC to +80ºC, Vcc=3.3V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CCT}		300	400	mA	
Power Dissipation	P_{DIST}		1.0	1.39	W	

Regulatory Compliance

The overall equipment design will determine the certification level. The module performance is offered as a figure of merit to assist the designer in considering their use in equipment designs.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the module prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, workbenches and floor mats in ESD controlled areas. The module performance has been shown to provide adequate performance in typical industry production environments.

The second case to consider is static discharges to the exterior of the equipment chassis containing the module parts. To the extent that the MT-based connector receptacle is exposed to the outside of the equipment chassis it may be subject to whatever system-level ESD test criteria that the equipment is intended to meet. The module performance exceeds typical industry equipment requirements of today.

Electromagnetic Interference (EMI)

Most equipment designs using these high-speed modules from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. These modules, with their shielded design, perform to the limits listed in Table 1 to assist the designer in the management of the overall equipment EMI performance.

Immunity

Equipment utilizing these modules will be subject to radio frequency electromagnetic fields in some environments. These modules have good immunity to such fields due to their shielded design.

Eye Safety

These 850 nm VCSEL-based transceiver modules provide eye safety by design.

The HFBR-7924WZ has been registered with CDRH and certified by TUV as a Class 1M device under Amendment 2 of IEC 60825-1. See the Regulatory Compliannce Table for further detail. If Class 1M exposure is possible, a safety-warning label should be placed on the product stating the following:

LASER RADIATION
DO NOT VIEW DIRECTLY WITH OPTICAL INSTRUMENTS.
CLASS 1M LASER PRODUCT

MTP®(MPO) Optics Cleaning Statement

The optical port has recessed optics that are visible through the nose of the port. The port plug provided should be installed whenever a fiber cable is not connected. This ensures the optics remain clean and no cleaning should be necessary. In the event of the optics being contaminated, forced nitrogen or dry clean air at less than 20 psi is the recommended cleaning agent. The features of the optical port and guide pins preclude the use of any solid instrument. Liquids are not advised due to potential damage.

Application of wave soldering, reflow soldering and/or aqueous wash processes with the HFBR-7924WZ modules device on board is not recommended as damage may occur.

Normal handling precautions for electrostatic sensitive devices should be taken (see ESD section).

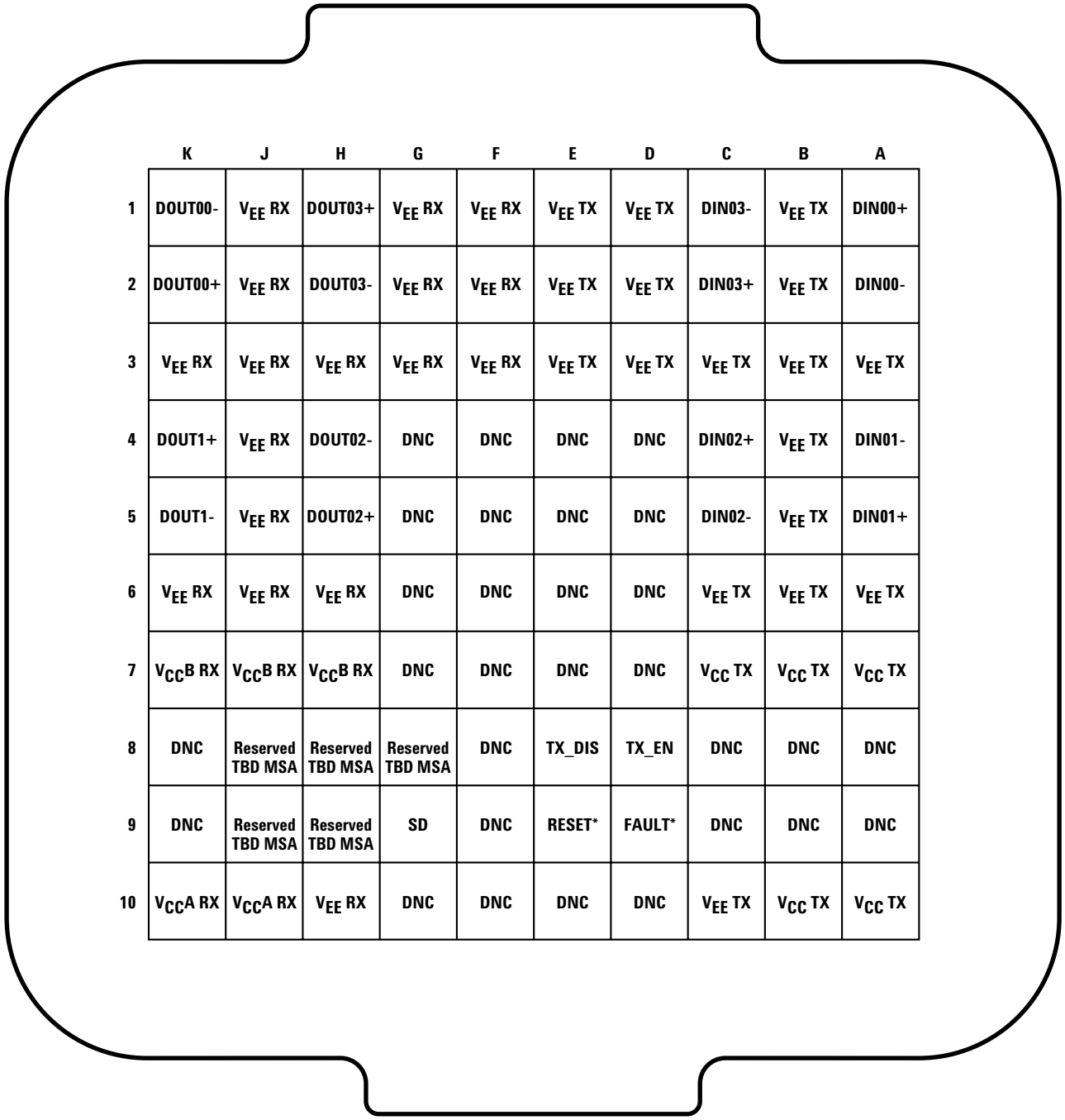
Table 1 - Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD to the Electrical Pads)	JEDEC Human Body (HBM) (JESD22-A114-B) JEDEC Machine Model (MM)	Module > 1000 V Module > 50 V
Electrostatic Discharge (ESD to the Connector Receptacle)	Variation of IEC 61000-4-2	Typically withstand at least 6 kV (module biased) without damage when the connector receptacle is contacted by a Human Body Model probe
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	Typically pass with 5 dB margin. (See Notes 24 and 25)
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	IEC 60825-1 Amendment 2 CFR 21 Section 1040	IEC AEL & US FDA CDRH Class 1M CDRH Accession Number: 9720151-22 TUV Bauart License: E2171095.04
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment.	UL File Number: E173874
RoHS Complaince		Less than 1000ppm of Cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers

Notes:

24. EMI performance only refers to shielded version HFBR-7924EWZ and HFBR-7924EHWZ.
25. EMI performance could be improved by connecting the following pads to electrical ground : C9, G7 and H9.

4+4 Transceiver Module Pad Assignment - HFBR-7924WZ



	K	J	H	G	F	E	D	C	B	A
1	DOUT00-	V_{EE} RX	DOUT03+	V_{EE} RX	V_{EE} RX	V_{EE} TX	V_{EE} TX	DIN03-	V_{EE} TX	DIN00+
2	DOUT00+	V_{EE} RX	DOUT03-	V_{EE} RX	V_{EE} RX	V_{EE} TX	V_{EE} TX	DIN03+	V_{EE} TX	DIN00-
3	V_{EE} RX	V_{EE} RX	V_{EE} RX	V_{EE} RX	V_{EE} RX	V_{EE} TX	V_{EE} TX	V_{EE} TX	V_{EE} TX	V_{EE} TX
4	DOUT1+	V_{EE} RX	DOUT02-	DNC	DNC	DNC	DNC	DIN02+	V_{EE} TX	DIN01-
5	DOUT1-	V_{EE} RX	DOUT02+	DNC	DNC	DNC	DNC	DIN02-	V_{EE} TX	DIN01+
6	V_{EE} RX	V_{EE} RX	V_{EE} RX	DNC	DNC	DNC	DNC	V_{EE} TX	V_{EE} TX	V_{EE} TX
7	V_{CC}B RX	V_{CC}B RX	V_{CC}B RX	DNC	DNC	DNC	DNC	V_{CC} TX	V_{CC} TX	V_{CC} TX
8	DNC	Reserved TBD MSA	Reserved TBD MSA	Reserved TBD MSA	DNC	TX_DIS	TX_EN	DNC	DNC	DNC
9	DNC	Reserved TBD MSA	Reserved TBD MSA	SD	DNC	RESET*	FAULT*	DNC	DNC	DNC
10	V_{CC}A RX	V_{CC}A RX	V_{EE} RX	DNC	DNC	DNC	DNC	V_{EE} TX	V_{CC} TX	V_{CC} TX

TOP VIEW (PCB LAYOUT)
(10 x 10 ARRAY)

Table 2. Transceiver Module Pad Description

Symbol	Functional Description
Din Ch 0 - 3 +/- through Din Ch 0 - 3 +/-	Transmitter differential data inputs for channels 0 through 3: Data inputs are CML compatible.
TX_DIS	Transmitter Disable: LVCMOS Input (Internal pull down). Control input used to turn off the transmitter optical outputs. High Active. VCSEL array is off when High. Normal operation is enabled when Low.
TX_EN	Transmitter Enable: LVCMOS Input (Internal pull up). Control input used to enable the transmitter optical outputs. High Active. VCSEL array is off when Low. Normal operation is enabled when High.
TX_FAULT*	Transmitter Fault: LVCMOS Output. Transmitter status output indicating an eye-safety over-current condition for any VCSEL, an out of temperature range condition and/or a calibration data corruption detection. High output state indicates normal operation. Low output state indicates the fault condition. An asserted FAULT* condition disables the VCSEL array and is cleared by TX_RESET*.
TX_RESET*	Transmitter Reset: LVCMOS Input (Internal pull up). Control input used to reset the transmitter logic functions. Active Low. VCSEL array is off when Low. Normal operation is enabled when High.
V_{EE}_TX	Transmitter signal common. All transmitter voltages are referenced to this potential unless otherwise stated. Directly connect these pads to the PC board transmitter ground plane.
V_{CC}_TX	Transmitter power supply.
Dout Ch 0 - 3 +/- through Dout Ch 0 - 3 +/-	Receiver differential data outputs for channels 0 through 3: Data outputs are CML compatible. Data outputs are squelched for de-asserted Signal Detect.
SD	Receiver Signal Detect: LVCMOS Output. Receiver status output indicating valid signal in all channels. High output state (asserted) indicates valid optical inputs to each and every channel. Low output state (de-asserted) indicates loss of signal at any of the monitored receiver inputs. All channels are monitored.
DNC	Do NOT Connect. Do not connect to any electrical potential.
V_{EE}_RX	Receiver signal common. All receiver voltages are referenced to this potential unless otherwise stated. Directly connect these pads to the PC board receiver ground plane.
V_{CC}A_RX	Pin preamplifier power supply rail.
V_{CC}B_RX	Receiver quantizer power supply rail.
V_{CC}A_RX and V_{CC}B_RX can be connected to the same power supply. However, to insure maximum receiver sensitivity and minimize the impact of noise from the power supply, it is recommended to keep the power supplies separate and to use the recommended power supply filtering network on V_{CC}A_RX (see Figure 8).	
Module Case	Transceiver Case Common. Transceiver Case Common incorporates all exposed conductive surfaces and is electrically isolated from Transmitter Signal Common and Receiver Signal Common.

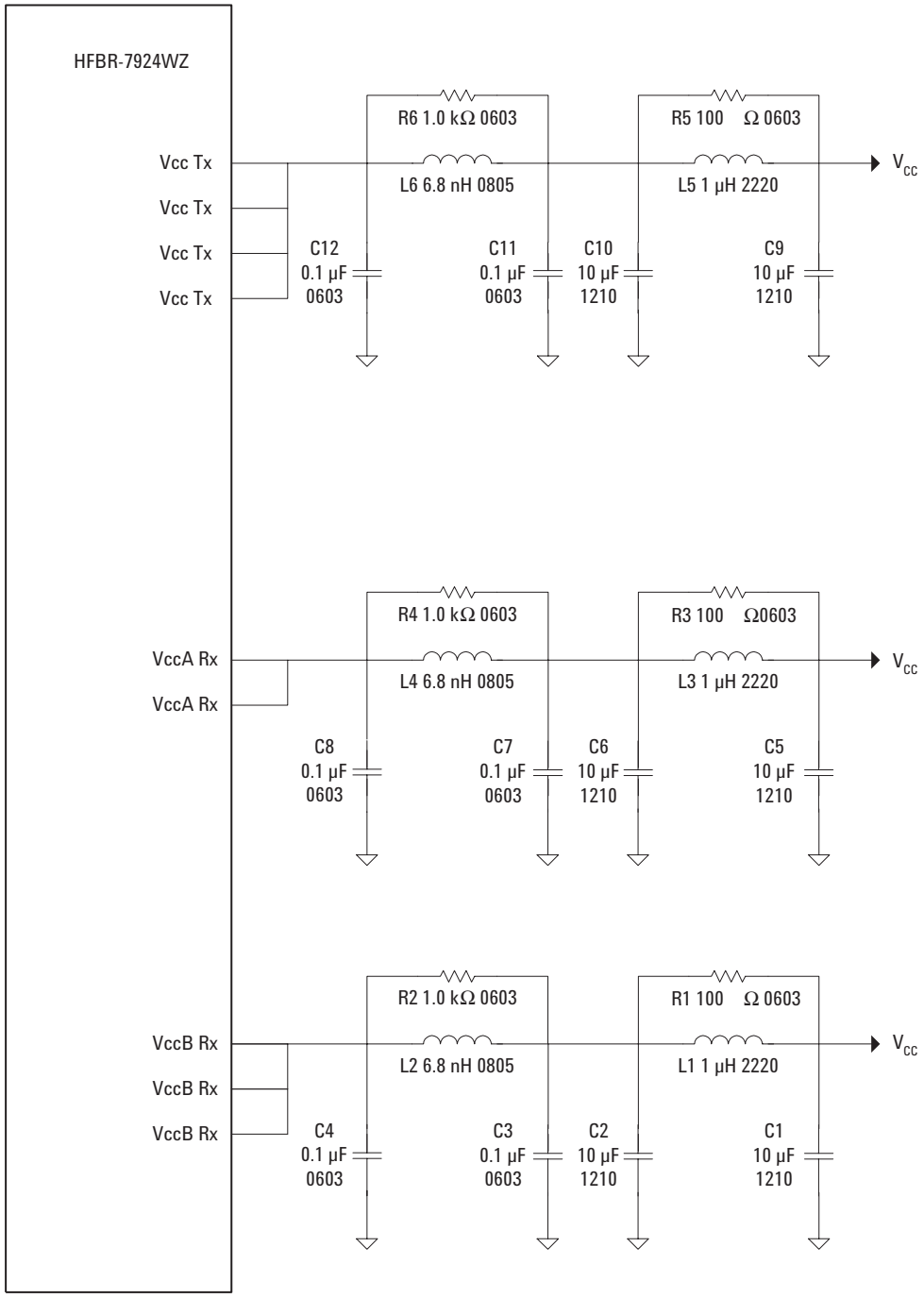
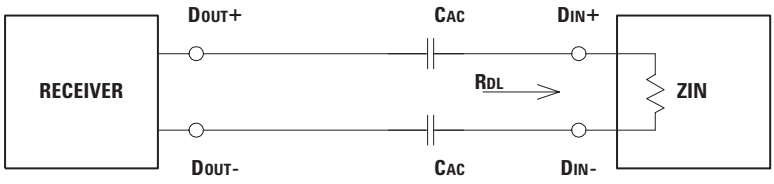


Figure 8 - Recommended power supply filter



AC COUPLING CAPACITORS (DC BLOCKING CAPACITORS) SHOULD BE USED TO CONNECT DATA OUTPUTS TO THE LOAD. THE DIFFERENTIAL DATA PAIR SHOULD BE TERMINATED WITH A DIFFERENTIAL LOAD, R_{DL}, OF 100 Ω USING EITHER AN INTERNAL LOAD, Z_{IN}, AS SHOWN ABOVE, OR AN EXTERNAL LOAD, IF NECESSARY.

Figure 9 - Recommended AC coupling and data signal termination

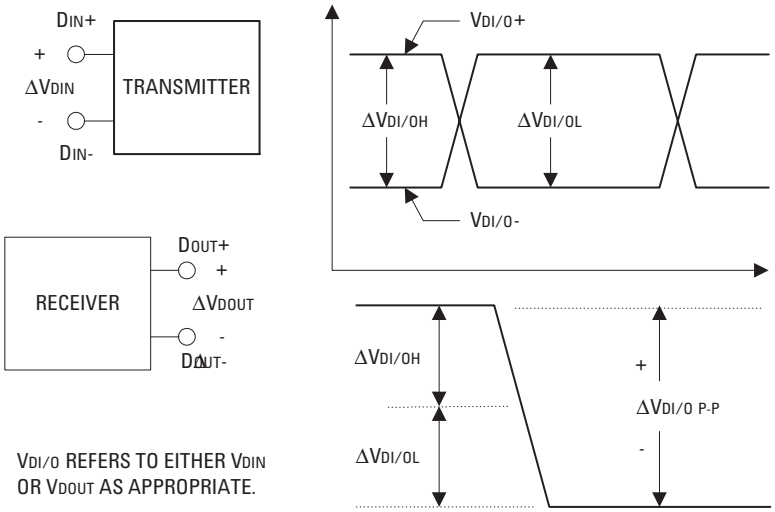


Figure 10 - Differential signals

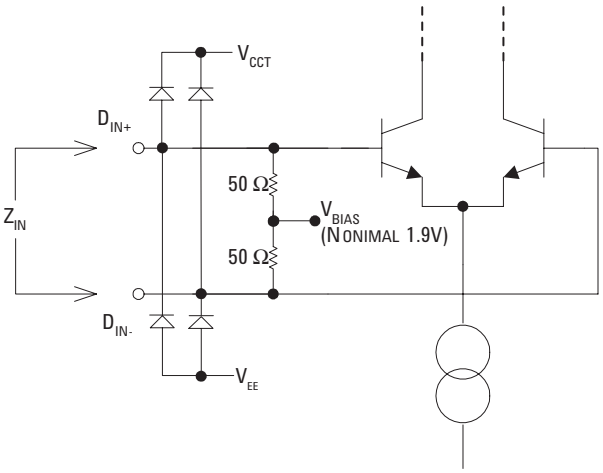


Figure 11 - Transmitter data input equivalent circuit

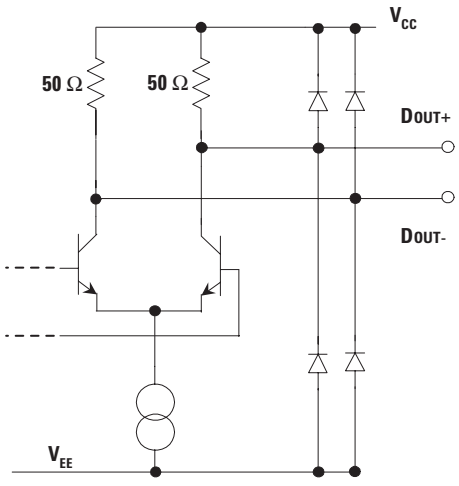


Figure 12 - Receiver data output equivalent circuit.

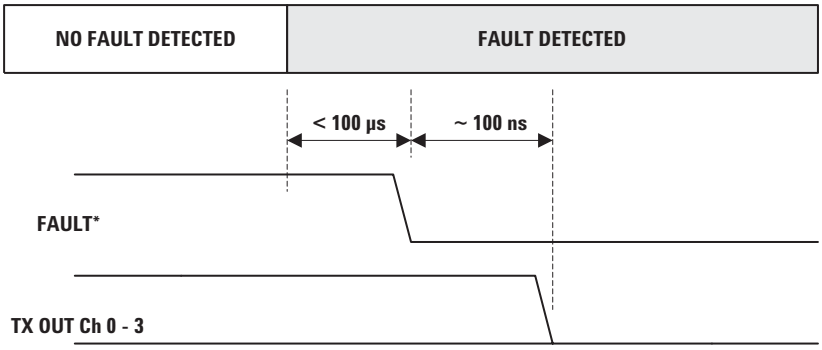


Figure 13 - Transmitter FAULT* signal timing diagram

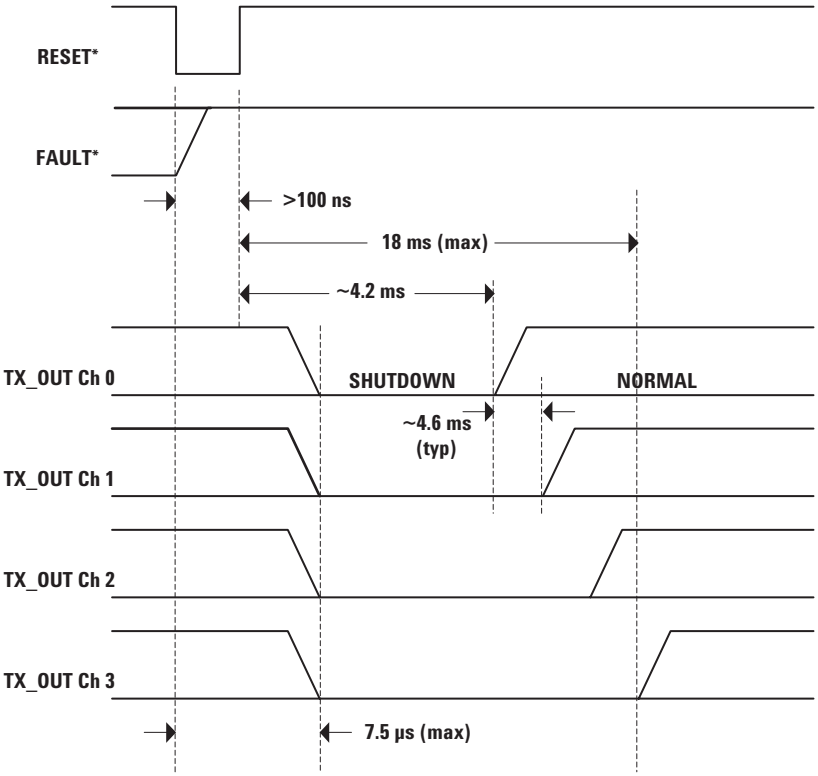


Figure 14 - Transmitter RESET* timing diagram

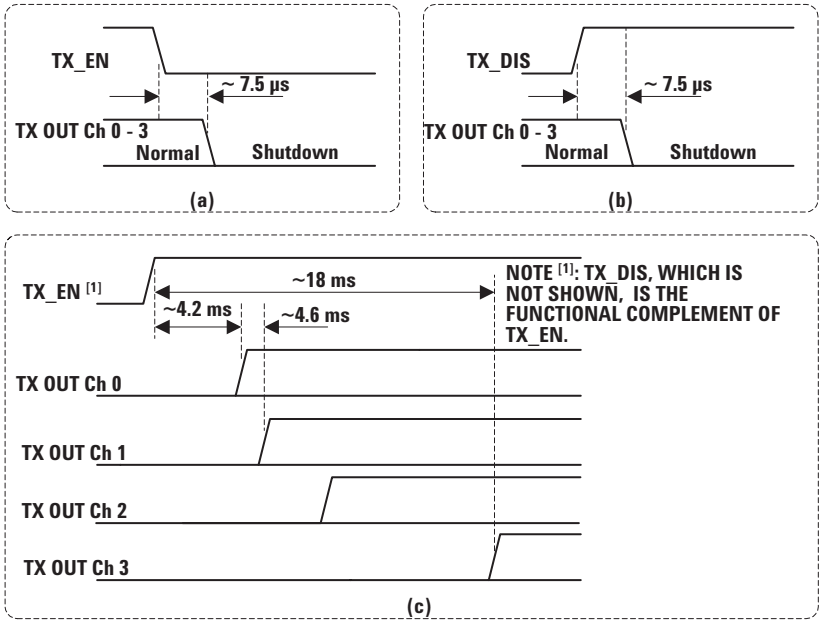
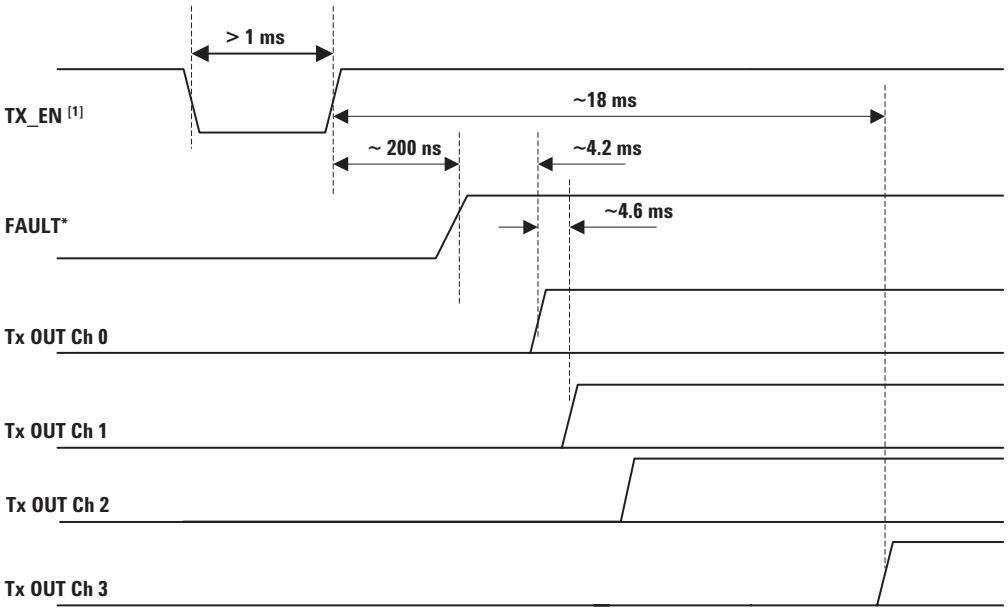


Figure 15 - Transmitter TX_EN and TX_DIS timing diagram



NOTE [1]. TX_DIS, WHICH IS NOT SHOWN, IS THE FUNCTIONAL COMPLEMENT OF TX_EN.

Figure 16 - Transmitter fault recovery via TX_EN timing diagram

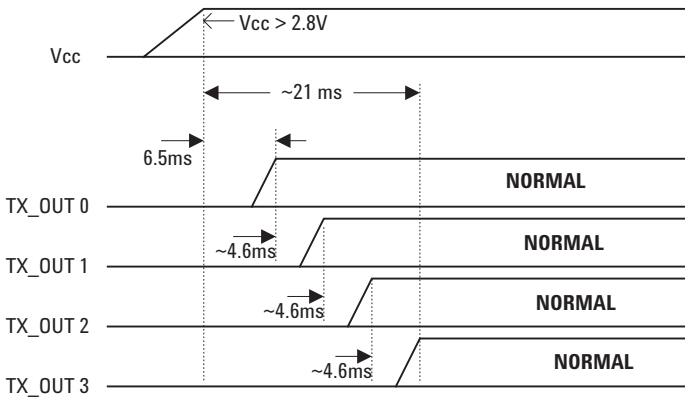


Figure 17. Typical Transmitter Power-Up Sequence

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