Multiformat SD, Progressive Scan/HDTV Video Encoder with Six NSV™ 14-Bit DACs

ADV7304A/ADV7305A

FEATURES

High Definition Input Formats
- YCrCb Compliant to SMPTE293M (525 p), ITU-R.BT1358 (625 p), SMPTE274M (1080 i), SMPTE296M (720 p), and Any Other High Definition Standard Using Async Timing Mode
- RGB in 3 × 10-Bit 4:4:4 Format
- BTA T-1004 EDTV2 525 p Parallel

High Definition Output Formats (525 p/625 p/720 p/1080 i)
- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA 770.3)
- RGB + H/V (HDTV 5-Wire Format)
- CGMS-A (720 p/1080 i)
- Macrovision Rev 1.0 (525 p/625 p)*
  - CGMS-A (525 p)

Standard Definition Input Formats
- CCIR-656 4:2:2 8-/10-Bit Parallel Input
- CCIR-601 4:2:2 16-/20-Bit Parallel Input

Standard Definition Output Formats
- Composite NTSC M, N;
  - PAL M, N, B, D, G, H, I, PAL-60
- SMPTE170M NTSC Compatible Composite Video
- ITU-R.BT470 PAL Compatible Composite Video
- S-Video (Y/C)
- EuroScart RGB
- Component YUV (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1*
  - CGMS/WSS
  - Closed Captioning

GENERAL FEATURES

- Simultaneous SD and HD Inputs and Outputs
- Oversampling (108 MHz/148.5 MHz)
- On-Board Voltage Reference
- 6 NSV Precision Video 14-Bit Σ-Δ DACs
- 2-Wire Serial MPU Interface
- Dual I/O Supply 2.5 V/3.3 V Operation
- Analog and Digital Supply 2.5 V
- On-Board PLL
- 64-LQFP Package
- Lead-Free Product

APPLICATIONS

- High End DVD Players
- SD/Program Scan/HDTV Display Devices
- SD/Program Scan/HDTV Set-Top Boxes
- SD/HDTV Studio Equipment
- Professional Video Equipment

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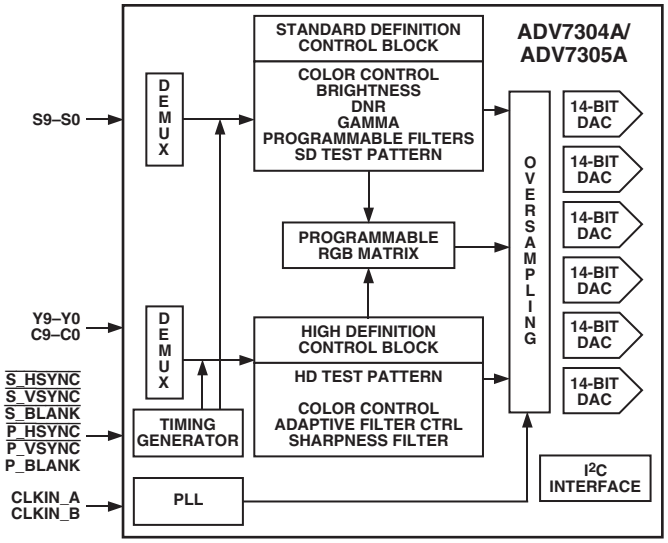
*ADV7304A Only

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7304A/ADV7305A is a high speed, digital-to-analog encoder on a single monolithic chip. It includes six high speed video D/A converters with TTL compatible inputs.

The ADV7304A/ADV7305A has three separate 10-bit wide input ports that accept data in high definition and/or standard definition video format. For all standards, external horizontal, vertical, and blanking signals, or EAV/SAV timing codes, control the insertion of appropriate synchronization signals into the digital data stream and therefore the output signals.

REV. A

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DETAILED FEATURES

High Definition Programmable Features (720 p/1080 i)
- **2× Oversampling (148.5 MHz)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Field/Frame)**
- **Fully Programmable YCrCb to RGB Matrix**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Programmable Sharpness Filter Control**
- **CGMS-A (720 p/1080 i)**

High Definition Programmable Features (525 p/625 p)
- **4× Oversampling (108 MHz Output)**
- **Internal Test Pattern Generator (Color Hatch, Black Bar, Flat Frame)**
- **Individual Y and PrPb Output Delay**
- **Gamma Correction**
- **Programmable Adaptive Filter Control**
- **Fully Programmable YCrCb to RGB Matrix**
- **Undershoot Limiter**
- **Macrovision Rev 1.0 (525 p/625 p)***
- **CGMS-A (525 p)**

Standard Definition Programmable Features
- **8× Oversampling (108 MHz)**
- **Internal Test Pattern Generator (Color Bars, Black Bar)**
- **Controlled Edge Rates for Sync, Active Video**
- **Individual Y and UV Output Delay**
- **Gamma Correction**
- **Digital Noise Reduction**
- **Multiple Chroma and Luma Filters**
- **Luma-SSAF™ Filter with Programmable Gain/ Attenuation**
- **UV SSAF**
- **Separate Pedestal Control on Component and Composite/S-Video Outputs**
- **VCR FF/RW Sync Mode**
- **Macrovision Rev 7.1***
- **CGMS/WSS**
- **Closed Captioning**

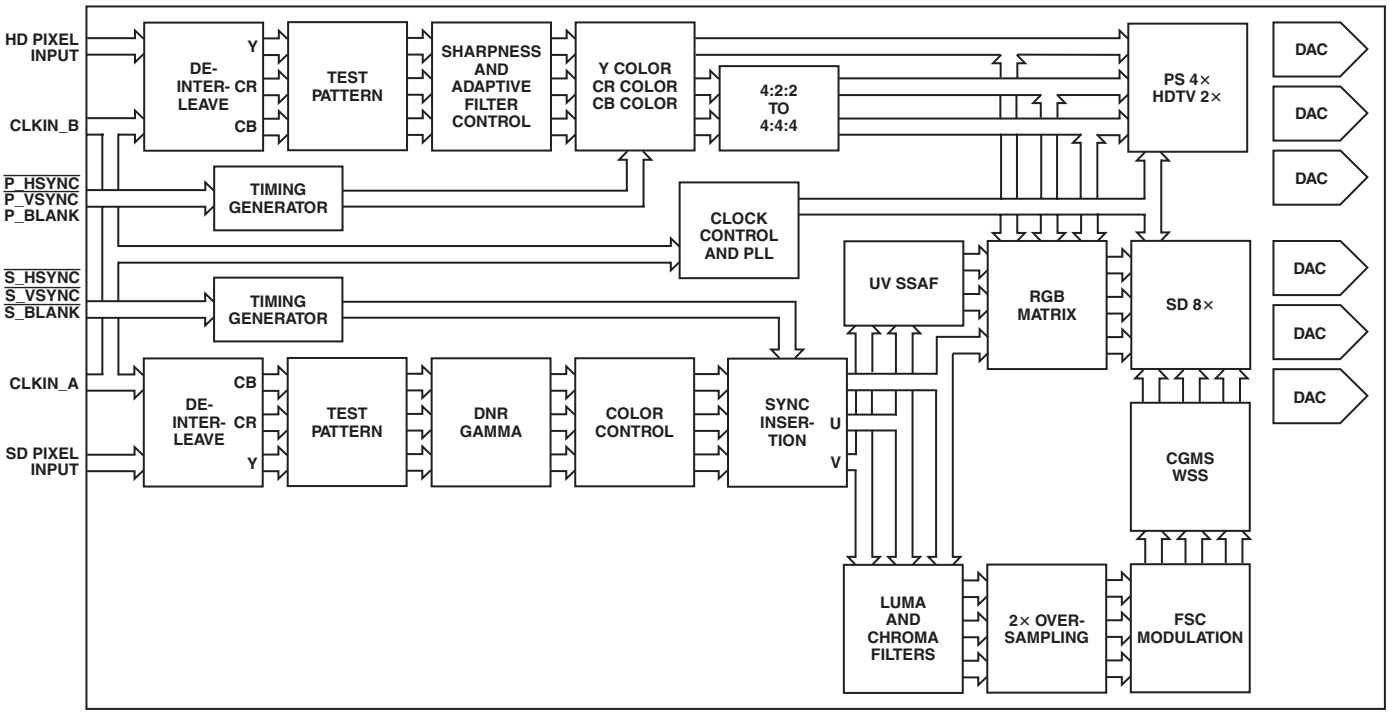

Figure 1. Functional Block Diagram

TERMS USED IN THIS DATA SHEET

SD Standard Definition Video, conforming to ITU-R.BT601/ITU-R.BT656.

HD High Definition Video, i.e., Progressive Scan or HDTV.

PS Progressive Scan Video, conforming to SMPTE293M or ITU-R.BT1358.

HDTV High Definition Television Video, conforming to SMPTE274M or SMPTE296M.

YCrCb SD or HD Component Digital Video.

YPrPb HD Component Analog Video.

YUV SD Component Analog Video.

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*ADV7304A Only

ADV7304A/ADV7305A–SPECIFICATIONS

(V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 1520 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE[1]					
Resolution		14		Bits	
Integral Nonlinearity		±3.0		LSB	
Differential Nonlinearity, +ve[2]		1		LSB	
Differential Nonlinearity, –ve[2]		5.5		LSB	
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4 [0.4][3]	V	I_{SINK} = 3.2 mA
Output High Voltage, V_{OH}	2.4 [2.0][3]			V	I_{SOURCE} = 400 µA
Three-State Leakage Current		±1.0		µA	V_{IN} = 0.4 V, 2.4 V
Three-State Output Capacitance		2		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current		1		µA	V_{IN} = 2.4 V
Input Capacitance, C_{IN}		2		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	4.2	4.33	4.5	mA	
Output Current Range	4.2	4.33	4.5	mA	
DAC to DAC Matching		2.0		%	
Output Compliance Range, V_{OC}	0	1.0	1.4	V	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE					
Reference Range, V_{REF}	1.17	1.235	1.3	V	
POWER REQUIREMENTS					
Normal Power Mode					
I_{DD}[4]		93		mA	SD Only [8×]
		52		mA	PS Only [4×]
		84		mA	HDTV Only [2×]
		90	110	mA	SD and PS
		99		mA	SD [8×] and HDTV
		108		mA	SD and HDTV [2×]
I_{DD_IO}		0.2		mA	
I_{AA}[5,6]		70	75	mA	
Sleep Mode					
I_{DD}		130		µA	
I_{AA}		10		µA	
I_{DD_IO}		110		µA	
Power Supply Rejection Ratio		0.01		%/%	

NOTES

[1]NSV features enabled.

[2]DNL measures the deviation of the actual DAC o/p voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value; for –ve DNL, the actual step values lie below the ideal step value.

[3]Value in brackets for V_{DD_IO} = 2.375 V to 2.750 V.

[4]I_{DD} or the circuit current is the continuous current required to drive the digital core without the I_{PLL}.

[5]I_{AA} is the total current required to supply all DACs including the V_{REF} and PLL circuitry.

[6]All DACs on.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 1520 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
PROGRESSIVE SCAN MODE					
Luma Bandwidth		12.5		MHz	
Chroma Bandwidth		5.8		MHz	
SNR		64		dB	Luma Ramp Unweighted
SNR		82		dB	Flat Field up to 5 MHz
SNR		79		dB	Flat Field Full Bandwidth
HDTV MODE					
Luma Bandwidth		30		MHz	
Chroma Bandwidth		13.75		MHz	
SNR		64		dB	Luma Ramp Unweighted
SNR		82		dB	Flat Field up to 5 MHz
SNR		79		dB	Flat Field Full Bandwidth
STANDARD DEFINITION MODE					
Hue Accuracy		0.6		Degrees	
Color Saturation Accuracy		0.5		%	
Chroma Nonlinear Gain		±0.4		%	Referenced to 40 IRE
Chroma Nonlinear Phase		±0.4		Degrees	
Chroma/Luma Intermodulation		0		%	
Chroma/Luma Gain Inequality		±98.5		%	
Chroma/Luma Delay Inequality		0.6		ns	
Luminance Nonlinearity		±0.1		%	
Chroma AM Noise		87.2		dB	
Chroma PM Noise		78.4		dB	
Differential Gain		0.07		%	NTSC
Differential Phase		0.13		Degrees	NTSC
SNR		64		dB	Luma Ramp
SNR		82		dB	Flat Field up to 5 MHz
SNR		79		dB	Flat Field Full Bandwidth

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{AA} = V_{DD} = 2.375 V–2.625 V, V_{DD_IO} = 2.375 V–3.600 V, V_{REF} = 1.235 V, R_{SET} = 1520 Ω, R_{LOAD} = 150 Ω, T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT[1]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	First Clock Generated after This Period
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
$\overline{\text{RESET}}$ Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		8		ns	
Output Skew		1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			27	MHz	Progressive Scan Mode
f_{CLK}		81		MHz	HDTV Mode/Async Mode
Clock High Time, t_9	40			% 1 clkcycle	
Clock Low Time, t_{10}	40			% 1 clkcycle	
Data Setup Time, t_{11}	2.0			ns	
Data Hold Time, t_{12}	2.0			ns	
Output Access Time, t_{13}			14	ns	
Output Hold Time, t_{14}	4.0			ns	
Pipeline Delay		61		clkcycles	SD [2×]
		62.5		clkcycles	SD [8×]
		66.5		clkcycles	SD Component Filter [8×]
		33		clkcycles	PS [1×], HD [1×], Async Timing Mode
		43.5		clkcycles	PS [4×]
		36		clkcycles	HD [2×]

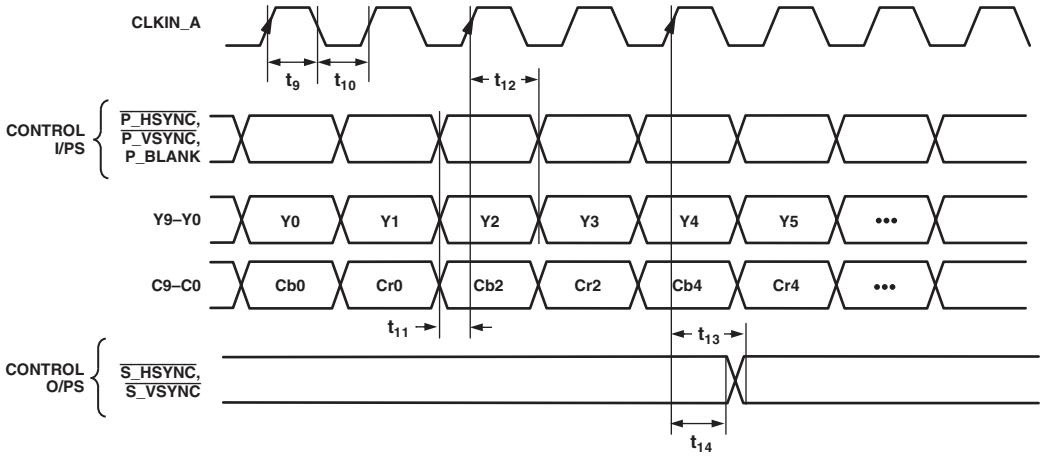
NOTES

[1]Guaranteed by characterization.

[2]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.

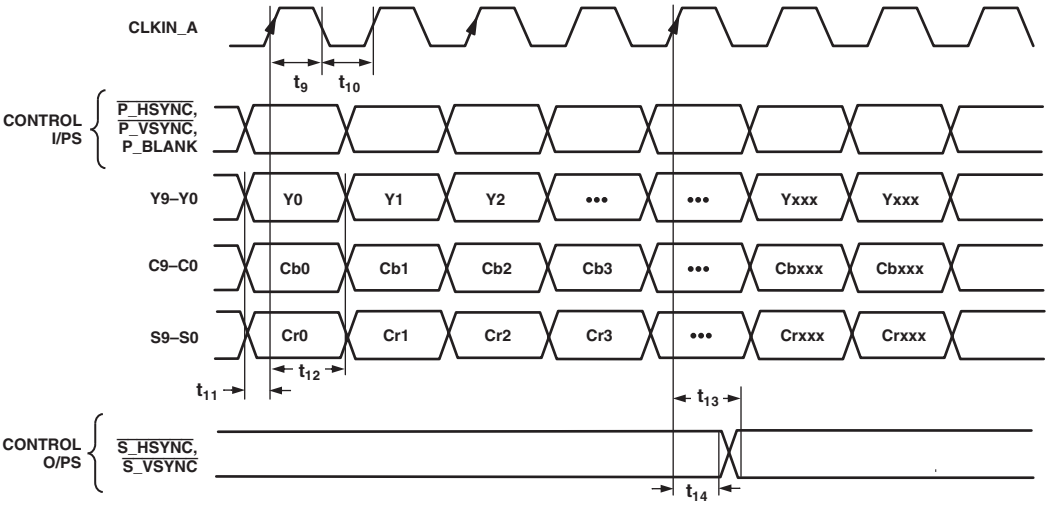
[3]Data: C[9:0]; S[9:0]; Y[9:0]
Control: $\overline{\text{P\_HSYNC}}$; $\overline{\text{P\_ VSYNC}}$; P_BLANK; $\overline{\text{S\_HSYNC}}$; $\overline{\text{S\_VSYNC}}$; $\overline{\text{S\_BLANK}}$

Specifications subject to change without notice.



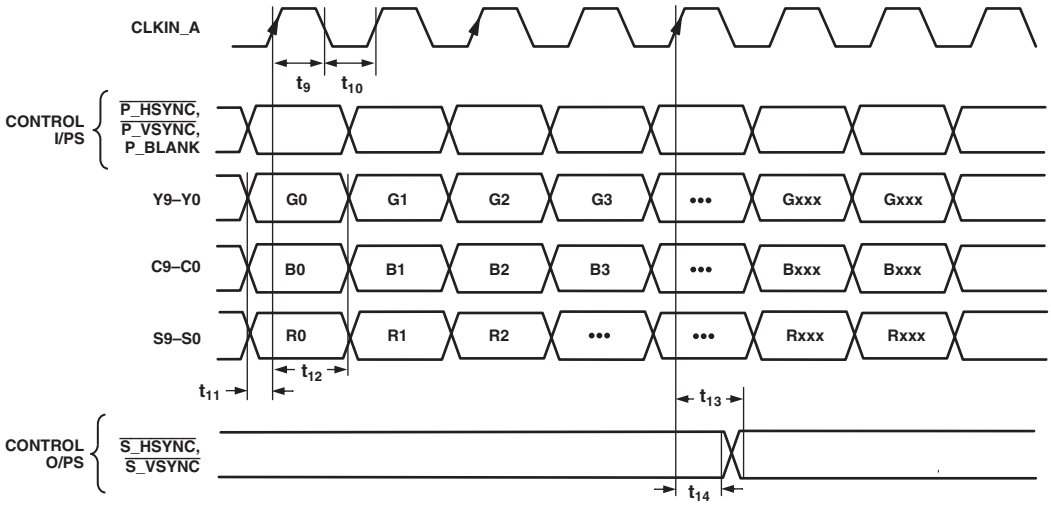
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 2. HD 4:2:2 Input Data Format Timing Diagram, Input Mode: PS Input Only, HDTV Input Only (Input Mode at Subaddress 01h = 001 or 010)



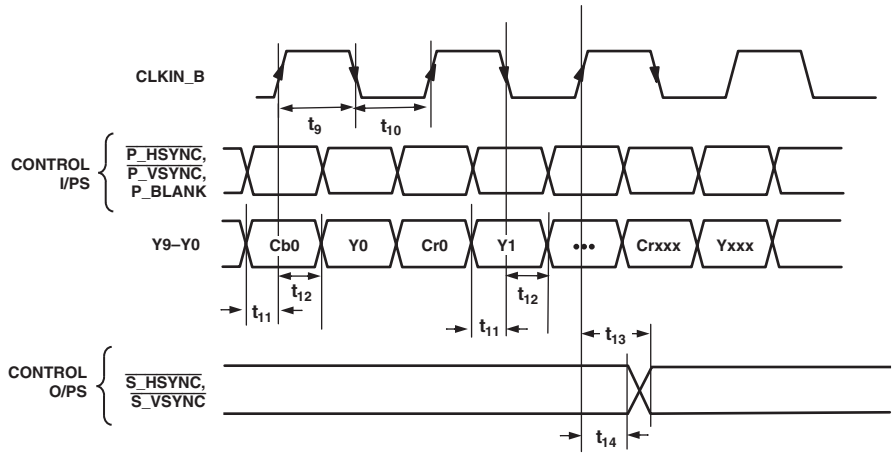
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 3. HD 4:4:4 YCrCb Input Data Format Timing Diagram, Input Mode: PS Input Only, HDTV Input Only (Input Mode at Subaddress 01h = 001 or 010)



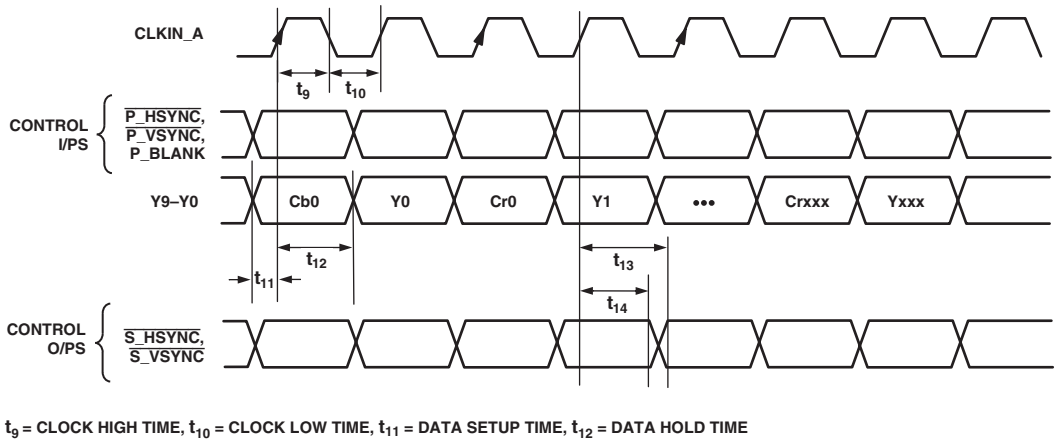
t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 4. HD 4:4:4 RGB Input Data Format Timing Diagram, HD RGB Input Enabled (Input Mode at Subaddress 01h = 001 or 010)



t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 5. PS 4:2:2 1 × 10-Bit Interleaved @ 27 MHz, Input Mode: PS Input Only (Input Mode at Subaddress 01h = 100)



t_9 = CLOCK HIGH TIME, t_{10} = CLOCK LOW TIME, t_{11} = DATA SETUP TIME, t_{12} = DATA HOLD TIME

Figure 6. PS 4:2:2 1 × 10-Bit Interleaved @ 54 MHz, Input Mode: PS 54 MHz Input (Input Mode at Subaddress 01h = 111)

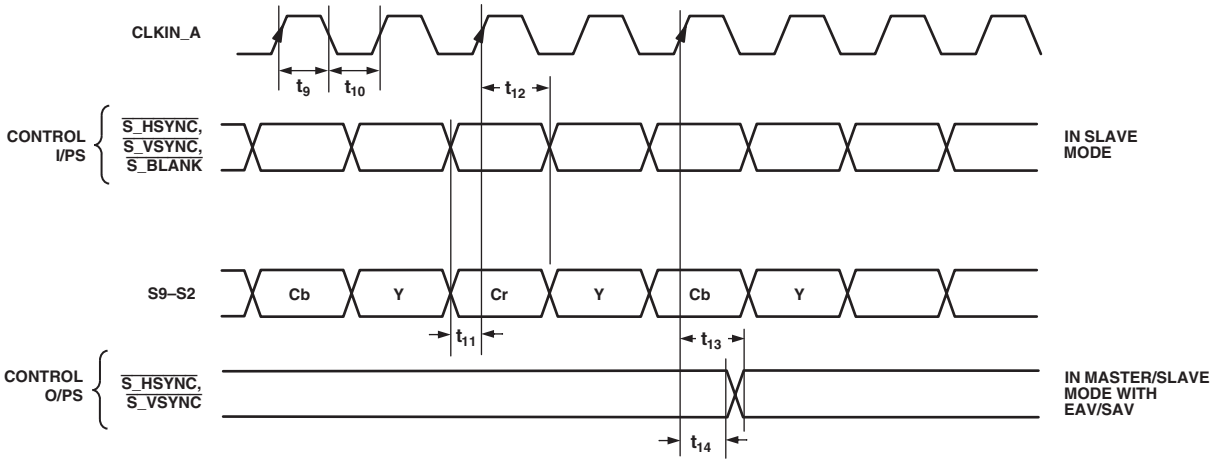


Figure 7. 8-Bit SD Pixel Input Timing Diagram, Input Mode: SD Input Only (Input Mode at Subaddress 01h = 000)

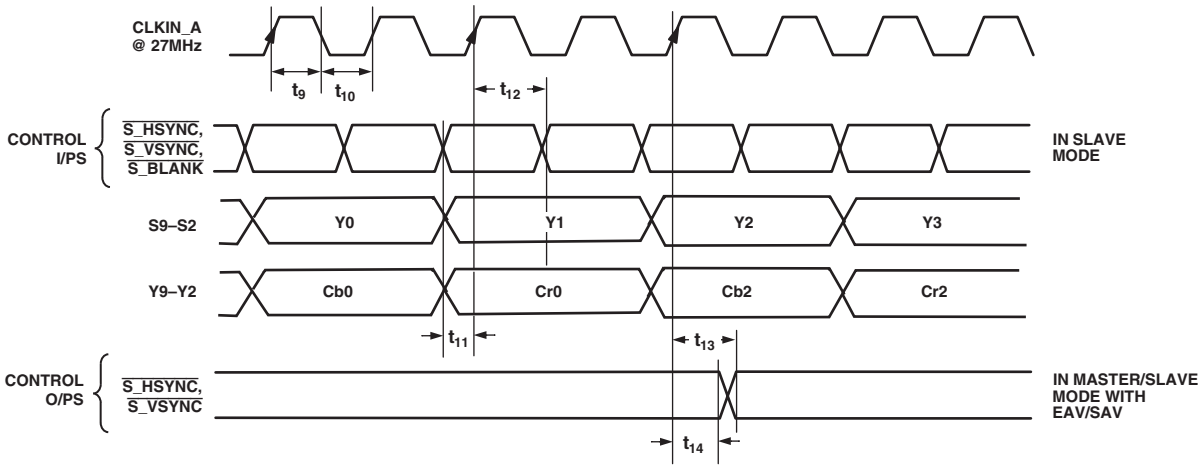


Figure 8. 16-Bit SD Pixel Input Timing Diagram, Input Mode: SD Input Only (Input Mode at Subaddress 01h = 000)

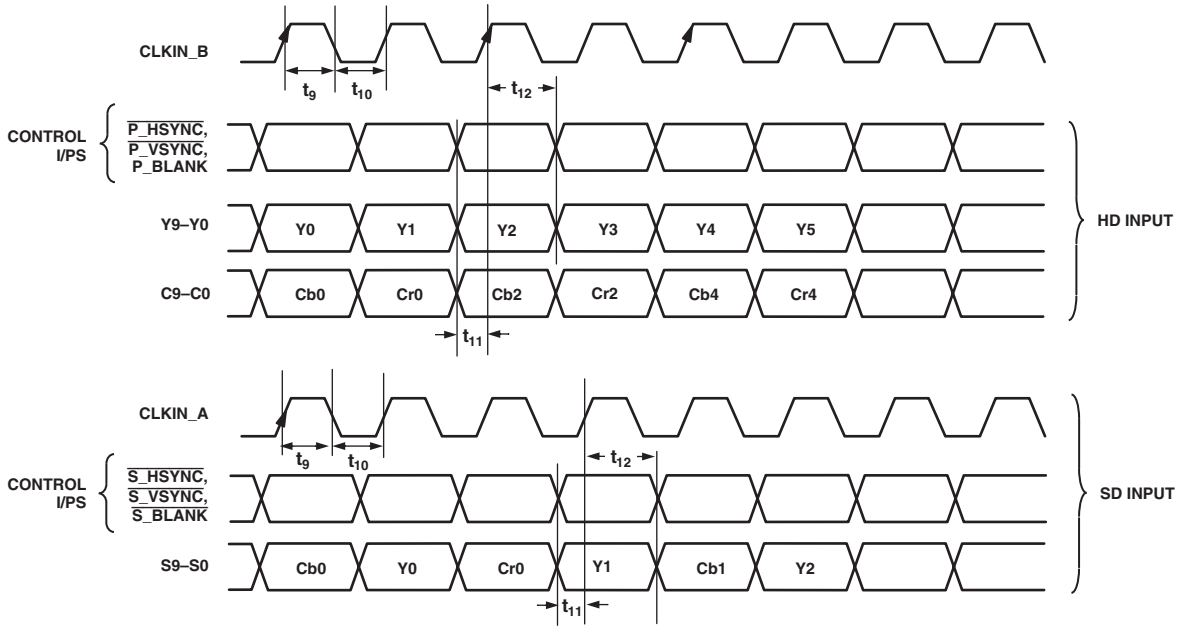


Figure 9. SD and HD Simultaneous Input, Input Mode: SD and PS 20-Bit or SD and HDTV (Input Mode at Subaddress 01h = 011, 101, or 110)

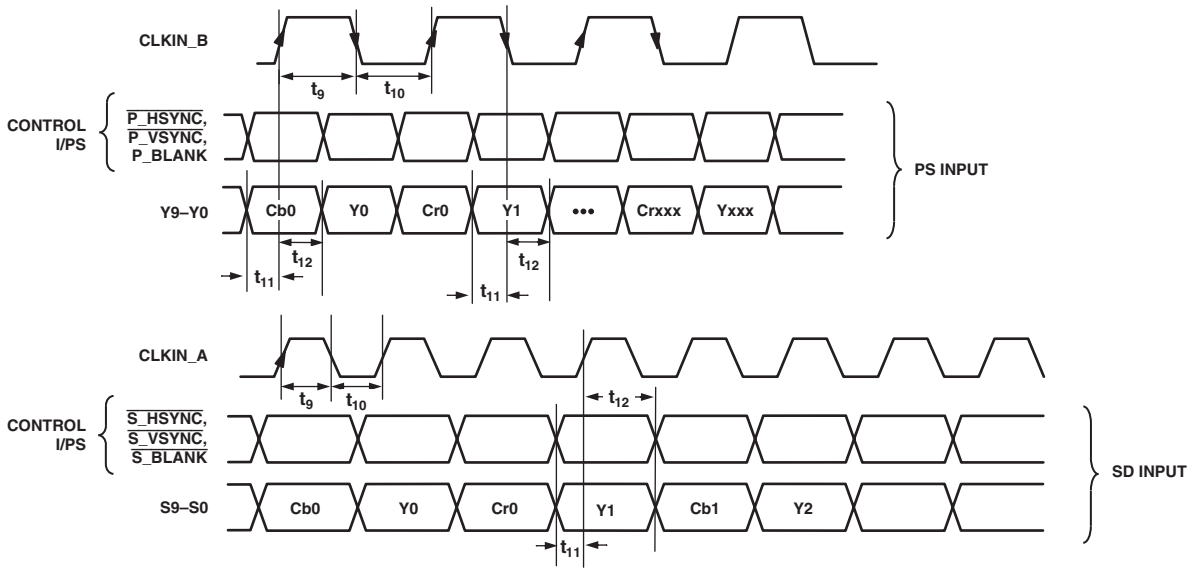


Figure 10. SD and HD Simultaneous Input, Input Mode: SD and PS 10-Bit (Input Mode at Subaddress 01h = 100)

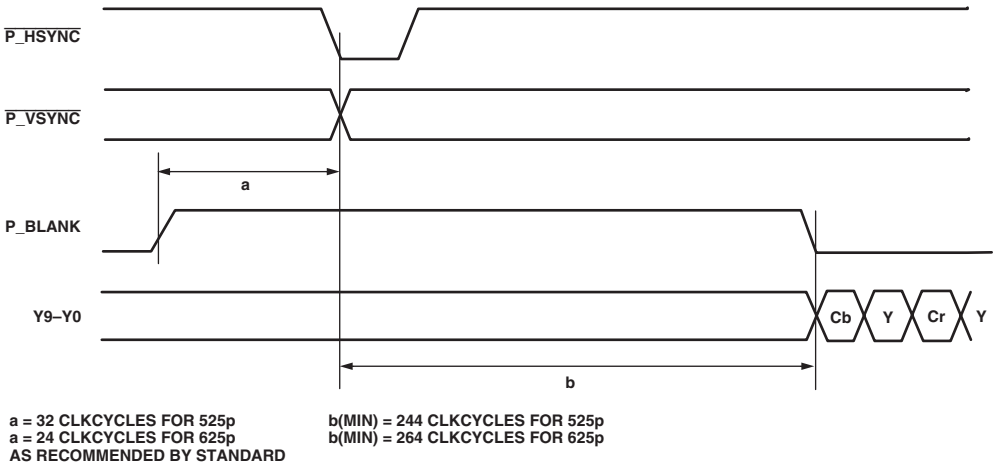
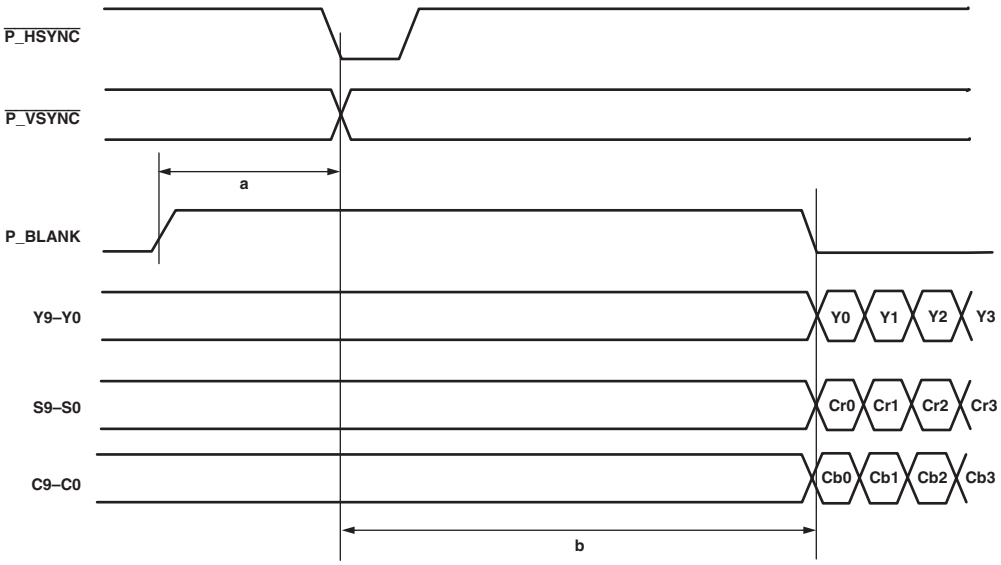


Figure 11. PS 4:2:2 1 × 10-Bit Interleaved @ 54 MHz Input Timing Diagram



a = 16 CLKCYCLES FOR 525p
a = 12 CLKCYCLES FOR 626p
a = 44 CLKCYCLES FOR 1080i
a = 70 CLKCYCLES FOR 720p
AS RECOMMENDED BY STANDARD

b(MIN) = 122 CLKCYCLES FOR 525p
b(MIN) = 132 CLKCYCLES FOR 625p
b(MIN) = 236 CLKCYCLES FOR 1080i
b(MIN) = 300 CLKCYCLES FOR 720p

Figure 12. HD Input Timing Diagram

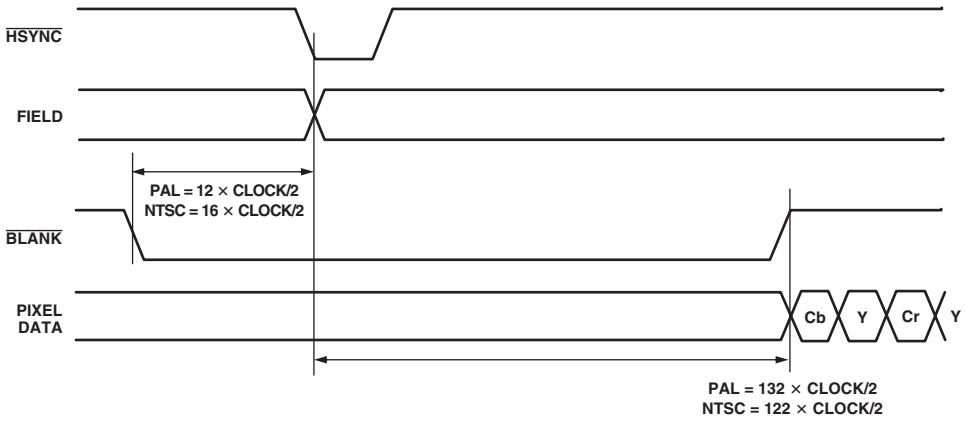


Figure 13. SD Timing Input for Timing Mode 1

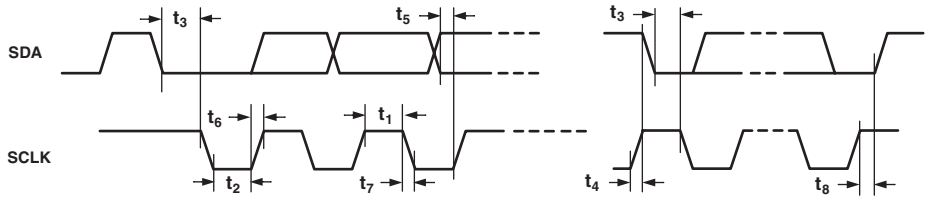


Figure 14. MPU Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to AGND . . . . . +3.0 V to –0.3 V
V_{DD} to GND . . . . . +3.0 V to –0.3 V
V_{DD_IO} to IO_GND . . . . . –0.3 V to V_{DD_IO} + 0.3 V
Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Infrared Reflow Soldering (20 sec) . . . . . 260°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The ADV7304A/ADV7305A is a lead-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure tin electroplate. The device is suitable for lead-free applications and is able to withstand surface-mount soldering up to 255°C (±5°C). In addition, it is backward compatible with conventional tin-lead soldering processes. This means that the electroplated tin coating can be soldered with tin-lead solder pastes at conventional reflow temperatures of 220°C to 235°C.

THERMAL CHARACTERISTICS

θ_{JC} = 11°C/W

θ_{JA} = 47°C/W

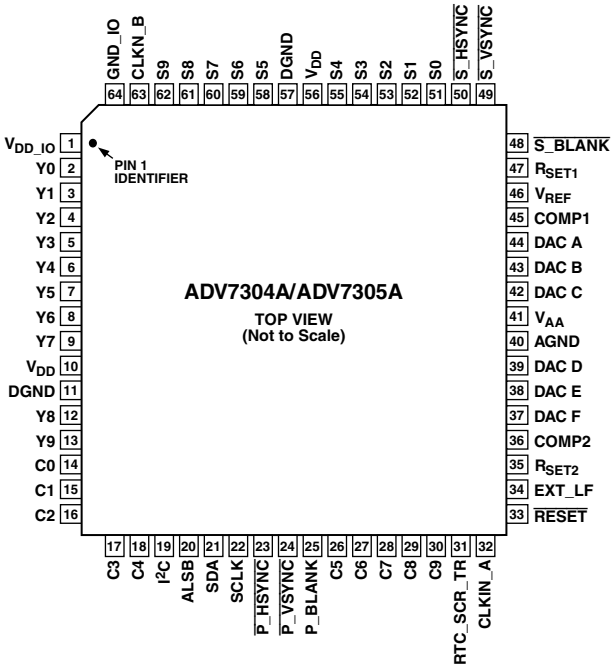
ORDERING GUIDE

Model	Package Description	Package Option
ADV7304AKST	Plastic Quad Flatpack	ST-64B
ADV7305AKST	Plastic Quad Flatpack	ST-64B

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7304A/ADV7305A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/Output	Function
1	V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs
2–9, 12, 13	Y0–Y9	I	10-Bit Progressive Scan/HDTV Input Port for Y Data. The LSBs are set up on Pins Y0 and Y1. In Default Mode, the input on this port is output on DAC D.
10, 56	V_{DD}	P	Digital Power Supply
11, 57	DGND	G	Digital Ground

Pin No.	Mnemonic	Input/Output	Function
14–18, 26–30	C0–C9	I	10-Bit Progressive Scan/HDTV Input Port for CrCb Color Data in 4:2:2 Input Mode. In 4:4:4 Input Mode, this input port is used for the Cb (Blue/U) data. The LSBs are set up on Pins C0 and C1. In Default Mode, the input on this port is output on DAC E.
19	I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7304A/ADV7305A to interface over the I^2C port.
20	ALSB	I/O	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
21	SDA	I/O	MPU Port Serial Data Input/Output
22	SCLK	I	MPU Port Serial Interface Clock Input
23	$\overline{\text{P\_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
24	$\overline{\text{P\_VSYNC}}$	I	Video Vertical Sync Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
25	P_BLANK	I	Video Blanking Control Signal for HD Sync in Simultaneous SD/HD Mode and HD Only Mode
31	RTC_SCR_TR	I	Multifunctional Input: Realtime Control (RTC) Input, Timing Reset Input, and Subcarrier Reset Input
32	CLKIN_A	I	Pixel Clock Input for HD Only or SD Only Modes
33	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7304A/ ADV7305A into default register setting. Reset is an active low signal.
34	EXT_LF	I	External Loop Filter for the Internal PLL
35, 47	$R_{SET1, 2}$	I	A 1520 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
36, 45	COMP2, 1	O	Compensation Pin for DACs. Connect 0.1 μF capacitor from COMP pin to V_{AA}.
37	DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output, in HD Only Mode and Simultaneous HD/SD: Pb/Blue (HD) Analog Output
38	DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output, in HD Only Mode and Simultaneous HD/SD: Pr/Red (HD) Analog Output
39	DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output, in HD Only Mode and Simultaneous HD/SD: Y/Green (HD) Analog Output
40	AGND	G	Analog Ground
41	V_{AA}	P	Analog Power Supply
42	DAC C	O	Chroma/Red/V SD Analog Output
43	DAC B	O	Luma/Blue/U SD Analog Output
44	DAC A	O	CVBS/Green/Y SD Analog Output
46	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V)
48	$\overline{\text{S\_BLANK}}$	I/O	Video Blanking Control Signal for SD
49	$\overline{\text{S\_VSYNC}}$	I/O	Video Vertical Control Signal for SD. Option to output SD VSYNC or SD HSYNC in SD Slave Mode 0 and/or any HD Mode.
50	$\overline{\text{S\_HSYNC}}$	I/O	Video Horizontal Control Signal for SD. Option to output SD HSYNC or HD HSYNC in SD Slave Mode 0 and/or any HD Mode.
51–55, 58–62	S0–S9	I	10-Bit Standard Definition Input Port or Progressive Scan/HDTV Input Port for Cr (Red/V) Color Data in 4:4:4 Input Mode. The LSBs are set up on Pins S0 and S1. In Default Mode, the input on this port is output on DAC F.
63	CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for Progressive Scan Mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV Mode. This clock input pin is only used in Simultaneous SD/HD Mode.
64	GND_IO		Digital Ground

MPU PORT DESCRIPTION

The ADV7304A/ADV7305A supports a 2-wire serial (I^2C compatible) microprocessor bus driving multiple peripherals. Two inputs, Serial Data (SDA) and Serial Clock (SCLK), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7304A/ADV7305A has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figures 15 and 16. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation, while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7304A/ADV7305A to Logic Level "0" or Logic Level "1." When ALSB is set to "1," there is greater input bandwidth on the I^2C lines, which allows high speed data transfers on this bus. When ALSB is set to "0," there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

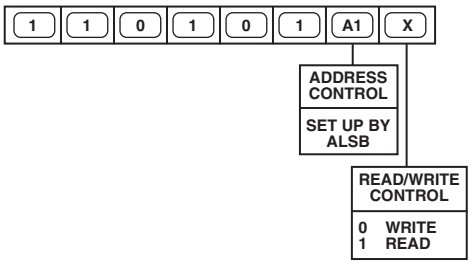


Figure 15. ADV7304A Slave Address = D4h

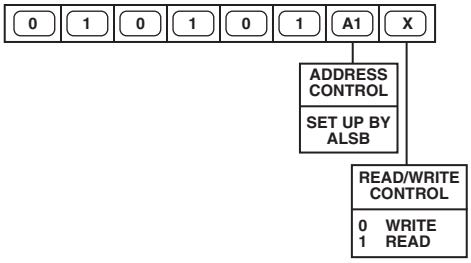


Figure 16. ADV7305A Slave Address = 54h

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA, while SCLK remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/W Bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an Acknowledge Bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCLK lines waiting for the start condition and the correct transmitted address. The R/W Bit determines the direction of the data.

A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7304A/ADV7305A acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long, supporting the 7-bit addresses plus the R/W Bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddress's auto-increment allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, it will cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7304A/ADV7305A will not issue an acknowledge and will return to the idle condition. If in Autoincrement Mode the user exceeds the highest subaddress, the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7304A/ADV7305A, and the part will return to the idle condition.

Before writing to the subcarrier frequency registers, it is a requirement that the ADV7304A/ADV7305A has been reset at least once since power-up.

The four subcarrier frequency registers must be updated starting with Subcarrier Frequency Register 0. The subcarrier frequency will not update until the last subcarrier frequency register byte has been received by the ADV7304A/ADV7305A.

Figure 17 illustrates an example of data transfer for a read sequence and the start and stop conditions.

Figure 18 shows bus write and read sequences.

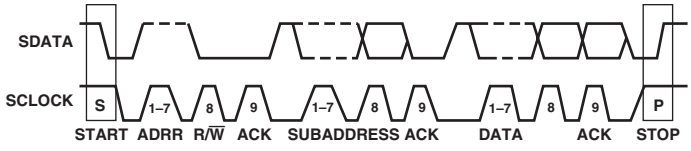


Figure 17. Bus Data Transfer

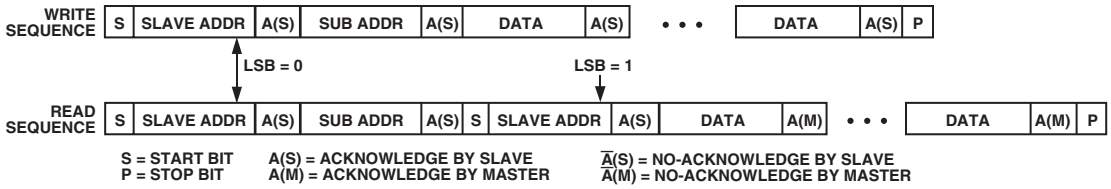


Figure 18. Read and Write Sequence

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7304A/ADV7305A except the subaddress registers that are write-only registers. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. Then a read/write operation is performed from/to the target address, which then increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes the functionality of each register. All registers can be read from as well as written to unless otherwise stated.

Subaddress Register (SR7–SR0)

The Communications Register is an 8-bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Register Select (SR7–SR0)

These bits are set up to point to the required starting address.

Table I. Power Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
00h	Power Mode Register	Sleep Mode[1]								0	Sleep Mode Off	Fch
										1	Sleep Mode On	
		PLL and Oversampling Control[2]							0		PLL On	
									1		PLL Off	
		DAC F: Power On/Off						0			DAC F Off	
								1			DAC F On	
		DAC E: Power On/Off					0				DAC E Off	
							1				DAC E On	
		DAC D: Power On/Off				0					DAC D Off	
						1					DAC D On	
		DAC C: Power On/Off			0						DAC C Off	
					1						DAC C On	
		DAC B: Power On/Off		0							DAC B Off	
				1							DAC B On	
		DAC A: Power On/Off	0								DAC A Off	
			1								DAC A On	

NOTES
[1]When enabled, the current consumption is reduced to μA level. All DACs and the internal PLL circuit are disabled. I^2C registers can be read from and written to.
[2]This control allows the internal PLL circuit to be powered down and the oversampling to be switched off.

Table II. Input Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
01h	Input Mode Register	BTA T-1004 Compatibility								0	Disabled	38h
										1	Enabled	
		Reserved							0		Zero must be written to this bit.	
		Pixel Align						0			Video input data starts with a Y0 bit. Only for PS Interleaved Mode.	
								1			Video input data starts with a Cb0 bit.	
		Clock Align					0					
							1				Must be set if the phase delay between the two input clocks is <9.25 ns or >27.75 ns. Only if two input clocks are used.	
		Input Mode		0	0	0					SD Input Only	
				0	0	1					PS Input Only	
				0	1	0					HDTV Input Only	
				0	1	1					SD and PS (20-Bit)	
				1	0	0					SD and PS (10-Bit)	
				1	0	1					SD and HDTV (SD Oversampled)	
				1	1	0					SD and HDTV (HDTV Oversampled)	
				1	1	1					PS 54 MHz Input	
		Reserved	0								Zero must be written to this bit.	

Table III. Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
02h	Mode Register 0	Reserved							0	0	Zero must be written to these bits.	20h
		Test Pattern Black Bar						0			Disabled	
								1			Enabled. 0x11h, Bit 2 must also be enabled.	
		RGB Matrix					0				Disable Programmable RGB Matrix	
							1				Enable Programmable RGB Matrix	
		SYNC on RGB				0					No SYNC	
						1					SYNC on all RGB Outputs	
		RGB/YUV Output			0						RGB Component Outputs	
					1						YUV Component Outputs	
		SD SYNC		0							No SYNC Output	
				1							Output SD SYNCs on $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$	
		HD SYNC	0								No SYNC Output	
			1								Output HD SYNCs on $\overline{\text{S\_HSYNC}}$ and $\overline{\text{S\_VSYNC}}$	
03h	RGB Matrix 0								X	X	LSB for GY	03h
04h	RGB Matrix 1								X	X	LSB for RV	F0h
							X	X			LSB for BU	
					X	X					LSB for GV	
			X	X							LSB for GU	
05h	RGB Matrix 2		X	X	X	X	X	X	X	X	Bits 9–2 for GY	4Eh
06h	RGB Matrix 3		X	X	X	X	X	X	X	X	Bits 9–2 for GU	0Eh
07h	RGB Matrix 4		X	X	X	X	X	X	X	X	Bits 9–2 for GV	24h
08h	RGB Matrix 5		X	X	X	X	X	X	X	X	Bits 9–2 for BU	92h
09h	RGB Matrix 6		X	X	X	X	X	X	X	X	Bits 9–2 for RV	7Ch
0Ah	Reserved											00h
0Bh	Reserved											00h
0Ch	Reserved											00h
0Dh	Reserved											00h
0Eh	Reserved											00h
0Fh	Reserved											00h

Table IV. HD Mode Register

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
10h	HD Mode Register 1	HD Output Standard							0	0	EIA770.2 Output	00h
									0	1	EIA770.1 Output	
									1	0	Output Levels for Full Input Range	
									1	1	Reserved	
		HD Input Control Signals					0	0			$\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{BLANK}$	
							0	1			EAV/SAV Codes[1]	
		HD 625 p					1	0			Async Timing Mode	
							1	1			Reserved	
		HD 720 p				0					525 p	
						1					625 p	
		HD BLANK Polarity			0						1080 i	
					1						720 p	
		HD Macrovision for 525p/625 p		0							BLANK Active High	
				1							BLANK Active Low	
11h	HD Mode Register 2	HD Pixel Data Valid	0								Macrovision Off	00h
			1								Macrovision On	
										0	Pixel Data Valid Off	
		HD Test Pattern Enable								1	Pixel Data Valid On	
									0		Reserved	
		HD Test Pattern Hatch/Field						0			HD Test Pattern Off	
								1			HD Test Pattern On	
		HD VBI Open					0				Hatch	
							1				Field/Frame	
		HD Undershoot Limiter				0					Disabled	
						1					Enabled	
				0	0						Disabled	
				0	1						–11 IRE	
		HD Sharpness Filter		1	0						–6 IRE	
				1	1						–1.5 IRE	
12h	HD Mode Register 3	HD Y Delay wrt Falling Edge of HSYNC	0								Disabled	
			1								Enabled	
								0	0	0	0 Clock Cycle	
								0	0	1	1 Clock Cycle	
								0	1	0	2 Clock Cycle	
		HD Color Delay wrt Falling Edge of HSYNC						0	1	1	3 Clock Cycle	
								1	0	0	4 Clock Cycle	
					0	0	0				0 Clock Cycle	
					0	0	1				1 Clock Cycle	
					0	1	0				2 Clock Cycle	
		HD CGMS			0	1	1				3 Clock Cycle	
					1	0	0				4 Clock Cycle	
		HD CGMS CRC		0							Disabled	
				1							Enabled	

Table IV. HD Mode Register (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
13h	HD Mode Register 4	HD Cr/Cb Sequence[2]								0	Cb after Falling Edge of $\overline{\text{HSYNC}}$	4Ch
										1	Cr after Falling Edge of $\overline{\text{HSYNC}}$	
									0		Reserved	
		HD Input Format						0			8-Bit Input	
								1			10-Bit Input	
		Sync Filter on DAC D, E, F					0				Disabled	
							1				Enabled	
						0					Reserved	
		HD Chroma SSAF[2]			0						Disabled	
					1						Enabled	
		HD Chroma Input		0							4:4:4	
				1							4:2:2	
		HD Double Buffering	0								Disabled	
			1								Enabled	
14h	HD Mode Register 5		0	0	0	0	0	0	0	X	A low-high-low transition resets the internal HD timing counters.	00h
15h	HD Mode Register 6	Reserved								0	Zero must be written to this bit.	00h
		HD RGB Input							0		Disabled	
									1		Enabled	
		HD Sync on PrPb						0			Disabled	
								1			Enabled	
		HD Color DAC Swap[3]					0				DAC E = Pr, DAC F = Pb	
							1				DAC F = Pr, DAC E = Pb	
		HD Gamma Curve A/B				0					Gamma Curve A	
						1					Gamma Curve B	
		HD Gamma Curve Enable			0						Disabled	
					1						Enabled	
		HD Adaptive Filter Mode		0							Mode A	
				1							Mode B	
		HD Adaptive Filter Enable	0								Disabled	
			1								Enabled	

NOTES
[1]EAV/SAV codes are not supported for PS 1 × 10-Bit Interleaved Mode at 54 MHz.
[2]4:2:2 Input Format Only
[3]4:4:4 Input Format Only

Table V. Register Settings

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
16h	HD Y Color		X	X	X	X	X	X	X	X	Y Color Value	A0h
17h	HD Cr Color		X	X	X	X	X	X	X	X	Cr Color Value	80h
18h	HD Cb Color		X	X	X	X	X	X	X	X	Cb Color Value	80h
19h	Reserved											00h
1Ah	Reserved											00h
1Bh	Reserved											00h
1Ch	Reserved											00h
1Dh	Reserved											00h
1Eh	Reserved											00h
1Fh	Reserved											00h
20h	HD Sharpness Filter Gain	HD Sharpness Filter Gain Value A					0	0	0	0	Gain A = 0	00h
							0	0	0	1	Gain A = +1	
							…	…	…	…	…	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							…	…	…	…	…	
							1	1	1	1	Gain A = –1	
		HD Sharpness Filter Gain Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			…	…	…	…					…	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			…	…	…	…					…	
			1	1	1	1					Gain B = –1	
21h	HD CGMS Data 0	HD CGMS Data Bits	0	0	0	0	C19	C18	C17	C16	CGMS 19–16	00h
22h	HD CGMS Data 1	HD CGMS Data Bits	C15	C14	C13	C12	C11	C10	C9	C8	CGMS 15–8	00h
23h	HD CGMS Data 2	HD CGMS Data Bits	C7	C6	C5	C4	C3	C2	C1	C0	CGMS 7–0	00h
24h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A0	00h
25h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A1	00h
26h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A2	00h
27h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A3	00h
28h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A4	00h
29h	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A5	00h
2Ah	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A6	00h
2Bh	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A7	00h
2Ch	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A8	00h
2Dh	HD Gamma A	HD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A9	00h
2Eh	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B0	00h
2Fh	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B1	00h
30h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B2	00h
31h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B3	00h
32h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B4	00h
33h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B5	00h
34h	HD Gamma B	HD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B6	00h

Table VI. HD Adaptive Filters

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
38h	HD Adaptive Filter Gain 1	HD Adaptive Filter Gain 1 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 1 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
39h	HD Adaptive Filter Gain 2	HD Adaptive Filter Gain 2 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 2 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
3Ah	HD Adaptive Filter Gain 3	HD Adaptive Filter Gain 3 Value A					0	0	0	0	Gain A = 0	00hex
							0	0	0	1	Gain A = +1	
							0	1	1	1	Gain A = +7	
							1	0	0	0	Gain A = –8	
							1	1	1	1	Gain A = –1	
		HD Adaptive Filter Gain 3 Value B	0	0	0	0					Gain B = 0	
			0	0	0	1					Gain B = +1	
			0	1	1	1					Gain B = +7	
			1	0	0	0					Gain B = –8	
			1	1	1	1					Gain B = –1	
3Bh	HD Adaptive Filter Threshold A	HD Adaptive Filter Threshold A Value	X	X	X	X	X	X	X	X	Threshold A	00hex
3Ch	HD Adaptive Filter Threshold B	HD Adaptive Filter Threshold B Value	X	X	X	X	X	X	X	X	Threshold B	00hex
3Dh	HD Adaptive Filter Threshold C	HD Adaptive Filter Threshold C Value	X	X	X	X	X	X	X	X	Threshold C	00hex

Table VII. SD Mode Registers

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
3Eh	Reserved											00h
3Fh	Reserved											00h
40h	SD Mode Register 0	SD Standard							0	0	NTSC	00h
									0	1	PAL B, D, G, H, I	
									1	0	PAL M	
									1	1	PAL N	
		SD Luma Filter				0	0	0			LPF NTSC	
						0	0	1			LPF PAL	
						0	1	0			Notch NTSC	
						0	1	1			Notch PAL	
						1	0	0			SSAF Luma	
						1	0	1			Luma CIF	
						1	1	0			Luma QCIF	
						1	1	1			Reserved	
		SD Chroma Filter	0	0	0						1.3 MHz	
			0	0	1						0.65 MHz	
			0	1	0						1.0 MHz	
			0	1	1						2.0 MHz	
			1	0	0						Reserved	
			1	0	1						Chroma CIF	
			1	1	0						Chroma QCIF	
			1	1	1						3.0 MHz	
41h	Reserved											00h
42h	SD Mode Register 1	SD UV SSAF								0	Disabled	08h
										1	Enabled	
		SD DAC Output 1*							0		DAC A, B, C: CVBS, L, C; DAC D, E, F: GBR or YUV	
									1		DAC A, B, C: GBR or YUV; DAC D, E, F: CVBS, L, C	
		SD DAC Output 2						0			Swap DAC A and DAC D Outputs	
								1				
		SD Pedestal					0				Disabled	
							1				Enabled	
		SD Square Pixel				0					Disabled	
						1					Enabled	
		SD VCR FF/RW Sync			0						Disabled	
					1						Enabled	
		SD Pixel Data Valid		0							Disabled	
				1							Enabled	
		SD Active Video Edge	0								Disabled	
			1								Enabled	

Table VII. SD Mode Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
43h	SD Mode Register 2	SD Pedestal YUV Output								0	No Pedestal on YUV	00h
										1	7.5 IRE Pedestal on YUV	
		SD Output Levels Y							0		Y = 700 mV/300 mV	
									1		Y = 714 mV/286 mV	
		SD Output Levels UV					0	0			700 mV p-p [PAL]; 1000 mV p-p [NTSC]	
							0	1			700 mV p-p	
							1	0			1000 mV p-p	
							1	1			648 mV p-p	
		SD VBI Open				0					Disabled	
						1					Enabled	
		SD CC Field Control		0	0						CC Disabled	
				0	1						CC on Odd Field Only	
				1	0						CC on Even Field Only	
				1	1						CC on Both Fields	
			1								Reserved	
44h	SD Mode Register 3	SD VSYNC-3H								0	Disabled	00h
										1	VSYNC = 2.5 lines [PAL]; VSYNC = 3 lines [NTSC]	
		SD RTC/TR/SCR						0	0		Genlock Disabled	
								0	1		Subcarrier Reset	
								1	0		Timing Reset	
								1	1		RTC Enabled	
		SD Active Video Length					0				720 Pixels	
							1				710 (NTSC); 702(PAL)	
		SD Chroma				0					Chroma Enabled	
						1					Chroma Disabled	
		SD Burst			0						Enabled	
					1						Disabled	
		SD Color Bars		0							Disabled	
				1							Enabled	
		Reserved	0								Zero must be written to this bit.	
45h	Reserved											00h
46h	Reserved											00h
47h	SD Mode Register 4	SD UV Scale								0	Disabled	00h
										1	Enabled	
		SD Y Scale							0		Disabled	
									1		Enabled	
		SD Hue Adjust						0			Disabled	
								1			Enabled	
		SD Brightness					0				Disabled	
							1				Enabled	
		SD Luma SSAF Gain				0					Disabled	
						1					Enabled	
		Reserved			0						Zero must be written to this bit.	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

Table VII. SD Mode Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
48h	SD Mode Register 5	Reserved								0	Zero must be written to this bit.	
		Reserved							0		Zero must be written to this bit.	00h
		SD Double Buffering						0			Disabled	
								1			Enabled	
		SD Input Format				0	0				8-Bit Input	
						0	1				16-Bit Input	
						1	0				10-Bit Input	
						1	1				20-Bit Input	
		SD Digital Noise Reduction			0						Disabled	
					1						Enabled	
		SD Gamma Control		0							Disabled	
				1							Enabled	
		SD Gamma Curve	0								Gamma Curve A	
			1								Gamma Curve B	
49h	SD Mode Register 6	SD Undershoot Limiter							0	0	Disabled	00h
									0	1	–11 IRE	
									1	0	–6 IRE	
									1	1	–1.5 IRE	
		SD Black Burst Output on DAC Y						0			Disabled	
								1			Enabled	
		SD Black Burst Output on DAC Luma					0				Disabled	
							1				Enabled	
		SD Chroma Delay			0	0					Disabled	
					0	1					4 Clock Cycles	
					1	0					8 Clock Cycles	
					1	1					Reserved	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

*For more detail, see Input and Output Configuration section.

Table VIII. SD Registers

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
4Ah	SD Timing Register 0	SD Slave/Master Mode								0	Slave Mode	08h
										1	Master Mode	
		SD Timing Mode						0	0		Mode 0	
								0	1		Mode 1	
								1	0		Mode 2	
								1	1		Mode 3	
		SD BLANK Input					0				Enabled	
							1				Disabled	
		SD Luma Delay			0	0					No Delay	
					0	1					2 Clock Cycles	
					1	0					4 Clock Cycles	
					1	1					6 Clock Cycles	
		SD Min. Luma Value		0							–40 IRE	
				1							–7.5 IRE	
		SD Timing Reset	X	0	0	0	0	0	0	0	A low-high-low transistion will reset the internal SD timing counters.	
4Bh	SD Timing Register 1	SD $\overline{\text{HSYNC}}$ Width							0	0	Ta = 1 Clock Cycle	00h
									0	1	Ta = 4 Clock Cycles	
									1	0	Ta = 16 Clock Cycles	
									1	1	Ta = 128 Clock Cycles	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Delay					0	0			Tb = 0 Clock Cycle	
							0	1			Tb = 4 Clock Cycles	
							1	0			Tb = 8 Clock Cycles	
							1	1			Tb = 18 Clock Cycles	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Rising Edge Delay (Mode 1 Only); $\overline{\text{VSYNC}}$ Width (Mode 2 Only)			X	0					Tc = Tb	
					X	1					Tc = Tb + 32 µs	
					0	0					1 Clock Cycle	
					0	1					4 Clock Cycles	
					1	0					16 Clock Cycles	
					1	1					128 Clock Cycles	
		$\overline{\text{HSYNC}}$ to Pixel Data Adjust	0	0							0 Clock Cycle	
			0	1							1 Clock Cycle	
			1	0							2 Clock Cycles	
			1	1							3 Clock Cycles	
4Ch	SD F_{SC} Register 0		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 7–0	16h
4Dh	SD F_{SC} Register 1		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 15–8	7Ch
4Eh	SD F_{SC} Register 2		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 23–16	F0h
4Fh	SD F_{SC} Register 3		X	X	X	X	X	X	X	X	Subcarrier Frequency Bits 31–24	21h
50h	SD F_{SC} Phase		X	X	X	X	X	X	X	X	Subcarrier Phase Bits 9–2	00h
51h	SD Closed Captioning	Extended Data on Even Fields	X	X	X	X	X	X	X	X	Extended Data Bits 7–0	00h
52h	SD Closed Captioning	Extended Data on Even Fields	X	X	X	X	X	X	X	X	Extended Data Bits 15–8	00h
53h	SD Closed Captioning	Data on Odd Fields	X	X	X	X	X	X	X	X	Data Bits 7–0	00h
54h	SD Closed Captioning	Data on Odd Fields	X	X	X	X	X	X	X	X	Data Bits 15–8	00h
55h	SD Pedestal Register 0	Pedestal on Odd Fields	17	16	15	14	13	12	11	10	Setting any of these bits to 1 will disable pedestal on the line number indicated by the bit settings.	00h
56h	SD Pedestal Register 1	Pedestal on Odd Fields	25	24	23	22	21	20	19	18		00h
57h	SD Pedestal Register 2	Pedestal on Even Fields	17	16	15	14	13	12	11	10		00h
58h	SD Pedestal Register 3	Pedestal on Even Fields	25	24	23	22	21	20	19	18		00h

Table VIII. SD Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
59h	SD CGMS/WSS 0	SD CGMS Data					19	18	17	16	CGMS Data Bits C19–C16	00h
		SD CGMS CRC				0					Disabled	
						1					Enabled	
		SD CGMS on Odd Fields			0						Disabled	
					1						Enabled	
		SD CGMS on Even Fields		0							Disabled	
				1							Enabled	
		SD WSS	0								Disabled	
			1								Enabled	
5Ah	SD CGMS/WSS 1	SD CGMS/WSS Data			13	12	11	10	9	8	CGMS Data Bits C13–C8 or WSS Data Bits C13–C8	00h
			15	14							CGMS Data Bits C15–C14	
5Bh	SD CGMS/WSS 2	SD CGMS/WSS Data	7	6	5	4	3	2	1	0	CGMS/WSS Data Bits C7–C0	00h
5Ch	SD LSB Register	SD LSB for Y Scale Value							X	X	SD Y Scale Bits 1–0	
		SD LSB for U Scale Value					X	X			SD U Scale Bits 1–0	
		SD LSB for V Scale Value			X	X					SD V Scale Bits 1–0	
		SD LSB for F_{SC} Phase	X	X							Subcarrier Phase Bits 1–0	
5Dh	SD Y Scale Register	SD Y Scale Value	X	X	X	X	X	X	X	X	SD Y Scale Bits 7–2	00h
5Eh	SD V Scale Register	SD V Scale Value	X	X	X	X	X	X	X	X	SD V Scale Bits 7–2	00h
5Fh	SD U Scale Register	SD U Scale Value	X	X	X	X	X	X	X	X	SD U Scale Bits 7–2	00h
60h	SD Hue Register	SD Hue Adjust Value	X	X	X	X	X	X	X	X	SD Hue Adjust Bits 7–0	00h
61h	SD Brightness/WSS	SD Brightness Value		X	X	X	X	X	X	X	SD Brightness Bits 6–0	00h
		SD Blank WSS Data*	0								Disabled	
			1								Enabled	
62h	SD Luma SSAF	SD Luma SSAF Gain/Attenuation	0	0	0	0	0	0	0	0	–4 dB	00h
			0	0	0	0	0	1	1	0	0 dB	
			0	0	0	0	1	1	0	0	+4 dB	
63h	SD DNR 0	Coring Gain Border					0	0	0	0	No Gain	00h
							0	0	0	1	+1/16 (–1/8 in DNR Mode)	
							0	0	1	0	+2/16 (–2/8 in DNR Mode)	
							0	0	1	1	+3/16 (–3/8 in DNR Mode)	
							0	1	0	0	+4/16 (–4/8 in DNR Mode)	
							0	1	0	1	+5/16 (–5/8 in DNR Mode)	
							0	1	1	0	+6/16 (–6/8 in DNR Mode)	
							0	1	1	1	+7/16 (–7/8 in DNR Mode)	
							1	0	0	0	+8/16 (–1 in DNR Mode)	
		Coring Gain Data	0	0	0	0					No Gain	
			0	0	0	1					+1/16 (–1/8 in DNR Mode)	
			0	0	1	0					+2/16 (–2/8 in DNR Mode)	
			0	0	1	1					+3/16 (–3/8 in DNR Mode)	
			0	1	0	0					+4/16 (–4/8 in DNR Mode)	
			0	1	0	1					+5/16 (–5/8 in DNR Mode)	
			0	1	1	0					+6/16 (–6/8 in DNR Mode)	
			0	1	1	1					+7/16 (–7/8 in DNR Mode)	
			1	0	0	0					+8/16 (–1 in DNR Mode)	

Table VIII. SD Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
64h	SD DNR 1	DNR Threshold			0	0	0	0	0	0	0	00h
					0	0	0	0	0	1	1	
					1	1	1	1	1	0	62	
					1	1	1	1	1	1	63	
		Border Area		0							2 Pixels	
				1							4 Pixels	
		Block Size Control	0								8 Pixels	
			1								16 Pixels	
65h	SD DNR 2	DNR Input Select						0	0	1	Filter A	00h
								0	1	0	Filter B	
								0	1	1	Filter C	
								1	0	0	Filter D	
		DNR Mode					0				DNR Mode	
							1				DNR Sharpness Mode	
		DNR Block Offset	0	0	0	0					0 Pixel Offset	
			0	0	0	1					1 Pixel Offset	
			1	1	1	0					14 Pixel Offset	
			1	1	1	1					15 Pixel Offset	
66h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A0	00h
67h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A1	00h
68h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A2	00h
69h	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A3	00h
6Ah	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A4	00h
6Bh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A5	00h
6Ch	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A6	00h
6Dh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A7	00h
6Eh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A8	00h
6Fh	SD Gamma A	SD Gamma Curve A Data Points	X	X	X	X	X	X	X	X	A9	00h
70h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B0	00h
71h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B1	00h
72h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B2	00h
73h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B3	00h
74h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B4	00h
75h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B5	00h
76h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B6	00h
77h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B7	00h
78h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B8	00h
79h	SD Gamma B	SD Gamma Curve B Data Points	X	X	X	X	X	X	X	X	B9	00h
7Ah	SD Brightness Detect	SD Brightness Value	X	X	X	X	X	X	X	X	Read-Only	
7Bh	Field Count Register	Field Count						X	X	X	Read-Only	
		Reserved					0				Zero must be written to this bit.	
		Reserved				0					Zero must be written to this bit.	
		Reserved			0						Zero must be written to this bit.	
		Reserved Code	X	X							Read-Only	

Table VIII. SD Registers (continued)

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
7Ch	Reset Register	Timing Reset								0	No reset of Timing Generator in Subcarrier Reset Mode. 44h, Bits 1 and 2 must be set to Subcarrier Reset.	00h
										1	Reset Timing Generator in Subcarrier Reset Mode	
		Reserved							0		Zero must be written to this bit.	
		Reserved						0			Zero must be written to this bit.	
		Reserved					0				Zero must be written to this bit.	
		Reserved				0					Zero must be written to this bit.	
		Reserved			0						Zero must be written to this bit.	
		Reserved		0							Zero must be written to this bit.	
		Reserved	0								Zero must be written to this bit.	

*Line 23

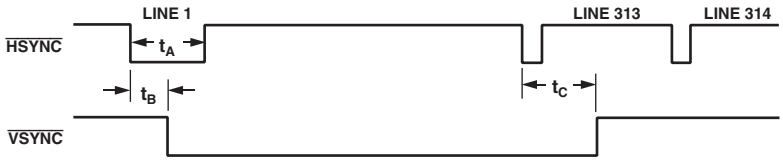


Figure 19. Timing Register 1 in PAL Mode

Table IX. Macrovision Registers*

Subaddress	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset
7Dh	Reserved											
7Eh	Reserved											
7Fh	Reserved											
80h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3a [7:0]	00h
81h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3b [15:8]	00h
82h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3c [23:16]	00h
83h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3d [31:24]	00h
84h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3e [39:32]	00h
85h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 3f [47:40]	00h
86h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 40 [55:48]	00h
87h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 41 [63:56]	00h
88h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 42 [71:64]	00h
89h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 43 [79:72]	00h
8Ah	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 44 [87:80]	00h
8Bh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 45 [95:88]	00h
8Ch	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 46 [103:96]	00h
8Dh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 47 [111:104]	00h
8Eh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 48 [119:112]	00h
8Fh	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 49 [127:120]	00h
90h	Macrovision	MV Control Bits	X	X	X	X	X	X	X	X	MV 4A [135:128]	00h
91h	Macrovision	MV Control Bit								X	MV 4B [136]	00h
			0	0	0	0	0	0	0		Zero must be written to these bits.	

*Macrovision Registers are only available on the ADV7304A.

INPUT AND OUTPUT CONFIGURATION
STANDARD DEFINITION ONLY

The 8- or 10-bit multiplexed input data is input on Pins S9–S0, with S0 being the LSB in 10-bit Input Mode. For 8-bit Input Mode, the data is input on Pins S9–S2. ITU-R.BT601/ITU-R.BT656 input standards are supported. In 16-bit Input Mode, the Y pixel data is input on Pins S9–S2 and CrCb data on Pins Y9–Y2. In 20-bit Input Mode, the Y pixel data is input on S9–S0 and CrCb pixel data on Pins Y9–Y0. The 27 MHz clock input must be input on Pin CLKIN_A. Input sync signals are optional and are input on the S_VSYNC, S_HSYNC, and S_BLANK pins.

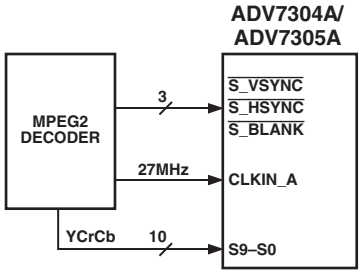


Figure 20. Standard Definition Only Input Mode

PROGRESSIVE SCAN ONLY OR HDTV ONLY

YCrCb Progressive Scan, HDTV, or any other HD YCrCb data can be input in 4:2:2 or 4:4:4 format. In 4:2:2 Input Mode, the Y data is input on Pins Y9–Y0 and the CrCb data on Pins C9–C0. In 4:4:4 Input Mode, Y data is input on Pins Y9–Y0, Cb data on Pins C9–C0, and Cr data on Pins S9–S0. If the YCrCb data does not conform to SMPTE293M (525 p), ITU-R.BT1358M (625 p), SMPTE274M (1080 i), SMPTE296M (720 p), or BTA-T1004, the Async Timing Mode must be used. RGB data can only be input in 4:4:4 format in PS Input Mode only, or HDTV Input Mode only, when HD RGB input is enabled. G data is input on Pins Y9–Y0, R data on S9–S0, and B data on Pins C9–C0. The clock signal must be input on Pin CLKIN_A. Synchronization signals are optional and are input on Pins P_VSYNC, P_HSYNC, and P_BLANK.

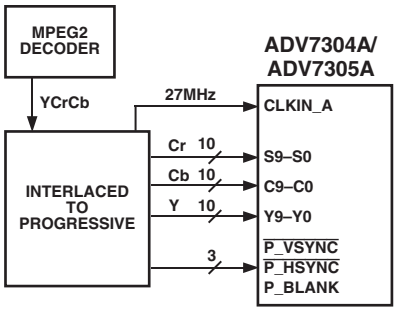


Figure 21. Progressive Scan Only Input Mode

SIMULTANEOUS STANDARD DEFINITION AND PROGRESSIVE SCAN OR HDTV

YCrCb PS, HDTV, or any other HD data must be input in 4:2:2 format. In 4:2:2 Input Mode, the Y data is input on Pins Y9–Y0 and the CrCb data on C9–C0. If PS 4:2:2 data is interleaved onto a single 10-bit bus, Pins Y9–Y0 are used for the Input Port. The interleaved data is to be input at 27 MHz in setting the Input Mode Register at Address 01h accordingly. If the YCrCb data does not conform to SMPTE293M (525 p), ITU-R.BT1358M (625 p), SMPTE274M (1080 i), SMPTE296M (720 p), or BTA-T1004, the Async Timing Mode must be used.

The 8- or 10-bit standard definition data must be compliant to ITU-R.BT601/ITU-R.BT656 in 4:2:2 format. Standard definition data is input on Pins S9–S0, with S0 being the LSB. Using 8-bit input format, the data is input on Pins S9–S2. The clock input for SD must be input on CLKIN_A, and the clock input for HD must be input on CLKIN_B. Synchronization signals are optional. SD syncs are input on Pins S_VSYNC, S_HSYNC, and S_BLANK; the HD syncs on Pins P_VSYNC, P_HSYNC, and P_BLANK.

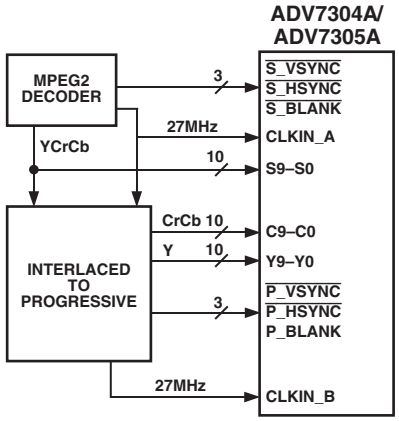


Figure 22. Simultaneous Progressive Scan and SD Input

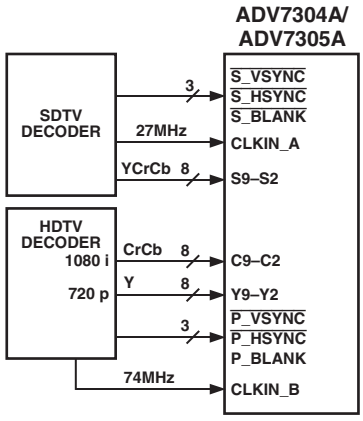


Figure 23. Simultaneous HDTV and SD Input

If in Simultaneous Input Mode the two clock phases differ by less than 9.25 ns or more than 27.75 ns, the Clock Align Bit must be set accordingly. This also applies if the Pixel Align Bit is set. If the application uses the same clock source for both SD and PS, the Clock Align Bit must be set since the phase difference between both inputs is less than 9.25 ns.

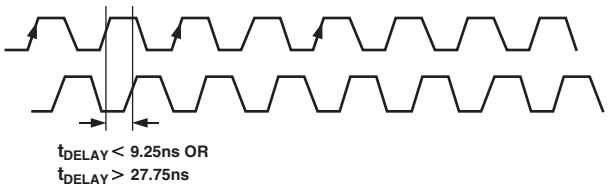


Figure 24. Clock Phase with Two Input Clocks

PROGRESSIVE SCAN AT 27 MHz OR 54 MHz

YCrCb progressive scan data can be input at 27 MHz or 54 MHz. The input data is interleaved onto a single 10-bit bus and is input on Pins Y9–Y0. For PS Input Only Mode, the input clock must be input on CLKIN_A. In Simultaneous SD/HD Mode, the input clock is input on CLKIN_B.

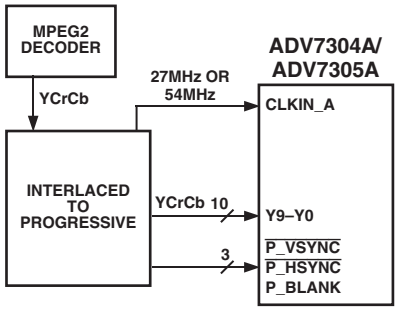


Figure 25. 1 × 10-Bit PS @ 27 MHz or 54 MHz

When the input sequence of the PS data, i.e., 10-bit interleaved at 27 MHz, starts with Y0 data, as shown in Figure 26, PIXEL ALIGN [Subaddress 01h] must be set to "0." In this case, the timing information embedded in the data stream is recognized and the video data is transferred to the according Y channel and CrCb channel processing blocks.

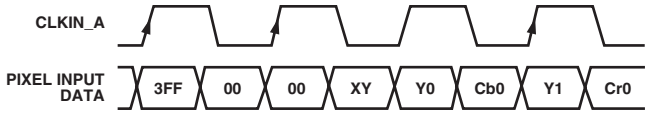


Figure 26. Input Sequence in PS 10-Bit Interleaved Mode, EAV/SAV Followed by Y0 Data

If the input sequence starts with Cb0 data as shown in Figure 27, initially PIXEL ALIGN [Subaddress 01h] must be set to "0." This ensures that the ADV7304A/ADV7305A locks to the input sequence in decoding the embedded timing information correctly. For correct color decoding, the Pixel Align Bit [Subaddress 01h] must then be set to "l" after a delay of one field. The ADV7304A/ADV7305A is now in Free Run Mode, any changes in the timing information are ignored.

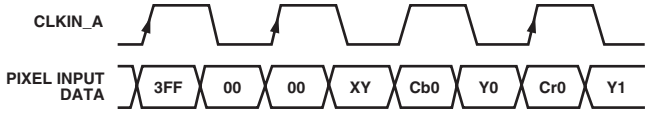


Figure 27. Input Sequence in PS 10-Bit Interleaved Mode, EAV/SAV Followed by Cb0 Data

PS 10-bit interleaved at 54 MHz must be input with separate timing signals. EAV/SAV codes cannot be used in this mode.

Table X. Overview of All Possible Input Configurations

Input Format	Total Bits		Input Video	Input Pins	Subaddress	Register Setting
ITU-R.BT656	8	4:2:2	YCrCb	S9–S2 [MSB = S9]	01h, 48h	00h, 00h
	10	4:2:2	YCrCb	S9–S0 [MSB = S9]	01h, 48h	00h, 10h
	16	4:2:2	Y	S9–S2 [MSB = S9]	01h, 48h	00h, 08h
			CrCb	Y9–Y2 [MSB = Y9]		
	20	4:2:2	Y	S9–S0 [MSB = S9]	01h, 48h	00h, 18h
			CrCb	Y9–Y0 [MSB = Y9]		
PS Only	8 (27 MHz Clock)	4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	01h, 13h	10h, 40h
	10 (27 MHz Clock)	4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 44h
	8 (54 MHz Clock)	4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	01h, 13h	70h, 40h
	10 (54 MHz Clock)	4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 44h
	16	4:2:2	Y	Y9–Y2 [MSB = Y9]	01h, 13h	10h, 40h
			CrCb	C9–C2 [MSB = C9]		
	20	4:2:2	Y	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 44h
			CrCb	C9–C0 [MSB = C9]		
	24	4:4:4	Y	Y9–Y2 [MSB = Y9]	01h, 13h	10h, 00h
			Cb	C9–C2 [MSB = C9]		
			Cr	S9–S2 [MSB = S9]		
	30	4:4:4	Y	Y9–Y0 [MSB = Y9]	01h, 13h	10h, 04h
			Cb	C9–C0 [MSB= C9]		
			Cr	S9–S0 [MSB = S9]		
HDTV Only	8	4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	01h, 13h	20h, 40h
	10	4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	01h, 13h	20h, 44h
	16	4:2:2	Y	Y9–Y2 [MSB = Y9]	01h, 13h	20h, 40h
			CrCb	C9–Y2 [MSB = C9]		
	20	4:2:2	Y	Y9–Y0 [MSB = Y9]	01h, 13h	20h, 44h
			CrCb	C9–C0 [MSB = C9]		
	24	4:4:4	Y	Y9–Y2 [MSB = Y9]	01h, 13h	20h, 00h
			Cb	C9–Y2 [MSB = C9]		
			Cr	S9–S2 [MSB = S9]		
	30	4:4:4	Y	Y9–Y0 [MSB = Y9]	01h, 13h	20h, 04h
			Cb	C9–C0 [MSB = C9]		
			Cr	S9–S0 [MSB = S9]		
HD RGB	24	4:4:4	G	Y9–Y2 [MSB = Y9]	01h, 13h, 15h	10h or 20h, 00h, 02h
			B	C9–C2 [MSB = C9]		
			R	S9–S2 [MSB = S9]		
	30	4:4:4	G	Y9–Y0 [MSB = Y9]	01h, 13h, 15h	10h or 20h, 04h, 02h
			B	C9–C0 [MSB = C9]		
			R	S9–S0 [MSB = S9]		
ITU-R.BT656 and PS	SD 8	4:2:2	YCrCb	S9–S2 [MSB = S9]	01h	40h
	PS 8	4:2:2	YCrCb	Y9–Y2 [MSB = Y9]	13h	40h
					48h	00h
	SD 10	4:2:2	YCrCb	S9–S0 [MSB = S9]	01h	40h
	PS 10	4:2:2	YCrCb	Y9–Y0 [MSB = Y9]	13h	44h
					48h	10h
ITU-R.BT656 and PS or HDTV	SD 8	4:2:2	YCrCb	S9–S2 [MSB = S9]	01h	30h, 50h, or 60h
	HD 16	4:2:2	Y	Y9–Y2 [MSB = Y9]	13h	40h
			CrCb	C9–C2 [MSB = C9]	48h	00h
	SD 10	4:2:2	YCrCb	S9–S0 [MSB = S9]	01h	30h, 50h, or 60h
	HD 20	4:2:2	Y	Y9–Y0 [MSB = Y9]	13h	44h
			CrCb	C9–C0 [MSB = C9]	48h	10h

OUTPUT CONFIGURATION

Tables XI–XIII demonstrate what output signals are assigned to the DACs when corresponding control bits are set.

Table XI. Output Configuration in SD Only Mode

RGB/YUV O/P Addr 02h, Bit 5	SD DAC O/P 1 Addr 42h, Bit 2	SD DAC O/P 2 Addr 42h, Bit 1	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
0	0	0	CVBS	Luma	Chroma	G	B	R
0	0	1	G	B	R	CVBS	Luma	Chroma
0	1	0	G	Luma	Chroma	CVBS	B	R
0	1	1	CVBS	B	R	G	Luma	Chroma
1	0	0	CVBS	Luma	Chroma	Y	U	V
1	0	1	Y	U	V	CVBS	Luma	Chroma
1	1	0	Y	Luma	Chroma	CVBS	U	V
1	1	1	CVBS	U	V	Y	Luma	Chroma

Table XII. Output Configuration in HD Only Mode

HD I/P Format	HD RGB I/P Addr 15h, Bit 1	RGB/YUV O/P Addr 02h, Bit 5	HD Color Swap Addr 15h, Bit 3	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
YCrCb 4:2:2	N/A	0	0	N/A	N/A	N/A	G	B	R
YCrCb 4:2:2	N/A	0	1	N/A	N/A	N/A	G	R	B
YCrCb 4:2:2	N/A	1	0	N/A	N/A	N/A	Y	Pb	Pr
YCrCb 4:2:2	N/A	1	1	N/A	N/A	N/A	Y	Pr	Pb
YCrCb 4:4:4	N/A	0	0	N/A	N/A	N/A	G	B	R
YCrCb 4:4:4	N/A	0	1	N/A	N/A	N/A	G	R	B
YCrCb 4:4:4	N/A	1	0	N/A	N/A	N/A	Y	Pb	Pr
YCrCb 4:4:4	N/A	1	1	N/A	N/A	N/A	Y	Pr	Pb
RGB 4:4:4	1	0	0	N/A	N/A	N/A	G	B	R
RGB 4:4:4	1	0	1	N/A	N/A	N/A	G	R	B
RGB 4:4:4	1	1	0	N/A	N/A	N/A	G	B	R
RGB 4:4:4	1	1	1	N/A	N/A	N/A	G	R	B

Table XIII. Output Configuration in Simultaneous SD/HD Mode

Input Formats	RGB/YUV O/P Addr 02h, Bit 5	HD Color Swap Addr 15h, Bit 3	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	0	0	CVBS	Luma	Chroma	G	B	R
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	0	1	CVBS	Luma	Chroma	G	R	B
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	1	0	CVBS	Luma	Chroma	Y	Pb	Pr
SD YCrCb in 4:2:2 and HD YCrCb in 4:2:2	1	1	CVBS	Luma	Chroma	Y	Pr	Pb

TIMING MODES

HD Async Timing Mode
[Subaddress 10h, Bits 3–2]

For any input data that does not conform to SMPTE293M, SMPTE274M, SMPTE296M, or ITU-R.BT1358 standards, an Asynchronous Timing Mode can be used to interface to the ADV7304A/ADV7305A. Timing control signals for HSYNC, VSYNC, and BLANK have to be programmed by the user. Macrovision is not available in Async Timing Mode.

Figure 28 shows an example of how to program the ADV7304A/ADV7305A to accept a different high definition standard other than SMPTE293M, SMPTE274M, SMPTE296M, or ITU-R.BT1358 standards.

Table XIV must be followed when programming the control signals in Async Timing Mode.

HD Timing Reset

A timing reset is achieved in setting the HD Timing Reset Control Bit at Address 14h from "0" to "1." In this state, the horizontal and vertical counters will remain reset. On setting this bit back to "0," the internal counters will again commence counting. The minimum time the pin has to be held high is one clock cycle; otherwise, this reset signal might not be recognized. This timing reset applies to the HD timing counters only.

SD Timing
Realtime Control, Subcarrier Reset, Timing Reset
[Subaddress 44h, Bits 2–1]

Together with the RTC_SCR_TR pin and SD Mode Register 3 [Address 44h, Bits 1–2], the ADV7304A/ADV7305A can be used in Timing Reset Mode, Subcarrier Phase Reset Mode, or RTC Mode.

a. A timing reset is achieved in a low-to-high transition on the RTC_SCR_TR pin (Pin 31). In this state, the horizontal and vertical counters will remain reset. On releasing this pin (set to low), the internal counters will again commence counting. The minimum time the pin has to be held high is one clock cycle; otherwise, this reset signal might not be recognized. This timing reset applies to the SD timing counters only.

b. Subcarrier phase reset, a low-to-high transition on the RTC_SCR_TR pin (Pin 31), will reset the subcarrier phase to zero when the SD RTC/TR/SCR control bits at Address 44h are set to "01." This reset signal will have to be held high for a minimum of one clock cycle. Since the Field Counter is not reset, it is recommended to apply the reset in Field 7 (PAL). The reset of the phase will then occur on the next field by being correctly lined up with the internal counters. The Field Count Register at Address 7Bh can be used to identify the number of the active field.

c. In RTC Mode, the ADV7304A/ADV7305A can be used to lock to an external video source. The Realtime Control Mode allows the ADV7304A/ADV7305A to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device that outputs a digital data stream in the RTC format (such as a ADV7185 video decoder, see Figure 29), the part will automatically change to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. 00h should be written into all four Subcarrier Frequency Registers when using this mode.

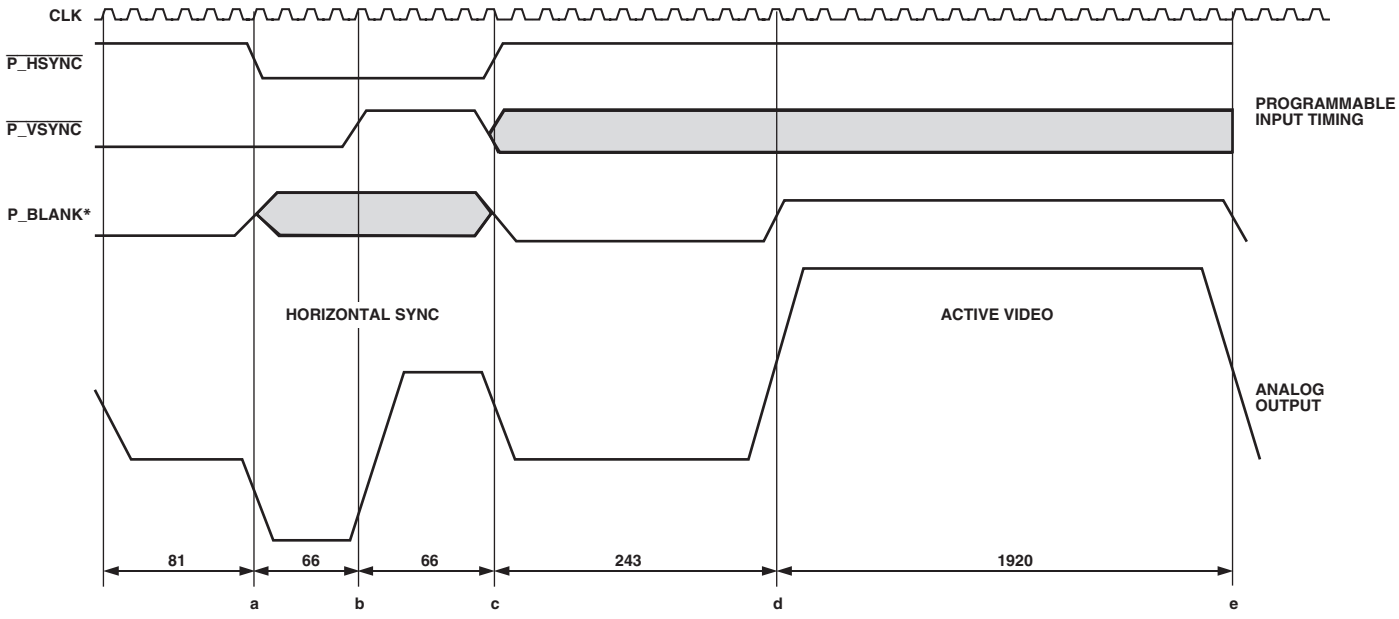
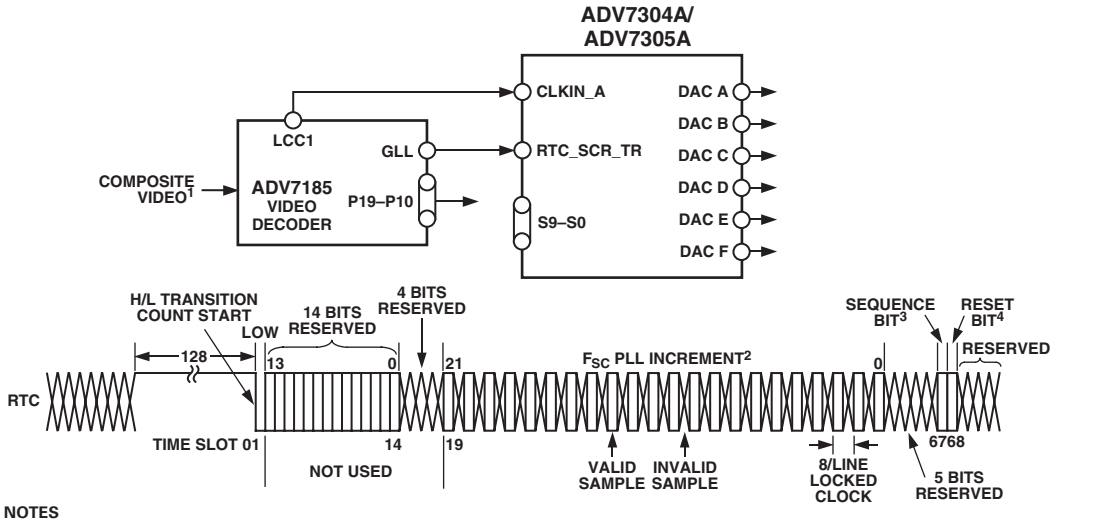


Figure 28. Async Timing Mode, Programming Input Control Signals for SMPTE295M Compatibility

Table XIV. Truth Table

$\overline{\text{P\_HSYNC}}$	$\overline{\text{P\_VSYNC}}$[1]	P_BLANK[1]		Reference[2]
1 → 0	0	0 or 1	50% point of falling edge of tri-level horizontal sync signal	a
0	0 → 1	0 or 1	25% point of rising edge of tri-level horizontal sync signal	b
0 → 1	0 or 1	0	50% point of falling edge of tri-level horizontal sync signal	c
1	0 or 1	0 → 1	50% start of active video	d
1	0 or 1	1 → 0	50% end of active video	e

NOTES
For standards that do not require a tri-sync level, P_BLANK must be tied low at all times.
[1]When Async Timing Mode is enabled, P_BLANK, Pin 25 becomes an active high input. P_BLANK is set to active low at Address 10h, Bit 6.
[2]See Figure 28.



NOTES
[1]i.e., VCR OR CABLE
[2]F_{SC} PLL INCREMENT IS 22 BITS LONG. VALUED LOADED INTO ADV7304A/ADV7305A F_{SC} DDS REGISTER IS F_{SC} PLL INCREMENTS BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7304A/ADV7305A.
[3]PAL: 0 = LINE NORMAL, 1 = LINE INVERTED; NTSC: 0 = NO CHANGE
[4]RESET ADV7304A/ADV7305A DDS

Figure 29. RTC Timing and Connections

SD VCR FF/RW Sync
[Subaddress 42h, Bit 5]
In DVD record applications where the encoder is used with a decoder, the VCR FF/RW Sync Control Bit can be used for nonstandard input video, i.e., in Fast Forward or Rewind Modes. In Fast Forward Mode, the sync information for the start of a new field in the incoming video usually occurs before the total number of lines/fields are reached; in Rewind Mode, this sync signal occurs usually after the total number of lines/fields are reached. Conventionally, this means that the output video will have an erroneous start of new field signals, one generated by the incoming video and one when the internal lines/field counters reach the end of a field. When VCR FF/RW sync control is enabled [Subaddress 42h, Bit 5], the lines/field counters are updated according to the incoming VSYNC signal, and the analog output matches the incoming VSYNC signal.

This control is available in all slave timing modes except Slave Mode 0.

RESET SEQUENCE
A reset is activated with a high-to-low transition on the $\overline{\text{RESET}}$ pin (Pin 33) according to the timing specifications. The ADV7304A/ADV7305A will revert to the default output configuration. Figure 30 illustrates the $\overline{\text{RESET}}$ sequence timing.

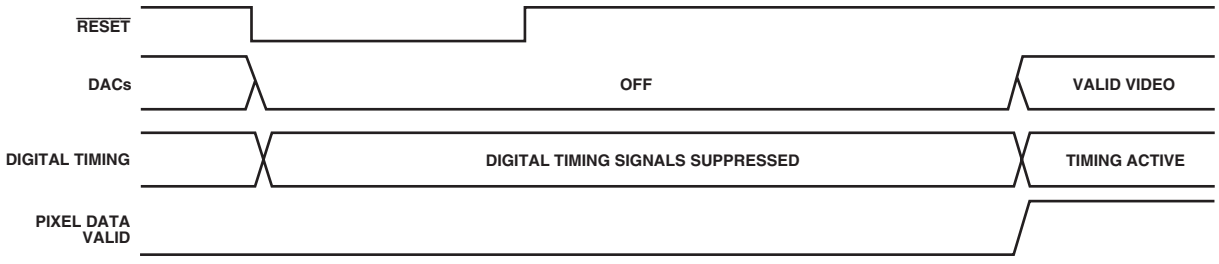


Figure 30. $\overline{\text{RESET}}$ Timing Sequence

VERTICAL BLANKING INTERVAL

The ADV7304A/ADV7305A accepts input data that contains VBI data (CGMS, WSS, VITS, and so on) in SD and HD Modes.

For SMPTE293M (525 p) standards, VBI data can be inserted on Lines 13 to 42 of each frame, or Lines 6 to 43 for ITU-R.BT1358 (625 p) standard.

For SD NTSC, this data can be present on Lines 10 to 20; in PAL, on Lines 7 to 22.

If VBI is disabled [Address 11h, Bit 4 for HD; Address 43h, Bit 4 for SD], VBI data is not present at the output and the entire VBI is blanked. These control bits are valid in all master and slave modes.

In Slave Mode 0, if VBI is enabled, the Blanking Bit in the EAV/SAV code is overwritten and it is possible to use VBI in this timing mode as well.

In Slave Mode 1 or 2, the $\overline{\text{BLANK}}$ Control Bit must be set to enabled [Address 4Ah, Bit 3] to allow VBI data to pass through the ADV7304A/ADV7305A. Otherwise, the ADV7304A/ADV7305A automatically blanks the VBI to standard.

If CGMS is enabled and VBI disabled, the CGMS data will nevertheless be available at the output.

SD SUBCARRIER FREQUENCY REGISTERS

[Subaddress 4Ch–4Fh]

Four 8-bit wide registers are used to set up the subcarrier frequency. The value of these registers is calculated in using the equation:

$$\textit{Subcarrier Frequency Register} = \frac{\#\textit{ of Subcarrier Frequency Cycles in One Video Line}}{\#\textit{ of 27 MHz Clock Cycles in One Video Line}} \times 2^{32}$$

Example:
NTSC Mode

$$\textit{Subcarrier Frequency} = \frac{227.5}{1716} \times 2^{32} = 569408542*$$

Subcarrier Register Value = 21F07C1Eh

SD F_{SC} Register 0: 1Eh
SD F_{SC} Register 1: 7Ch
SD F_{SC} Register 2: F0h
SD F_{SC} Register 3: 21h

Refer to the MPU Port Description Section for more detail on how to access the Subcarrier Frequency Registers.

SUBCARRIER PHASE REGISTER

[Subaddress 50h, 5Ch, Bits 7, 6]

Ten bits are used to set up the subcarrier phase. Each bit represents 0.352°. For normal operation, this register is set to 00h.

*Rounded to the nearest integer

FILTERS

Table XV shows an overview of the programmable filters available on the ADV7304A/ADV7305A.

Table XV. Selectable Filters

Filter	Subaddress
SD Luma LPF NTSC	40h
SD Luma LPF PAL	40h
SD Luma Notch NTSC	40h
SD Luma Notch PAL	40h
SD Luma SSAF	40h
SD Luma CIF	40h
SD Luma QCIF	40h
SD Chroma 0.65 MHz	40h
SD Chroma 1.0 MHz	40h
SD Chroma 1.3 MHz	40h
SD Chroma 2.0 MHz	40h
SD Chroma 3.0 MHz	40h
SD Chroma CIF	40h
SD Chroma QCIF	40h
SD UV SSAF	42h
HD Chroma Input	13h
HD Sync Filter	13h
HD Chroma SSAF	13h

HD Sync Filter

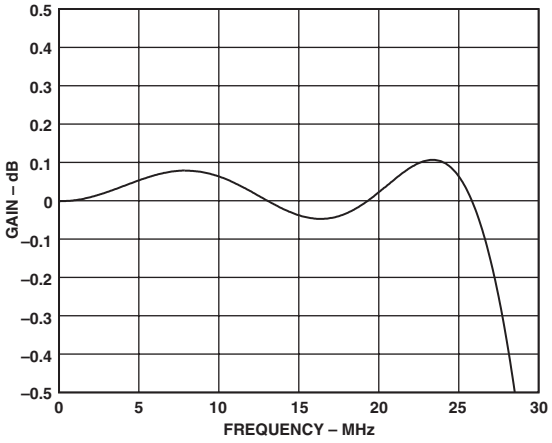


Figure 31. HD Sync Filter Enabled

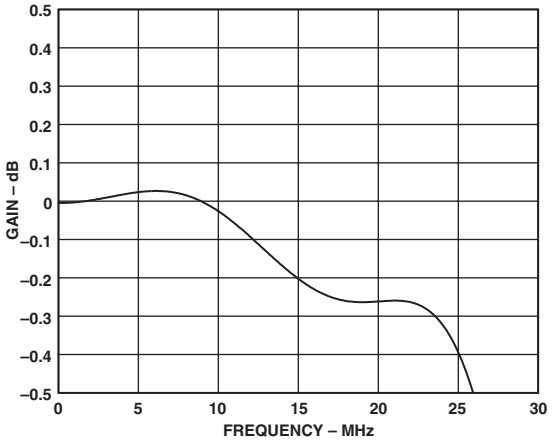


Figure 32. HD Sync Filter Disabled

HD 4:2:2 to 4:4:4 Interpolation Filters and Chroma SSAF
It is recommended to input data in 4:2:2 Input Mode to make use of the HD chroma SSAFs on the ADV7304A/ADV7305A. This filter has a 0 dB pass-band response and prevents signal components from being folded back into the frequency band. In 4:4:4 Input Mode, the video data is already interpolated by the external input device and the chroma SSAFs of the ADV7304A/ADV7305A are bypassed.

The chroma SSAF is controlled with Address 13h, Bit 5. When the HD input format is 4:2:2, the HD Chroma Input Bit [Address 13h, Bit 6] must be set to "1."

2×/4×/8× Oversampling Filters
The oversampling filters are enabled in setting the PLL ON control [Subaddress 00h, Bit 1] to "1." If enabled, PS and ITU-R.BT656 data is output at a rate of 108 MHz, HDTV at a rate of 148 MHz.

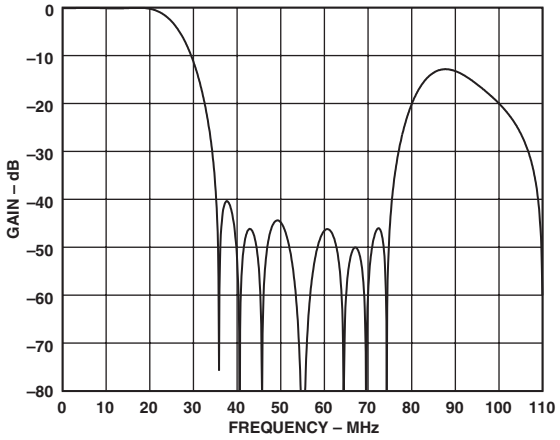


Figure 33. Y – PS 4× Oversampling Filter

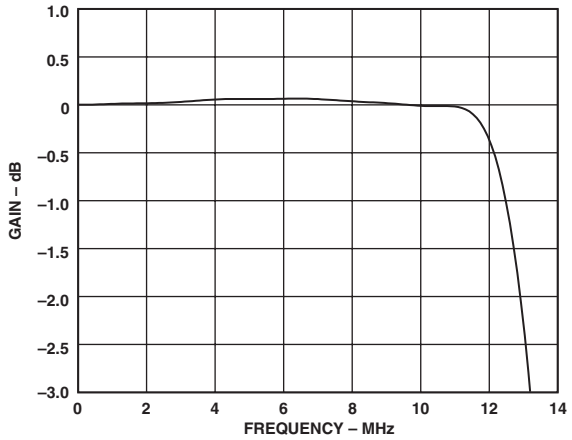


Figure 34. Y – PS 4× Oversampling Filter in the Pass Band

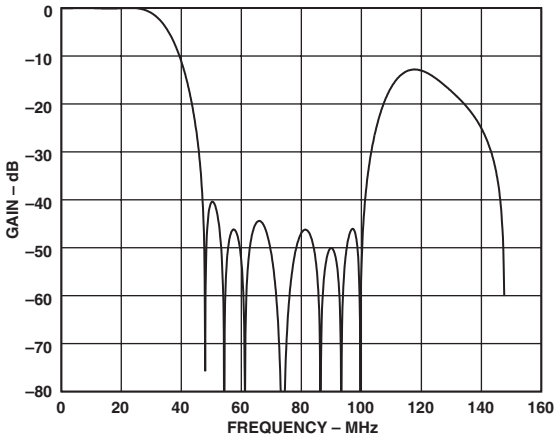


Figure 35. Y – HDTV 2× Oversampling Filter

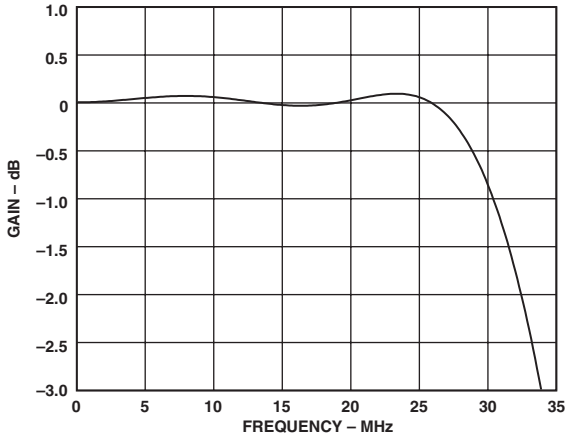


Figure 36. Y – HDTV 2× Oversampling Filter in the Pass Band

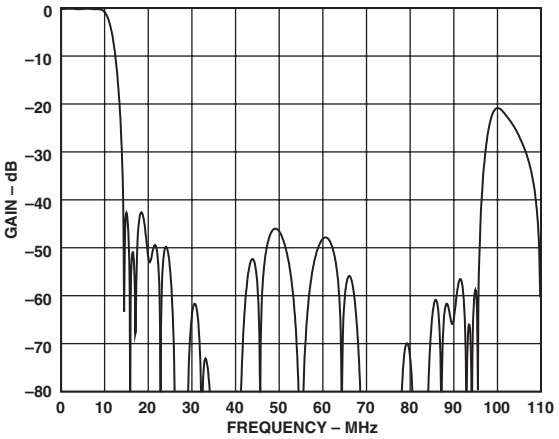


Figure 37. UV – HDTV 2× Oversampling Filter

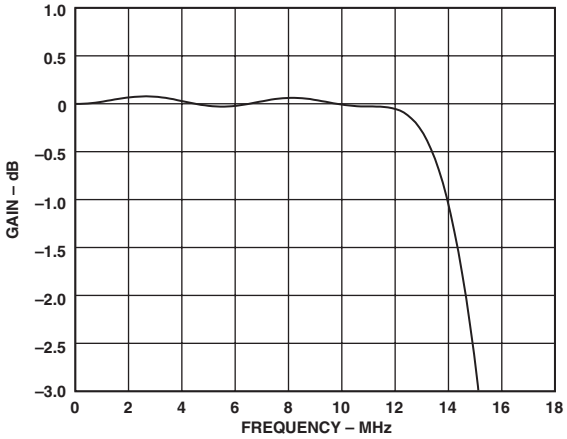


Figure 39. UV – HDTV 2× Oversampling Filter, Pass Band

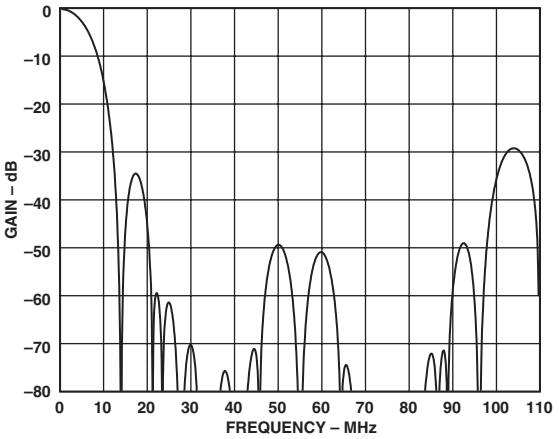


Figure 38. UV – PS 4× Oversampling Filter, Linear

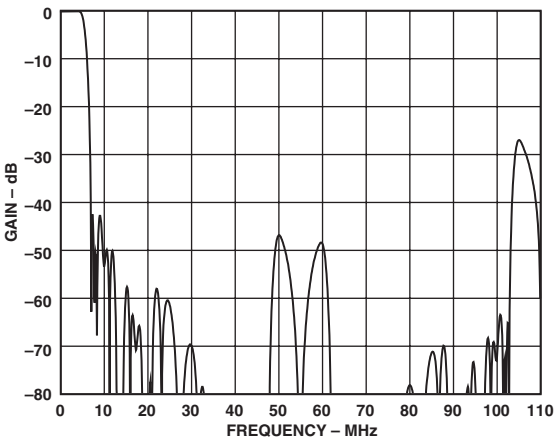


Figure 40. UV – PS 4× Oversampling Filter, SSAF

SD Internal Filter Response
[Subaddress 42h, Bit 0]

The Y filter supports several different frequency responses including two low-pass responses, two notch responses, an extended (SSAF) response with or without gain boost/attenuation, a CIF response, and a QCIF response. The UV filter supports several different frequency responses, including six low-pass responses, a CIF response, and a QCIF response, as can be seen in Figures 41–59.

If SD SSAF gain is enabled, there is the option of 12 responses in the range from –4 dB to +4 dB. The desired response can be chosen by the user by programming the correct value via the I^2C. The variation of frequency responses can be seen in Figures 41–59.

In addition to the chroma filters listed above, the ADV7304A/ADV7305A contains an SSAF filter specifically designed for and applicable to the color difference component outputs U and V. This filter has a cutoff frequency of approximately 2.7 MHz and –40 dB at 3.8 MHz, as shown in Figure 41. This filter can be controlled via Address 42h, Bit 0. If this filter is disabled, the selectable chroma filters shown in Table XVI can be used for the CVBS or chroma signal.

Table XVI. Internal Filter Specifications

Filter	Pass-Band Ripple[1] (dB)	3 dB Bandwidth[2] (MHz)
Luma LPF NTSC	0.16	4.24
Luma LPF PAL	0.1	4.81
Luma Notch NTSC	0.09	2.3/4.9/6.6
Luma Notch PAL	0.1	3.1/5.6/6.4
Luma SSAF	0.04	6.45
Luma CIF	0.127	3.02
Luma QCIF	Monotonic	1.5
Chroma 0.65 MHz	Monotonic	0.65
Chroma 1.0 MHz	Monotonic	1
Chroma 1.3 MHz	0.09	1.395
Chroma 2.0 MHz	0.048	2.2
Chroma 3.0 MHz	Monotonic	3.2
Chroma CIF	Monotonic	0.65
Chroma QCIF	Monotonic	0.5

NOTES
[1]Pass-band ripple is the maximum fluctuations from the 0 dB response in the pass band, measured in dB. The pass band is defined to have 0 Hz to fc (Hz) frequency limits for a low-pass filter, 0 Hz to f1 (Hz) and f2 (Hz) to infinity for a notch filter, where fc, f1, f2 are the –3 dB points.
[2]+3 dB bandwidth refers to the –3 dB cutoff frequency.

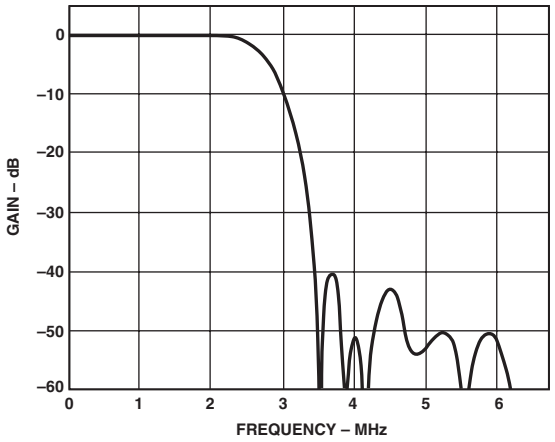


Figure 41. UV SSAF Filter

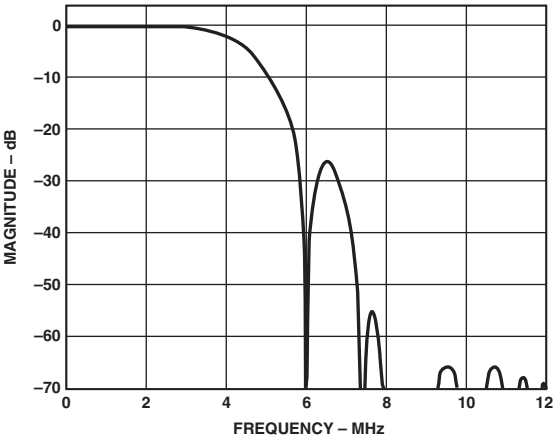


Figure 42. Luma NTSC Low-Pass Filter

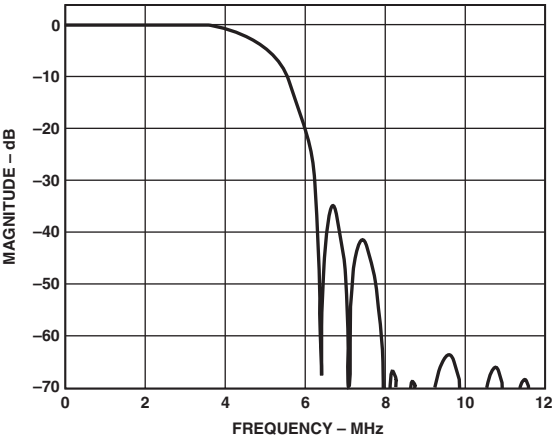


Figure 43. Luma PAL Low-Pass Filter

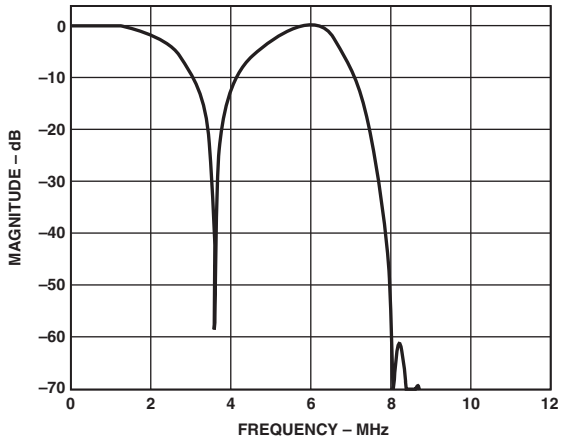


Figure 44. Luma NTSC Notch Filter

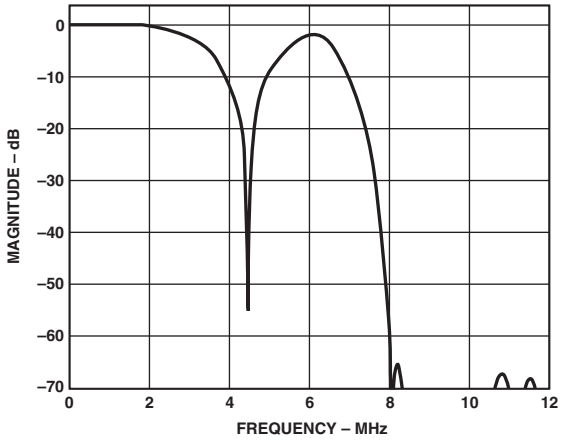


Figure 45. Luma PAL Notch Filter

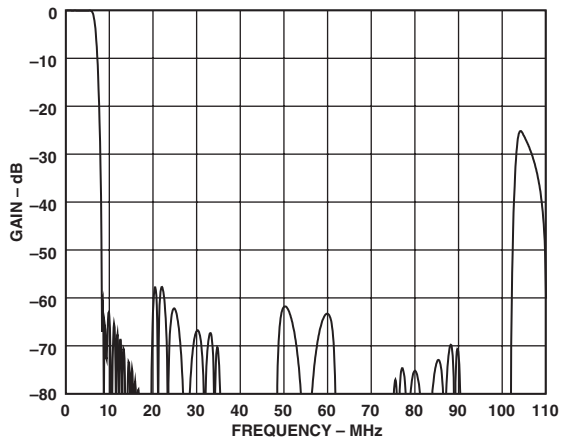


Figure 46. Luma SSAF Filter up to 108 MHz

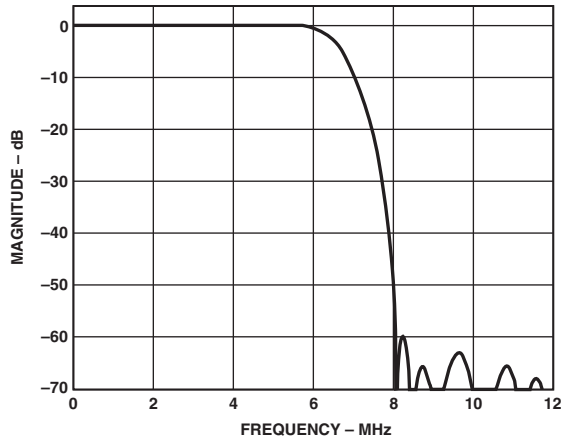


Figure 47. Luma SSAF Filter up to 12 MHz

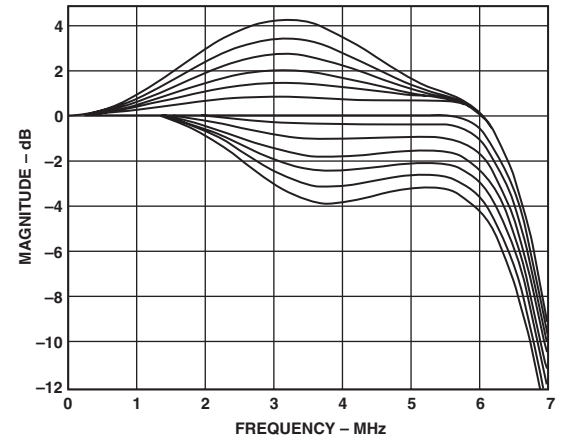


Figure 48. Luma SSAF Filter, Programmable Responses

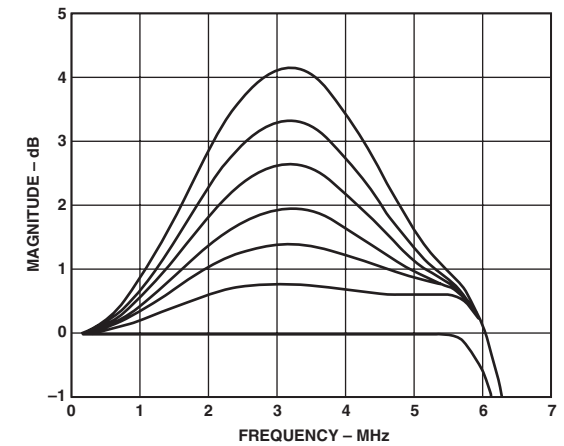


Figure 49. Luma SSAF Filter, Programmable Gain

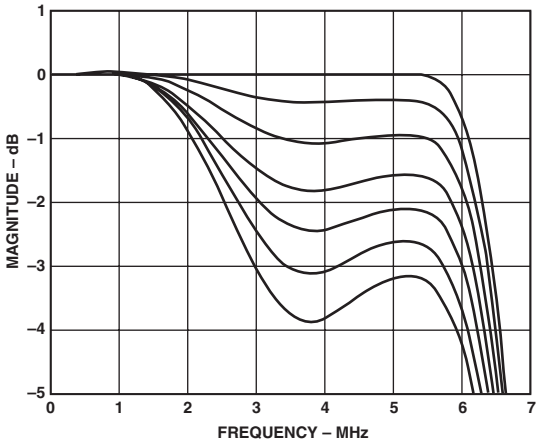


Figure 50. Luma SSAF Filter, Programmable Attenuation

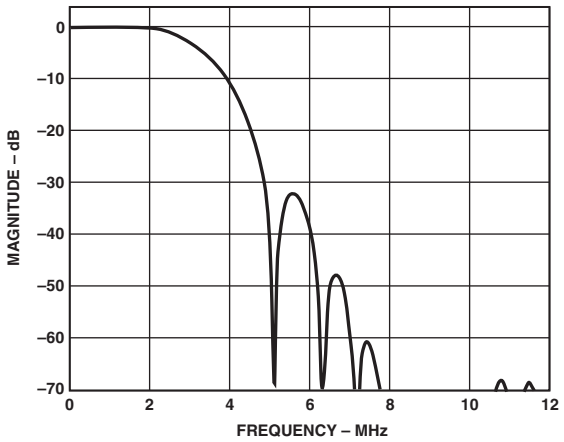


Figure 51. Luma CIF LP Filter

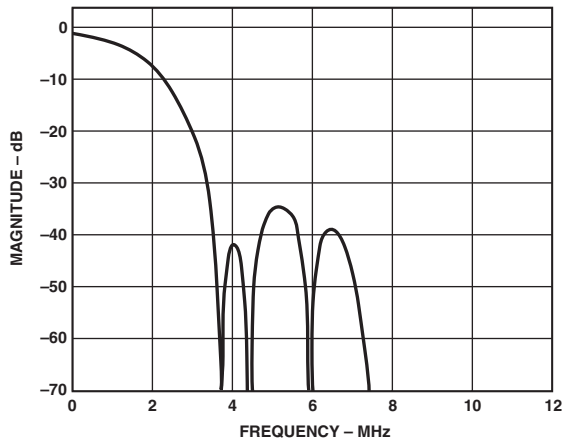


Figure 52. Luma QCIF LP Filter

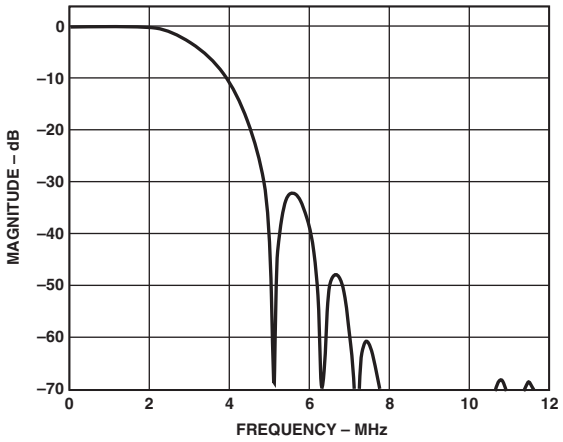


Figure 53. Chroma 3.0 MHz LP Filter

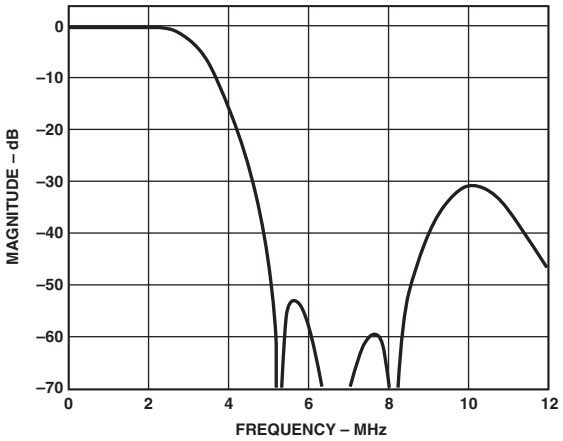


Figure 54. Chroma 2.0 MHz LP Filter

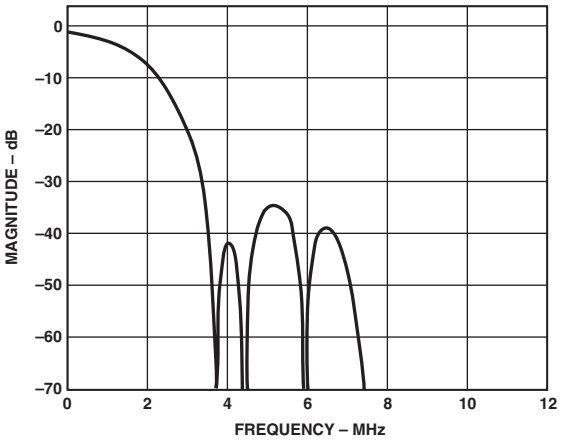


Figure 55. Chroma 1.3 MHz LP Filter

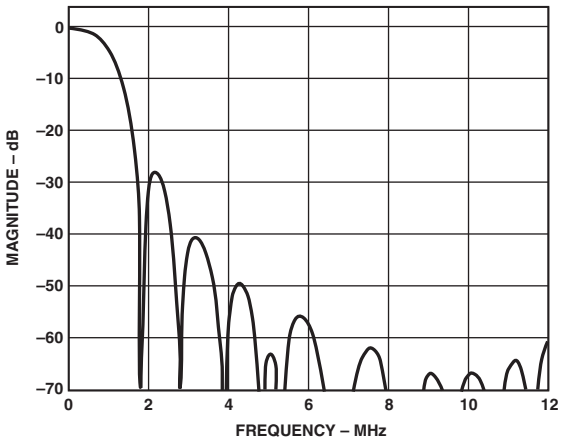


Figure 56. Chroma 1.0 MHz LP Filter

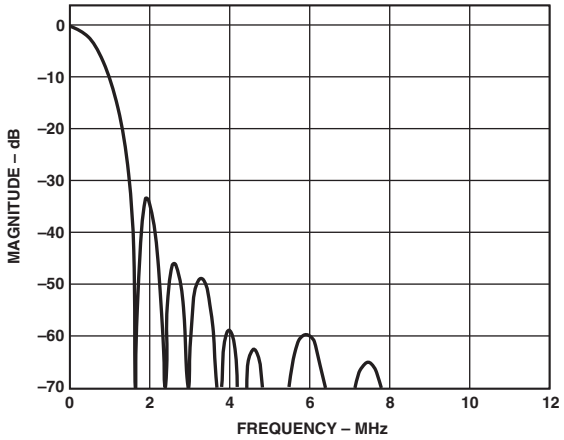


Figure 57. Chroma 0.65 MHz LP Filter

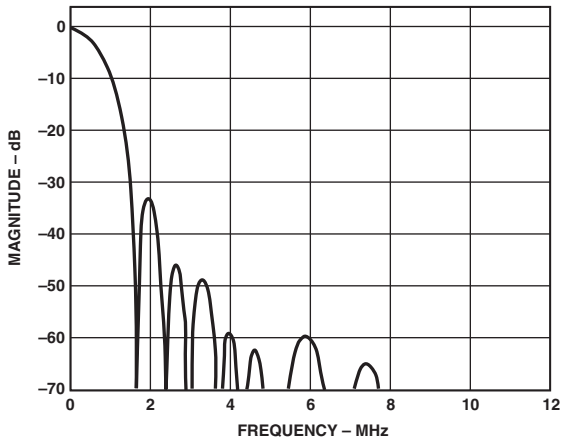


Figure 58. Chroma CIF LP Filter

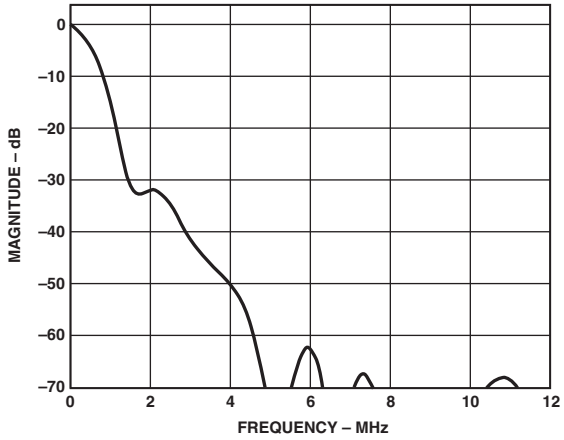


Figure 59. Chroma QCIF LP Filter

COLOR CONTROLS AND RGB MATRIX

HD Y Color, HD Cr Color, HD Cb Color [Subaddresses 16h–18h]

Three 8-bit wide registers at Addresses 16h, 17h, and 18h are used to program the output color of the internal HD test pattern generator, be it the lines of the crosshatch pattern or the uniform field test pattern. They are not functional as color controls on external pixel data input. For this purpose, the RGB matrix is used.

The standard used for the values for Y and the color difference signals to obtain white, black, and the saturated primary and complementary colors conforms to the ITU-R.BT601–ITU-R.BT604 standards. Table XVII shows sample color values to be programmed into the color registers when Output Standard Selection is set to EIA 770.2.

Table XVII. Sample Color Values for EIA 770.2 Output Standard Selection

Sample Color	Color Y Value	Color Cr Value	Color Cb Value
White	235 (EB)	128 (80)	128 (80)
Black	16 (10)	128 (80)	128 (80)
Red	81 (51)	240 (F0)	90 (5A)
Green	145 (91)	34 (22)	54 (36)
Blue	41 (29)	110 (6E)	240 (F0)
Yellow	210 (D2)	146 (92)	16 (10)
Cyan	170 (AA)	16 (10)	166 (A6)
Magenta	106 (6A)	222 (DE)	202 (CA)

HD RGB Matrix [Subaddresses 03h–09h]

When the programmable RGB matrix is disabled [Address 02h, Bit 3], the internal RGB matrix takes care of all YCrCb to YUV or RGB scaling according to the input standard programmed into the device.

When the programmable RGB matrix is enabled, the color components are converted according to the SMPTE274M standard (1080 i):

$$Y' = (0.2126 \times R') + (0.7152 \times G') + (0.0722 \times B')$$

$$Cb' = \frac{0.5}{1 - 0.0722} \times (B' - Y')$$

$$Cr' = \frac{0.5}{1 - 0.2126} \times (R' - Y')$$

This is reflected in the preprogrammed values for GY = 13Bh, RV = 1F0h, BU = 248h, GV = 93h, and GU = 3Bh.

If another input standard is used, the scale values for GY, GU, GV, BU, and RV have to be adjusted according to this input standard. It must be considered by the user that the color component conversion might use different scale values. For example, SMPTE293M uses the following conversion:

$$Y' = (0.299 \times R') + (0.587 \times G') + (0.114 \times B')$$

$$Cb' = \frac{0.5}{1 - 0.114} \times (B' - Y')$$

$$Cr' = \frac{0.5}{1 - 0.299} \times (R' - Y')$$

The programmable RGB matrix can be used to control the HD output levels in cases where the video output does not conform to standards due to altering the DAC output stages, such as termination resistors. The programmable RGB matrix is used for external HD data and is not functional when the HD test pattern is enabled.

To make use of the programmable RGB matrix, the YCrCb data should contain the HSYNC signal on the Y channel only. The RGB matrix should be enabled [Address 02h, Bit 3], the output should be set to RGB [Address 02h, Bit 3], Sync on PrPb should be disabled [Address 15h, Bit 2], and Sync on RGB is optional [Address 02h, Bit 4].

GY at Addresses 03h and 05h control the output levels on the green signal, BU at 04h and 08h the blue signal output levels, and RV at 04h and 09h the red output levels. To control YPrPb output levels, YUV output should be enabled [Address 02h, Bit 5]. In this case, GY [Address 05h; Address 03, Bits 0–1] is used for the Y output, RV [Address 09; Address 04, Bits 0–1] is used for the Pr output, and BU [Address 08h; Address 04h, Bits 2–3] is used for the Pb output.

If RGB output is selected, the RGB matrix scaler uses the following equations:

$$R = GY \times Y + RV \times Cr$$

$$G = GY \times Y - GU \times Cb - GV \times Cr$$

$$B = GY \times Y + BU \times Cb$$

If YUV output is selected, the following equations are used:

$$R = RV \times Cr$$

$$G = GY \times Y$$

$$B = BU \times Cb$$

On power-up, the RGB matrix is programmed with default values:

Address 03h: 03h
Address 04h: F0h
Address 05h: 4Eh
Address 06h: 0Eh
Address 07h: 24h
Address 08h: 92h
Address 09h: 7Ch

When the programmable RGB matrix is not functional, the ADV7304A/ADV7305A automatically scales YCrCb inputs to all standards supported. For SMPTE293M, the register values are as follows:

Address 03h: 03h
Address 04h: 1Eh
Address 05h: 4Eh
Address 06h: 1Bh
Address 07h: 38h
Address 08h: 8Bh
Address 09h: 6Eh

Address 15h, Bit 3 must be set to "1" in this mode.

SD Color Control [Subaddresses 5Ch, 5Dh, 5Eh, and 5Fh]

SD Y SCALE, SD Cr SCALE, and SD Cb SCALE are three 10-bit wide control registers to scale the Y, U, and V output levels.

Each of these registers represents the value required to scale the U or V level from 0 to 2.0 and the Y level from 0 to 1.5 of its initial level. The value of these 10 bits is calculated using the equation:

$$Y,\ U,\ or\ V\ Scalar\ Value = Scale\ Factor \times 512$$

Example:
Scale Factor = 1.18

$$Y, U, or V Scale Value = 1.18 \times 512 = 665.6$$
$$Y, U, or V Scale Value = 665 \text{ (rounded to nearest integer)}$$
$$Y, U, or V Scale Value = 1010011001_b$$

Address 5Ch, SD LSB Register = 15h
Address 5Dh, SD Y Scale Register = A6h
Address 5Eh, SD V Scale Register = A6h
Address 5Fh, SD U Scale Register = A6h

SD Hue Adjust Value
[Subaddress 60h]
The Hue Adjust Value is used to adjust the hue on the composite and chroma outputs.

These eight bits represent the value required to vary the hue of the video data, i.e., the variance in phase of the subcarrier during active video with respect to the phase of the subcarrier during the color burst. The ADV7304A/ADV7305A provides a range of ±22.5° in increments of 0.17578125°. For normal operation (zero adjustment), this register is set to 80h. FFh and 00h represent the attainable upper and lower limit (respectively) of adjustment.

For a positive hue adjust value:

$$0.17578125° \times (HCR - 128)$$

Example:
To adjust the hue by +4°, write 97h to the Hue Adjust Value Register:

$$\frac{+4}{0.17578125} + 128 = 151 = 97h$$

where 151 is rounded to the nearest integer. To adjust the hue by –4°, write 69h to the Hue Adjust Value Register:

$$\frac{-4}{0.17578125} + 128 = 105 = 69h$$

where 105 is rounded to the nearest integer.

SD Brightness Control
[Subaddress 61h]
The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level may be added onto the scaled Y data. For NTSC with pedestal, the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal and for PAL, the setup can vary from –7.5 IRE to +15 IRE.

The Brightness Control Register is an 8-bit wide register. Seven bits are used to control the brightness level. This brightness level can be a positive or negative value.

Example:
Standard: NTSC with pedestal. To add +20 IRE brightness level, write 28h to Address 61h, SD Brightness:

$$SD Brightness Value \text{ (hex)} = (IRE Value \times 2.015631)$$
$$28h = (20 \times 2.015631) = 40.31262$$

Standard: PAL. To add –7 IRE brightness level, write 72h to Address 61h, SD Brightness:

$$SD Brightness Value \text{ (hex)} = (IRE Value \times 2.015631)$$
$$0001110_b = (7 \times 2.015631) = 14.109417$$

0001110 in twos complement equals 1110010, or 72h.

SD Brightness Detect
[Subaddress 7Ah]
The ADV7304A/ADV7305A allows monitoring of the brightness level of the incoming video data. The Brightness Detect Register is a read-only register.

Double Buffering
[Subaddress 13h, Bit 7; Subaddress 48h, Bit 2]
Double buffered registers are updated once per field on the falling edge of the VSYNC signal. Double buffering improves the overall performance since modifications to register settings will not be made during active video but take effect on the start of the active video.

Double buffering can be activated on the following HD Registers: HD Gamma A and Gamma B curves, and HD CGMS Registers. Double buffering can be activated on the following SD Registers: SD Gamma A and Gamma B Curves, SD Y Scale, SD U Scale, SD V Scale, SD Brightness, SD Closed Captioning, and SD Macrovision Bits 5–0.

Table XVIII. Brightness Control Values

Setup Level— NTSC w/Pedestal (IRE)	Setup Level— NTSC w/o Pedestal (IRE)	Setup Level— PAL (IRE)	SD Brightness Value
22.5	+15	+15	1Eh
15	+7.5	+7.5	0Fh
7.5	0	0	00h
0	–7.5	–7.5	71h

Values in the range from 3Fh to 44h might result in an invalid output signal.

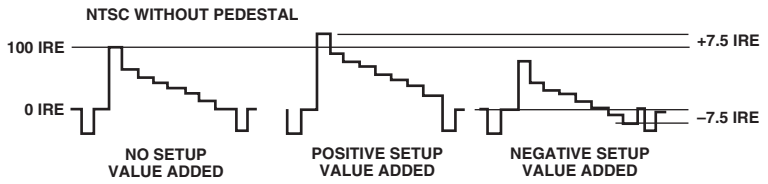


Figure 60. Examples for Brightness Control Values

Gamma Correction
[Subaddresses 21h–37h for HD;
Subaddresses 66h–79h for SD]

Gamma correction is available for SD and HD video. For each standard there are 20 8-bit wide registers. They are used to program the Gamma Correction Curves A and B. HD Gamma Curve A is programmed at Addresses 24h–2Dh and HD Gamma Curve B at 2Eh–37h. SD Gamma Curve A is programmed at Addresses 66h–6Fh, and SD Gamma Curve B at Addresses 70h–79h.

Generally, gamma correction is applied to compensate for the nonlinear relationship between signal input and brightness level output (as perceived on the CRT). It can also be applied wherever nonlinear processing is used.

Gamma correction uses the function:

$$Signal_{OUT} = \left(Signal_{IN}\right)^{\gamma}$$

where γ equals the gamma power factor.

Gamma correction is performed on the luma data only. The user has the choice to use two different curves, Curve A or Curve B. At any one time only one of these curves can be used. The response of the curve is programmed at 10 predefined locations. In changing the values at these locations, the gamma curve can be modified. Between these points, linear interpolation is used to generate intermediate values. Considering the curve to have a total length of 256 points, the 10 locations are: 24, 32, 48, 64, 80, 96, 128, 160, 192, and 224. Locations 0, 16, 240, and 255 are fixed and cannot be changed.

For the length of 16 to 240, the gamma correction curve must be calculated as:

$$y = x^{\gamma}$$

where y = gamma corrected output, x = linear input signal, and γ = the gamma power factor.

To program the gamma correction registers, the values for y must be calculated using the formula:

$$y_n = \left(\frac{x_{(n-16)}}{240-16}\right)^{\gamma} \times \left(240-16\right) + 16$$

where $x_{(n-16)}$ = the value for x along the x-axis at points n = 24, 32, 48, 64, 80, 96, 128, 160, 192, or 224; y_n = the value for y along the y-axis, which has to be written into the Gamma Correction Register.

Example:

$$y_{24} = \left(\left(\frac{8}{224}\right)^{0.5} \times 224\right) + 16 = 58\,*$$

$$y_{32} = \left(\left(\frac{16}{224}\right)^{0.5} \times 224\right) + 16 = 76\,*$$

$$y_{48} = \left(\left(\frac{32}{224}\right)^{0.5} \times 224\right) + 16 = 101\,*$$

$$y_{64} = \left(\left(\frac{48}{224}\right)^{0.5} \times 224\right) + 16 = 120\,*$$

$$y_{80} = \left(\left(\frac{64}{224}\right)^{0.5} \times 224\right) + 16 = 136\,*$$

$$y_{96} = \left(\left(\frac{80}{224}\right)^{0.5} \times 224\right) + 16 = 150\,*$$

$$y_{128} = \left(\left(\frac{112}{224}\right)^{0.5} \times 224\right) + 16 = 174\,*$$

$$y_{160} = \left(\left(\frac{144}{224}\right)^{0.5} \times 224\right) + 16 = 195\,*$$

$$y_{192} = \left(\left(\frac{176}{224}\right)^{0.5} \times 224\right) + 16 = 214\,*$$

$$y_{224} = \left(\left(\frac{208}{224}\right)^{0.5} \times 224\right) + 16 = 232\,*$$

The gamma curves shown in Figures 61 and 62 are examples. Any user defined curve is acceptable in the range of 16–240.

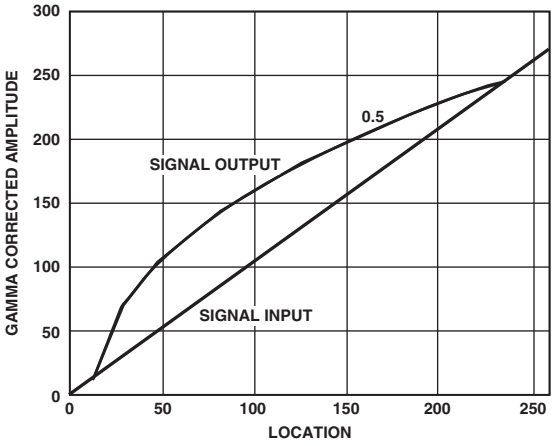


Figure 61. Signal Input (Ramp) and Signal Output for Gamma 0.5

*Rounded to the nearest integer

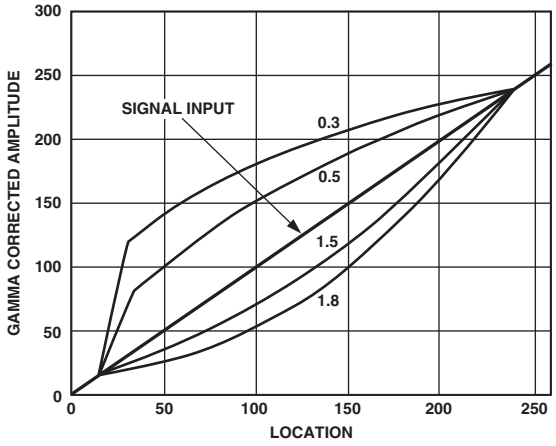


Figure 62. Signal Input (Ramp) and Selectable Gamma Output

HD SHARPNESS FILTER CONTROL AND ADAPTIVE FILTER CONTROL

[Subaddresses 20h and 38h–3Dh]

There are three filter modes available on the ADV7304A/ADV7305A: Sharpness Filter Mode and two adaptive filter modes.

HD Sharpness Filter Mode

To enhance or attenuate the Y signal in the frequency ranges shown in Figure 63, the following register settings must be used: HD Sharpness Filter must be enabled and HD Adaptive Filter Enable must be set to disabled.

To select one of the 256 individual responses, the corresponding gain values for each filter, which range from –8 to +7, must be programmed into the HD Sharpness Filter Gain Register at Address 20h.

HD Adaptive Filter Mode

The HD Adaptive Filter Threshold A, B, and C Registers, the HD Adaptive Filter Gain 1, 2, and 3 Registers, and the HD Sharpness Filter Gain Register are used in Adaptive Filter Mode. To activate the adaptive filter control, the HD Sharpness Filter and HD Adaptive Filter Enable must be enabled.

The derivative of the incoming signal is compared to the three programmable threshold values: HD Adaptive Filter Threshold A, B, and C. The recommended threshold range is from 16–235, although any value in the range of 0–255 can be used.

The edges can then be attenuated with the settings in HD Adaptive Filter Gain 1, 2, and 3 Registers and HD Sharpness Filter Gain Register.

According to the settings of the HD Adaptive Filter Mode control, there are two adaptive filter modes available:

1. Mode A is used when Adaptive Filter Mode is set to "0." In this case, Filter B (LPF) will be used in the adaptive filter block. Also, only the programmed values for Gain B in the HD Sharpness Filter Gain, HD Adaptive Filter Gain 1, 2, and 3 are applied when needed. The Gain A values are fixed and cannot be changed.
2. Mode B is used when Adaptive Filter Mode is set to "1." In this mode, a cascade of Filter A and Filter B is used. Both settings for Gain A and Gain B in the HD Sharpness Filter Gain, HD Adaptive Filter Gain 1, 2, and 3 become active when needed.

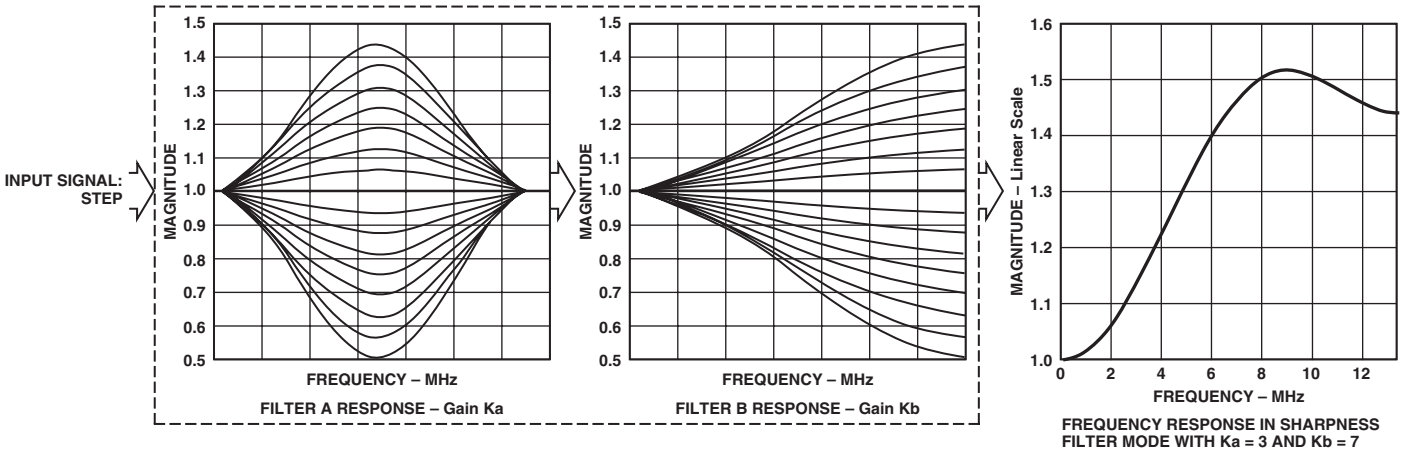


Figure 63. Sharpness and Adaptive Filter Control Block

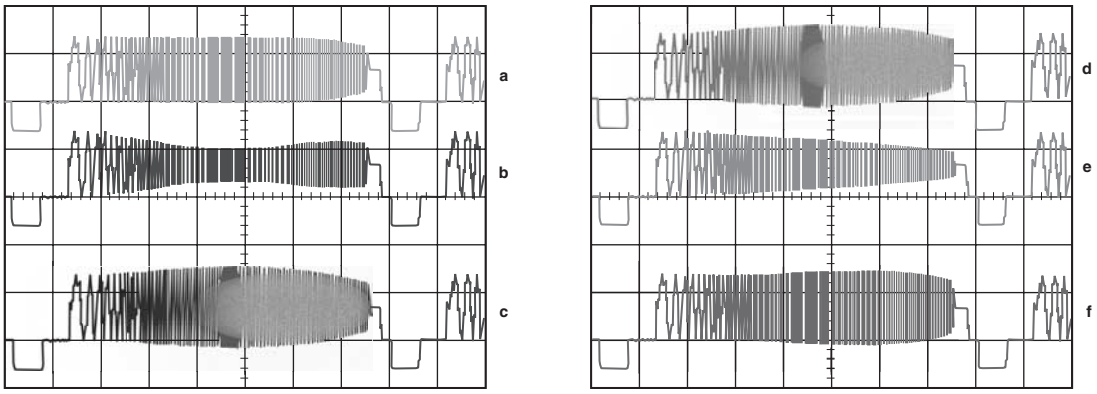


Figure 64. HD Sharpness Filter Control with Different Gain Settings for HD Sharpness Filter Gain Value

HD Sharpness Filter and Adaptive Filter Application Examples

HD Sharpness Filter Application

The HD sharpness filter can be used to enhance or attenuate the Y video output signal.

The register settings in Tables XIX and XX are used to achieve the results shown in Figure 64. Input data was generated by an external signal source.

Table XIX. Sharpness Filter on Frequency Sweep

Address	Register Setting	Reference*
00h	FCh	
01h	10h	
02h	20h	
10h	00h	
11h	81h	
20h	00h	a
20h	08h	b
20h	04h	c
20h	40h	d
20h	80h	e
20h	22h	f

*See Figure 64.

The effect of the sharpness filter can also be seen when using the internally generated crosshatch pattern.

Table XX. Sharpness Filter on Internal Test Pattern

Address	Register Setting
00h	FCh
01h	10h
02h	20h
10h	00h
11h	85h
20h	99h

In toggling the Sharpness Filter Enable Bit [Address 11h, Bit 8], it can be seen that the line contours of the crosshatch pattern change their sharpness.

Adaptive Filter Control Application

Figure 65 shows a typical signal to be processed by the adaptive filter control block.

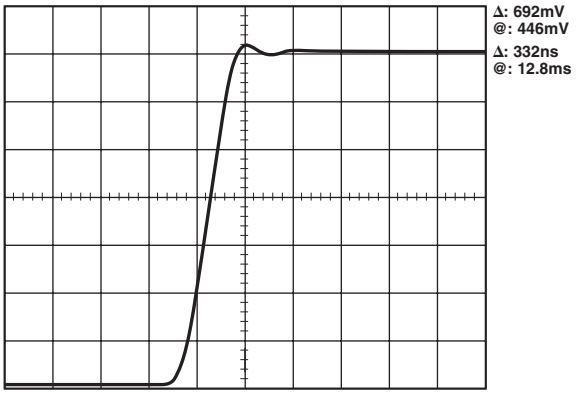


Figure 65. Input Signal to Adaptive Filter Control

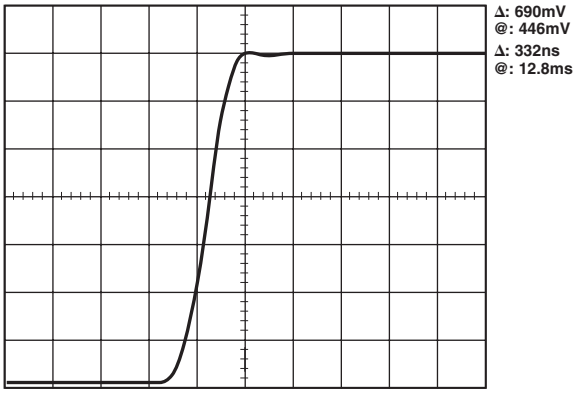


Figure 66. Output Signal after Adaptive Filter Control

The register settings in Table XXI are used to obtain the results shown in Figure 66, i.e., to remove the ringing on the Y signal. Input data was generated by an external signal source.

Table XXI. Adaptive Filter Control on Step Input Signal

Address	Register Setting
00h	FCh
01h	38h
02h	20h
10h	00h
11h	81h
15h	80h
20h	00h
38h	ACh
39h	9Ah
3Ah	88h
3Bh	28h
3Ch	3Fh
3Dh	64h

All other register settings are 00h.

When changing the Adaptive Filter Mode to Mode B [Address 15h, Bit 6], the output in Figure 67 can be obtained.

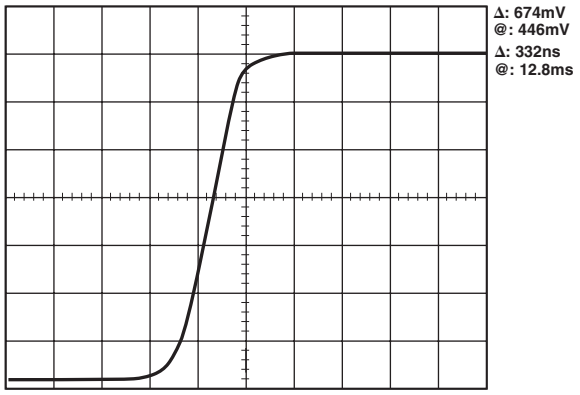


Figure 67. Output Signal from Adaptive Filter Control

The adaptive filter control can also be demonstrated using the internally generated crosshatch test pattern and toggling the Adaptive Filter Control Bit [Address 15h, Bit 7], shown in Table XXII.

Table XXII. Adaptive Filter Control on Internal Test Pattern

Address	Register Setting
00h	FCh
01h	38h
02h	20h
10h	00h
11h	85h
15h	80h
20h	00h
38h	ACh
39h	9Ah
3Ah	88h
3Bh	28h
3Ch	3Fh
3Dh	64h

SD DIGITAL NOISE REDUCTION
[Subaddresses 63h, 64h, and 65h]

DNR is applied to the Y data only. A filter block selects the high frequency, low amplitude components of the incoming signal (DNR input select). The absolute value of the filter output is compared to a programmable threshold value (DNR threshold control). There are two DNR modes available: DNR Mode and DNR Sharpness Mode.

In DNR Mode, if the absolute value of the filter output is smaller than the threshold, it is assumed to be noise. A programmable amount (coring gain border, coring gain data) of this noise signal will be subtracted from the original signal.

In DNR Sharpness Mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise, as before. Otherwise, if the level exceeds the threshold now being identified as a valid signal, a fraction of the signal (coring gain border, coring gain data) will be added to the original signal in order to boost high frequency components and to sharpen the video image.

In MPEG systems, it is common to process the video information in blocks of 8 × 8 pixels for MPEG2 systems, or 16 × 16 pixels for MPEG1 systems (block size control). DNR can be applied to the resulting block transition areas that are known to contain noise. Generally, the block transition area contains two pixels. It is possible to define this area to contain four pixels (border area).

It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the (DNR block offset).

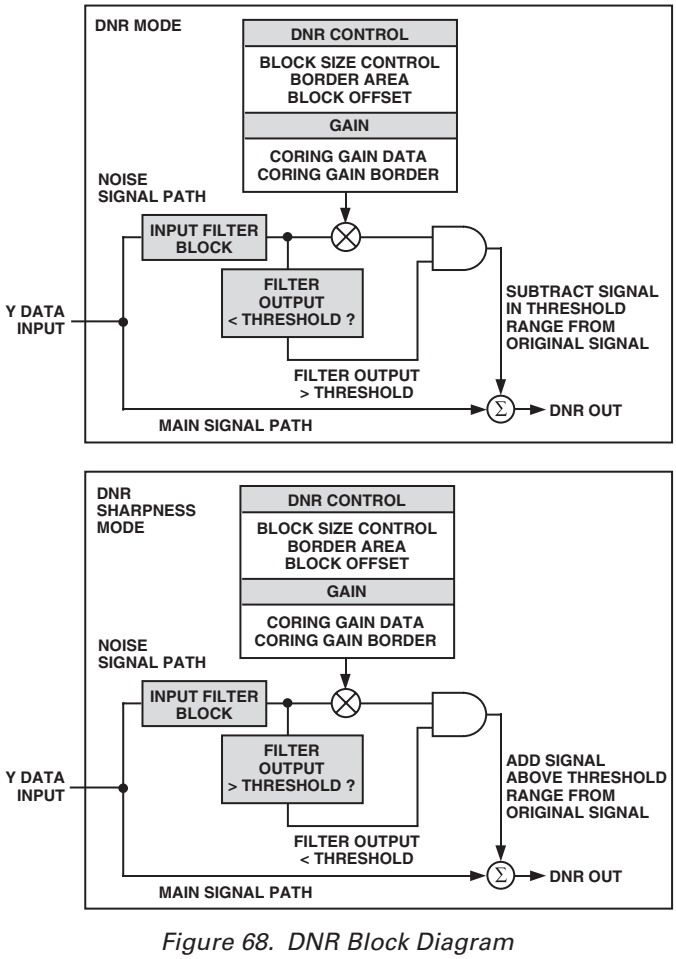


Figure 68. DNR Block Diagram

The Digital Noise Reduction Registers are three 8-bit wide registers. They are used to control the DNR processing.

Coring Gain Border
[Address 63h, Bits 3–0]
These four bits are assigned to the gain factor applied to the border areas. In DNR Mode, the range of gain values is 0–1, in increments of 0.125. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR Sharpness Mode, the range of gain values is 0 to 0.5, in increments of 0.0625. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

Coring Gain Data
[Address 63h, Bits 7–4]
These four bits are assigned to the gain factor applied to the luma data inside the MPEG pixel block.

In DNR Mode, the range of gain values is 0–1, in increments of 0.125. This factor is applied to the DNR filter output that lies below the set threshold range. The result is then subtracted from the original signal.

In DNR Sharpness Mode, the range of gain values is 0–0.5, in increments of 0.0625. This factor is applied to the DNR filter output that lies above the threshold range. The result is added to the original signal.

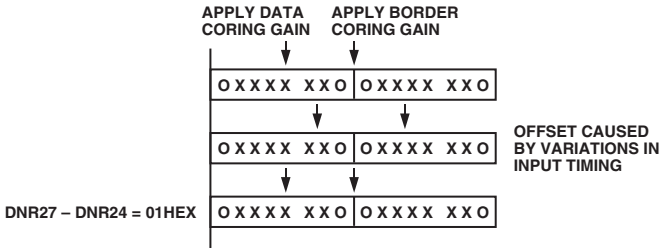


Figure 69. DNR Block Offset Control

DNR Threshold
[Address 64h, Bits 5–0]
These six bits are used to define the threshold value in the range of 0 to 63. The range is an absolute value.

Border Area
[Address 64h, Bit 6]
In setting this bit to a Logic "1," the block transition area can be defined to consist of four pixels. If this bit is set to a Logic "0," the border transition area consists of two pixels, where one pixel refers to two clock cycles at 27 MHz.

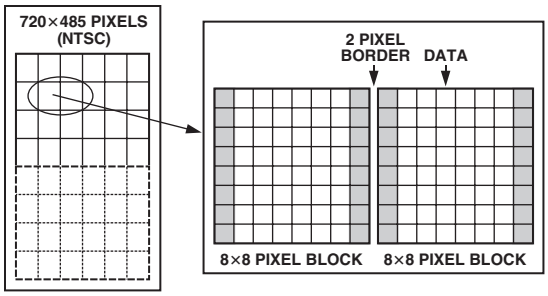


Figure 70. DNR Border Area

Block Size Control
[Address 64h, Bit 7]
This bit is used to select the size of the data blocks to be processed. Setting the block size control function to a Logic "1" defines a 16 × 16 pixel data block, a Logic "0" defines an 8 × 8 pixel data block, where 1 pixel refers to 2 clock cycles at 27 MHz.

DNR Input Select Control
[Address 65h, Bits 2–0]
Three bits are assigned to select the filter that is applied to the incoming Y data. The signal that lies in the pass band of the selected filter is the signal that will be DNR processed. The figure below shows the filter responses selectable with this control.

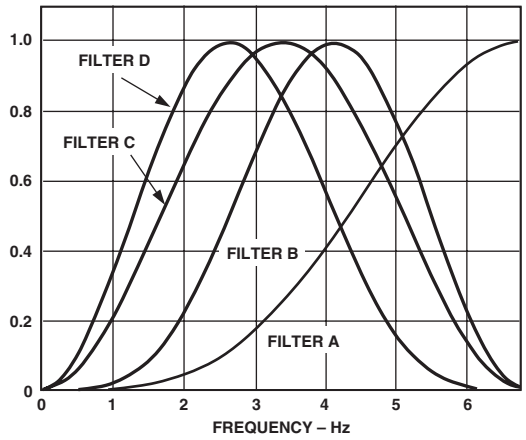


Figure 71. DNR Input Select

DNR Mode Control
[Address 65h, Bit 3]
This bit controls the DNR Mode selected. A Logic "0" selects DNR Mode, and Logic "1" selects DNR Sharpness Mode. DNR works on the principle of defining low amplitude, high frequency signals as probable noise and subtracting this noise from the original signal.

In DNR Mode, it is possible to subtract a fraction of the signal that lies below the set threshold, assumed to be noise, from the original signal. The threshold is set in DNR Register 1.

When DNR Sharpness Mode is enabled, it is possible to add a fraction of the signal that lies above the set threshold to the original signal, since this data is assumed to be valid data and not noise. The overall effect is that the signal will be boosted (similar to using extended SSAF filter).

Block Offset Control
[Address 65h, Bits 7–4]
Four bits are assigned to this control, which allows a shift of the data block of 15 pixels maximum. Consider the coring gain positions fixed. The block offset shifts the data in steps of one pixel such that the border coring gain factors can be applied at the same position regardless of variations in input timing of the data.

SD ACTIVE VIDEO EDGE

[Subaddress 42h, Bit 7]

When the active video edge is enabled, the first three pixels and the last three pixels of the active video on the Luma Channel are scaled in such a way that maximum transitions on these pixels are not possible. The scaling factors are 1/8×, 1/2×, and 7/8×. All other active video passes through unprocessed.

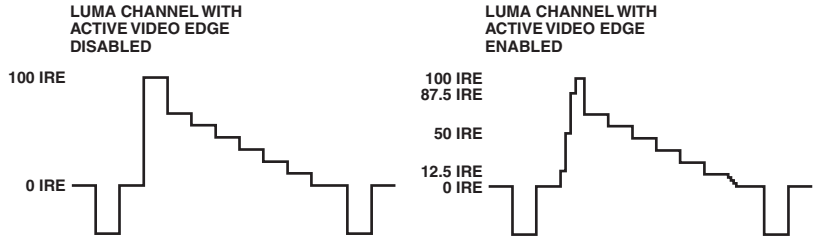


Figure 72. Active Video Edge Functionality Example

BOARD DESIGN AND LAYOUT CONSIDERATIONS

DAC Termination and Layout Considerations

The ADV7304A/ADV7305A contain an on-board voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor when the internal V_{REF} is used. Alternatively, the ADV7304A/ADV7305A can be used with an external V_{REF} (e.g., AD1580). The R_{SET} resistors are connected between the R_{SET} pins and AGND and are used to control the full-scale output current and, therefore, the DAC voltage output levels. For full-scale output, R_{SET} must have a value of 760 Ω. The R_{SET} values should not be changed. R_{LOAD} has a value of 150 Ω for full-scale output.

Video Output Buffer and Optional Output Filter

Output buffering on all six DACs is necessary in order to drive output devices, such as SD or HD monitors. Analog Devices produces a range of suitable op amps for this application, for example the AD8061. More information on line driver buffering circuits is given in the relevant op amp data sheets.

An optional analog reconstruction LPF might be required as an antialias filter if the ADV7304A/ADV7305A is connected to a device that requires this filtering. The filter specifications vary with the application, see Table XXIII.

Table XXIII. External Filter Requirements

Input Mode	External Filter Oversampling	Cutoff Frequency	Attenuation
SD	2×	>6.5 MHz	–50 dB @ 20.5 MHz
SD	8×	>6.5 MHz	–50 dB @ 101.5 MHz
PS	1×	>12.5 MHz	–50 dB @ 14.5 MHz
PS	4×	>12.5 MHz	–50 dB @ 95.5 MHz
HDTV	1×	>30 MHz	–50 dB @ 44.25 MHz
HDTV	2×	>30 MHz	–50 dB @ 118.5 MHz

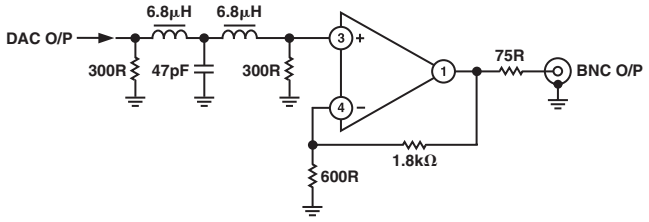


Figure 73. Example for Output Filter for SD, 8× Oversampling

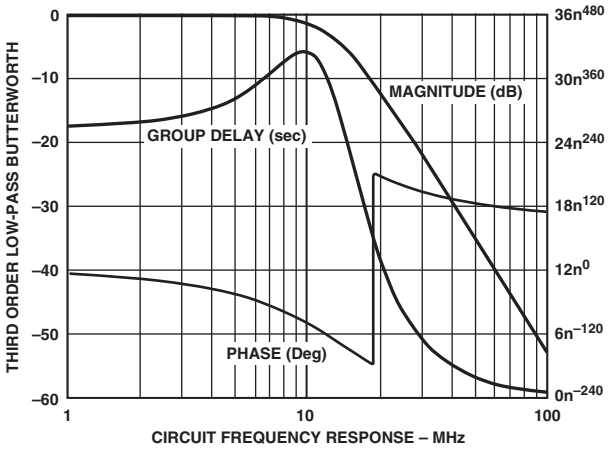


Figure 74. Filter Plot for Output Filter for SD, 8× Oversampling

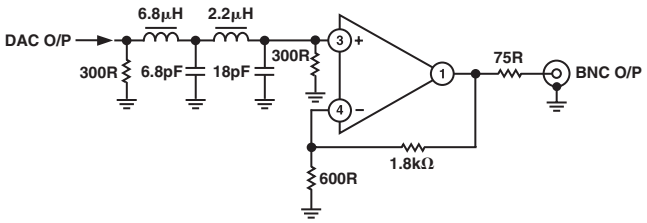


Figure 75. Example of Output for Output Filter for PS, 4× Oversampling

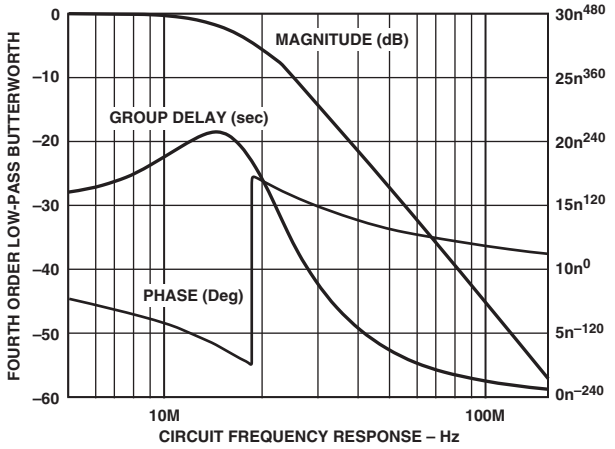


Figure 76. Filter Plot for Output Filter for PS, 4× Oversampling

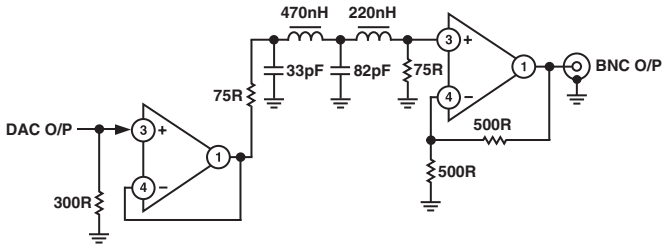


Figure 77. Example for Output Filter HDTV, 2× Oversampling

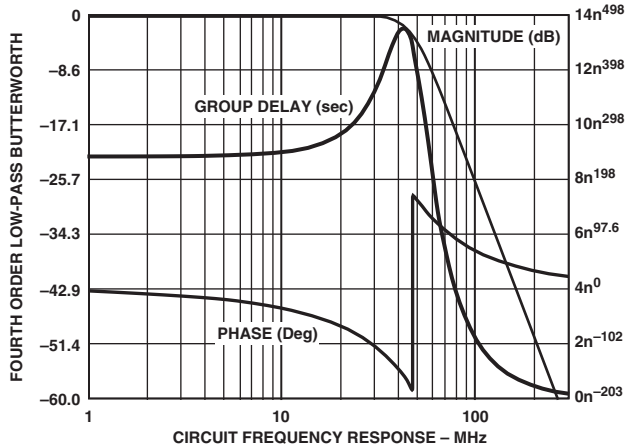


Figure 78. Filter Plot for Output Filter for HDTV, 2× Oversampling

Table XXIV. Possible Output Rates

Input Mode Addr 01h, Bits 6–4	PLL Addr 00h, Bit 1	Output Rate
SD	Off	27 MHz (2×)
	On	108 MHz (8×)
PS	Off	27 MHz (1×)
	On	108 MHz (4×)
HDTV	Off	74.25 MHz (1×)
	On	148.5 MHz (2×)
SD and	Off	27 MHz (2×)
	On	108 MHz (8×)
PS	Off	27 MHz (1×)
	On	108 MHz (4×)
SD* and	Off	27 MHz (2×)
	On	108 MHz (8×)
HDTV	Off	74.25 MHz (1×)
	On	74.25 MHz (1×)
SD and	Off	27 MHz (2×)
	On	27 MHz (2×)
HDTV*	Off	74.25 MHz (1×)
	On	148.5 MHz (2×)

*Oversampled

PCB Board Layout Considerations

The ADV7304A/ADV7305A is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7304A/ADV7305A, it is imperative that great care be given to the PC board layout. The layout should be optimized for the lowest noise on the ADV7304A/ADV7305A power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and AGND, V_{DD} and DGND, and V_{DD_IO} and GND_IO pins should be kept as short as possible to minimize inductive ringing.

It is recommended that a four-layer printed circuit board be used with power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Placement of components should take into account noisy circuits, such as crystal clocks, high speed logic circuitry, and analog circuitry.

There should be a separate analog ground plane and a separate digital ground plane.

Power planes should encompass a digital and an analog power plane. The analog power plane should contain the DACs and all associated circuitry, V_{REF} circuitry. The digital power plane should contain all logic circuitry. The analog and digital power planes should be individually connected to the common power plane at one single point through a suitable filtering device, such as a ferrite bead.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than three inches). The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As well as minimizing reflections, short analog output traces will reduce noise pickup due to neighboring digital circuitry.

To avoid crosstalk between the DAC outputs, it is recommended to leave as much space as possible between the tracks of the individual DAC output pins.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of decoupling capacitors. Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the group of V_{AA}, V_{DD}, or V_{DD_IO} pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

Digital Signal Interconnect

The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane. Due to the high clock rates used, long clock lines to the ADV7304A/ADV7305A should be avoided to minimize noise pickup. Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not the analog power plane.

Analog Signal Interconnect

The ADV7304A/ADV7305A should be located as close as possible to the output connectors, thus minimizing noise pickup and reflections due to impedance mismatch. For optimum performance, the analog outputs should each be source and load terminated, as shown in Figure 79. The termination resistors should be as close as possible to the ADV7304A/ADV7305A to minimize reflections.

Any unused inputs should be tied to ground.

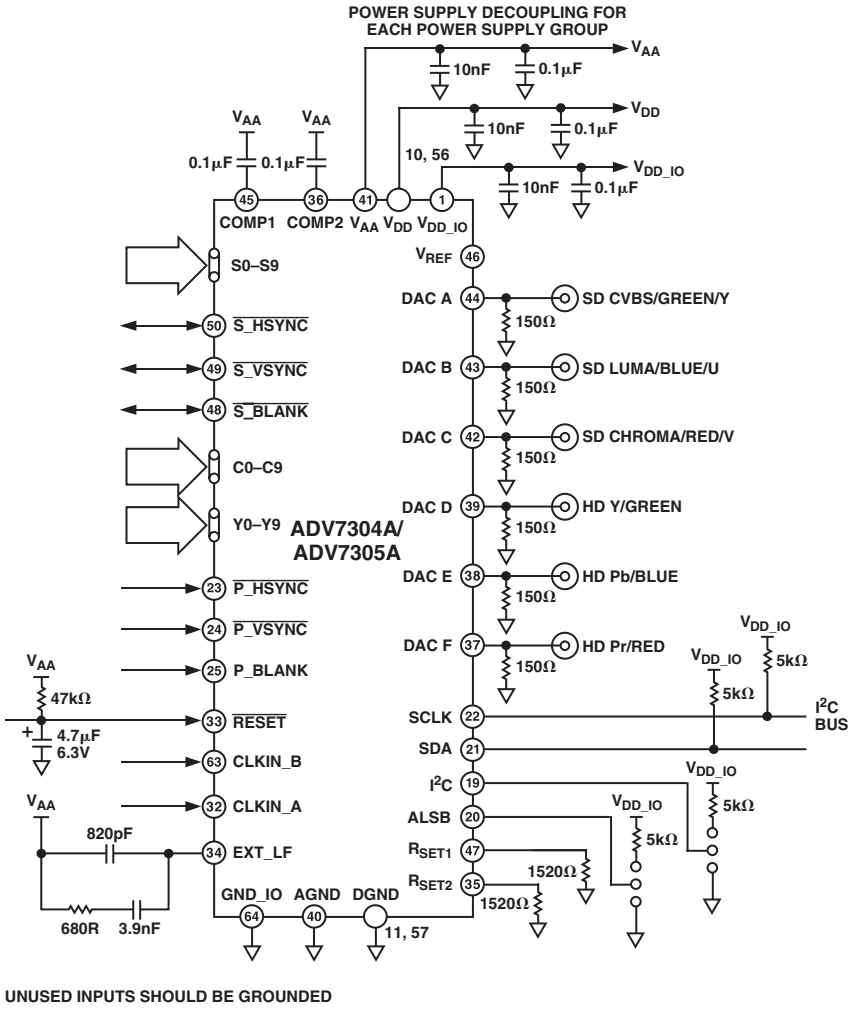


Figure 79. Circuit Layout

Appendix A

COPY GENERATION MANAGEMENT SYSTEM
HD CGMS DATA Registers 2–0
[Subaddress 12h]

HD CGMS is available in 525 p Mode only, conforming to "CGMS-A EIA-J CPR1204-1, Transfer Method of Video ID information using vertical blanking interval (525 p System), March 1998" and IEC61880, 1998, video systems (525/60)—video and accompanied data using the vertical blanking interval—analog interface.

When HD CGMS is enabled, CGMS data is inserted on Line 41. The HD CGMS Data Registers are to be found at Addresses 21h, 22h, and 23h.

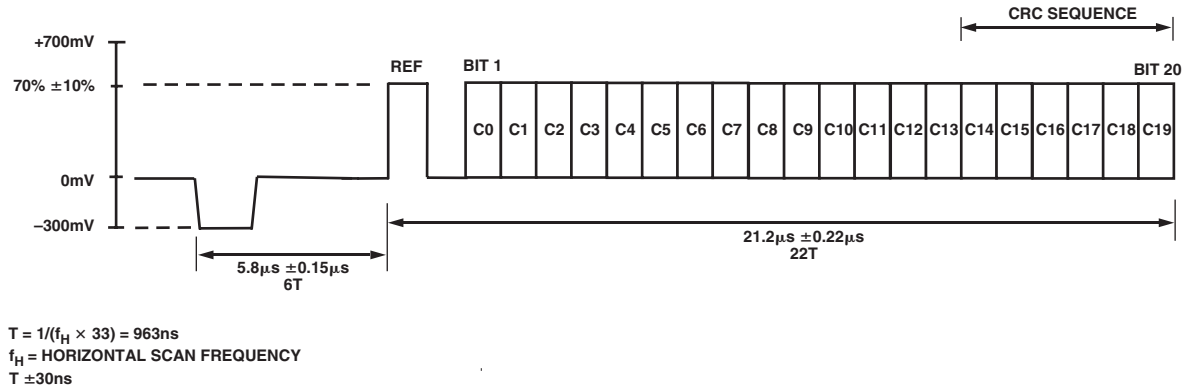


Figure 80. CGMS Waveform

SD CGMS Data Registers 2–0
[Subaddresses 59h, 5Ah, and 5Bh]

The ADV7304A/ADV7305A supports Copy Generation Management System (CGMS) conforming to the standard. CGMS data is transmitted on Line 20 of the odd fields and Line 283 of the even fields. Bits C/W05 and C/W06 control whether or not CGMS data is output on odd and even fields. CGMS data can only be transmitted when the ADV7304A/ADV7305A is configured in NTSC Mode. The CGMS data is 20 bits long; the function of each of these bits is as shown below. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit, see Figure 81.

If SD CGMS CRC [Address 59h, Bit 4] is set to a Logic "1," the last six bits, C19–C14, that comprise the 6-bit CRC check sequence are calculated automatically on the ADV7304A/ADV7305A based on the lower 14 bits (C0–C13) of the data in the data registers and output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial:

$$x^6 + x + 1$$

with a preset value of 111111. If SD CGMS CRC [Address 59h, Bit 4] is set to a Logic "0," then all 20 bits (C0–C19) are output directly from the CGMS registers (no CRC calculated; must be calculated by the user).

Table XXV. Function of CGMS Bits

Word	Bit	Function	
0	B1	Aspect Ratio	0 = 4:3 1 = 16:9
	B2	Display Format	0 = Normal 1 = Letterbox
	B3	Undefined	
	B4–B6	Identification Information about Video and Other Signals (i.e., Audio)	
1	B7–B10	Identification Signal. Incidental to Word 0.	
2	B11–B14	Identification Signal and Information. Incidental to Word 0.	

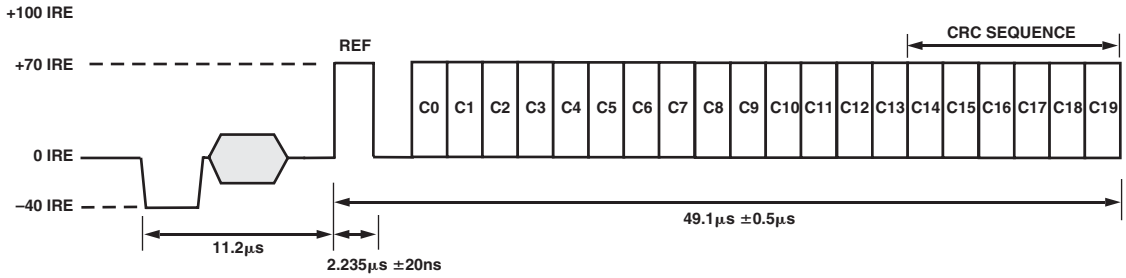


Figure 81. CGMS Waveform

Appendix B

SD WIDE SCREEN SIGNALLING
[Subaddresses 59h, 5Ah, and 5Bh]

The ADV7304A/ADV7305A supports Wide Screen Signalling (WSS) conforming to the standard. WSS data is transmitted on Line 23. WSS data can only be transmitted when the ADV7304A/ADV7305A is configured in PAL Mode. The WSS data is 14 bits long. The function of each of these bits is shown in Table XXVI. The WSS data is preceded by a run-in sequence and a start code (see Figure 82). If SD WSS [Address 59h, Bit 7] is set to a Logic "1," it enables the WSS data to be transmitted on Line 23. The latter portion of Line 23 (42.5 µs from the falling edge of HSYNC) is available for the insertion of video.

It is possible to blank the WSS portion of Line 23 with Subaddress 61h, Bit 7.

Table XXVI. Function of WSS Bits

Bit	Function
0	Aspect Ratio
1	Format
2	Position
3	Odd Parity Check of Bits 0–2
4	0 = Camera Mode 1 = Film Mode
5	0 = Standard Coding 1 = Motion Adaptive Color Plus
6	0 = No Helper 1 = Modulated Helper
7	Reserved
8	Reserved
9–10	00 = No Open Subtitles 10 = Subtitles Inside Active Image Area 01 = Subtitles Outside Active Image Area 11 = Reserved
11	0 = No Surround Sound Information 1 = Surround Sound Mode
12–13	Reserved

Table XXVII. Function of WSS Bits 0–3

B0	B1	B2	B3	Aspect Ratio	Format	Position
0	0	0	1	4:3	Full Format	N/A
1	0	0	0	14:9	Letterbox	Center
0	1	0	0	14:9	Letterbox	Top
1	1	0	1	16:9	Letterbox	Center
0	0	1	0	16:9	Letterbox	Top
1	0	1	1	>16:9	Letterbox	Center
0	1	1	1	14:9	Full Format	Center
1	1	1	0	16:9	N/A	N/A

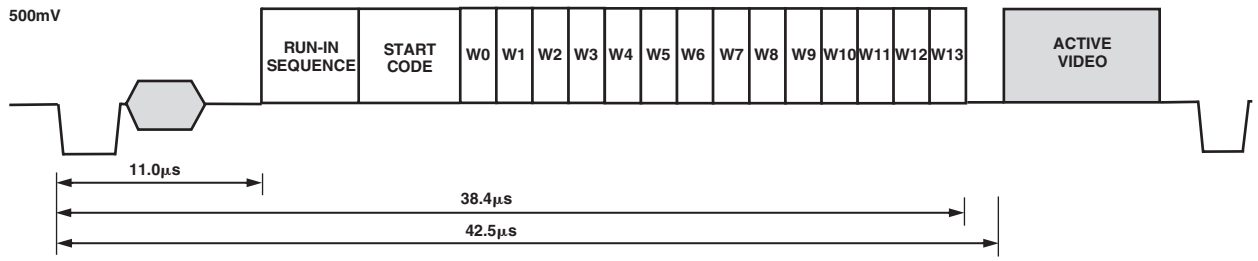


Figure 82. WSS Waveform

Appendix C

SD CLOSED CAPTIONING
[Subaddresses 51h–54h]

The ADV7304A/ADV7305A supports closed captioning conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of the even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase-locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by a Logic Level "1" start bit. Sixteen bits of data follow the start bit. These consist of two 8-bit bytes, 7 data bits, and 1 odd parity bit. The data for these bytes is stored in the SD Closed Captioning Registers [Addresses 53h–54h].

The ADV7304A/ADV7305A also supports the extended closed captioning operation that is active during even fields and is encoded on Line 284. The data for this operation is stored in the SD Closed Captioning Registers [Addresses 51h–52h].

All clock run-in signals and timing to support closed captioning on Lines 21 and 284 are generated automatically by the ADV7304A/ADV7305A. All pixels inputs are ignored during Lines 21 and 284 if closed captioning is enabled.

FCC Code of Federal Regulations (CFR) 47, Section 15.119 and EIA608 describe the closed captioning information for Lines 21 and 284.

The ADV7304A/ADV7305A uses a single buffering method. This means that the closed captioning buffer is only one byte deep; therefore, there will be no frame delay in outputting the closed captioning data unlike other 2-byte deep buffering systems. The data must be loaded one line before (Line 20 or Line 283) it is output on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor that in turn will load the new data (2 bytes) every field. If no new data is required for transmission, "0" must be inserted in both data registers; this is called nulling. It is also important to load "control codes," all of which are double bytes on Line 21, or a TV will not recognize them. If there is a message like "Hello World" that has an odd number of characters, it is important to pad it out to even to get the "end of caption" 2-byte control code to land in the same field.

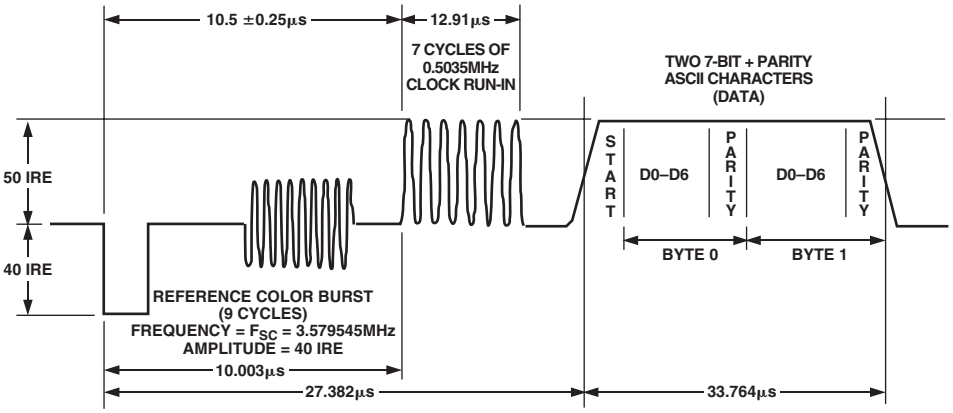


Figure 83. Closed Captioning Waveform, NTSC

Appendix D

TEST PATTERNS

The ADV7304A/ADV7305A can generate SD and HD test patterns.

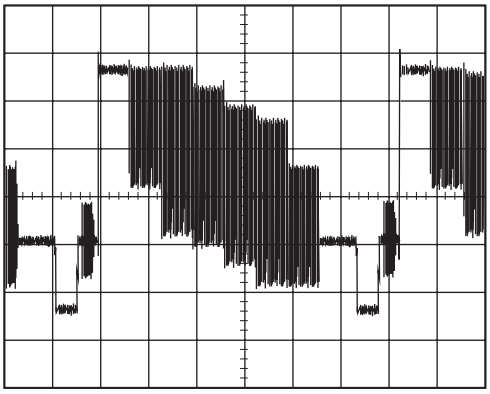


Figure 84. NTSC Color Bars

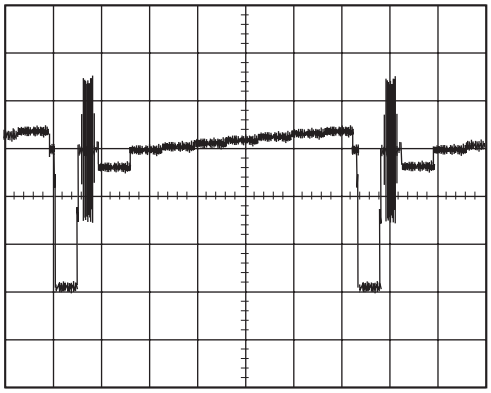


Figure 85. NTSC Black Bar (–21 mV, 0 mV, +3.5 mV, +7 mV, +10.5 mV, +14 mV, +18 mV, +23 mV)

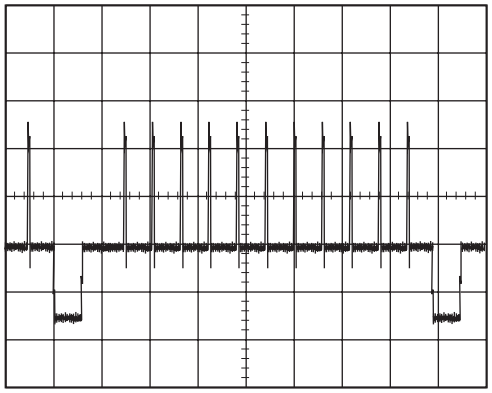


Figure 86. 525 p Hatch Pattern

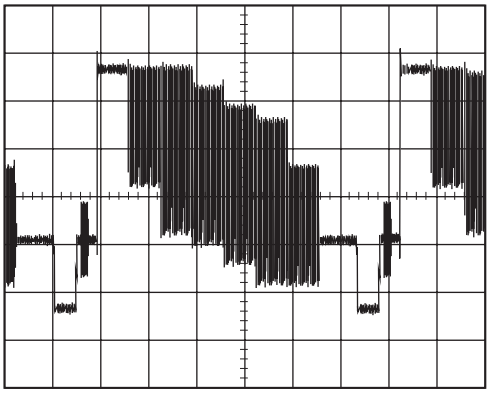


Figure 87. PAL Color Bars

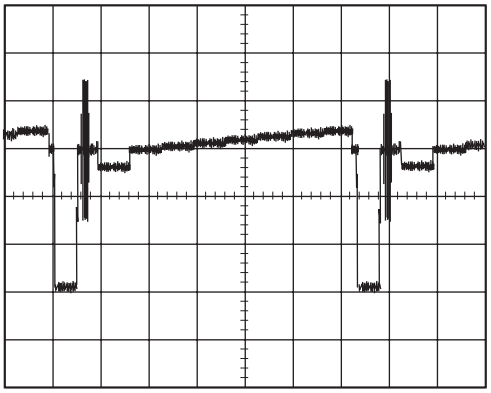


Figure 88. PAL Black Bar (–21 mV, 0 mV, +3.5 mV, +7 mV, +10.5 mV, +14 mV, +18 mV, +23 mV)

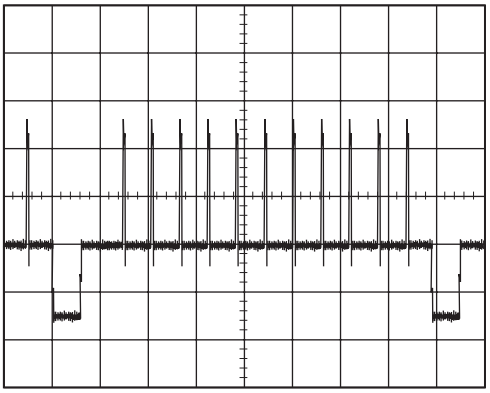


Figure 89. 625 p Hatch Pattern

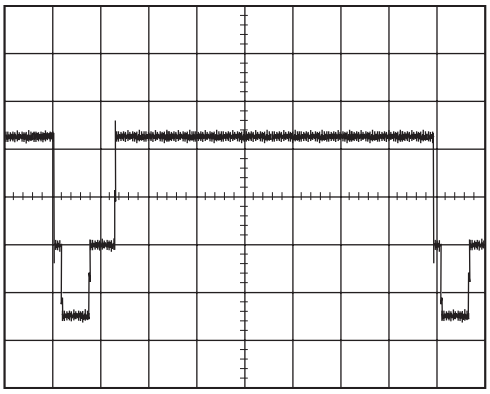


Figure 90. 525 p Field Pattern

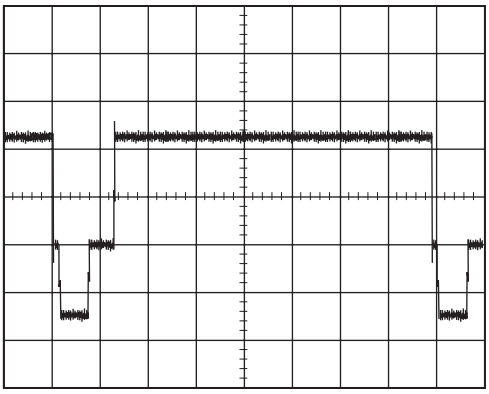


Figure 92. 625 p Field Pattern

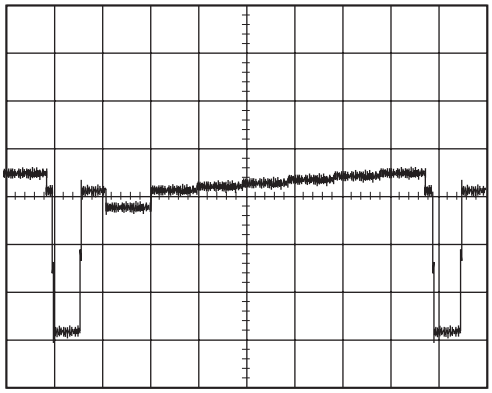


Figure 91. 525 p Black Bar (–35 mV, 0 mV, +7 mV, +14 mV, +21 mV, +28 mV, +35 mV)

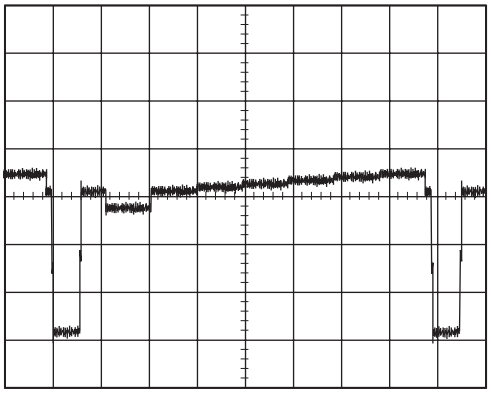


Figure 93. 625 p Black Bar (–35 mV, 0 mV, +7 mV, +14 mV, +21 mV, +28 mV, +35 mV)

Table XXVIII. NTSC CVBS Output on DAC A

Subaddress	Register Setting
00h	82h
11h	01h
40h	10h
42h	40h
44h	40h
4Ah	08h
4Ch	16h
4Dh	7Ch
4Eh	F0h
4Fh	21h

All other registers are set to 00h.

For PAL CVBS output on DAC A, the same settings in Table XXVIII are used except those listed in Table XXIX.

Table XXIX. PAL CVBS Output on DAC A

Subaddress	Register Setting
40h	11h
4Ch	CBh
4Dh	8Ah
4Eh	09h
4Fh	2Ah

Table XXX. NTSC Black Bar Pattern Output on DAC A

Subaddress	Register Setting
00h	82h
02h	04h
11h	01h
40h	10h
42h	40h
44h	40h
4Ah	08h
4Ch	16h
4Dh	7Ch
4Eh	F0h
4Fh	21h

All other registers are set to 00h. The Subcarrier Frequency Registers 4Ch–4Fh will be needed to generate the correct color burst signal.

For PAL Black Bar Pattern Output on DAC A, the same settings in Table XXX are used except those listed in Table XXXI.

Table XXXI. PAL Black Bar Pattern Output on DAC A

Subaddress	Register Setting
40h	11h
4Ch	CBh
4Dh	8Ah
4Eh	09h
4Fh	2Ah

Table XXXII. 525 p Hatch Pattern on DAC D

Subaddress	Register Setting
00h	12h
01h	10h
02h	20h
10h	40h
11h	05h
16h	A0h
17h	80h
18h	80h

All other registers are set to 00h.

For a 625 p Hatch Pattern on DAC D, the same settings in Table XXXII are used except for Subaddress 10h, which has a register setting of 50h.

Table XXXIII. 525 p Field Pattern*

Subaddress	Register Setting
00h	12h
01h	10h
02h	20h
10h	40h
11h	0Dh
16h	A0h
17h	80h
18h	80h

All other registers are set to 00h.
*See Figure 90.

For a 625 p Field Pattern on DAC D, the same settings in Table XXXIII are used except for Subaddress 10h, which has a register setting of 50h.

For a 525 p Black Bar Pattern Output on DAC D, the same settings in Table XXXIII are used except for Subaddresses 02h, which has a register setting of 24h.

For a 625 p Black Bar Pattern Output on DAC D, the same settings in Table XXXIII are used except for Subaddresses 02h and 10h, which have register settings of 24h and 50h, respectively.

Appendix E

SD TIMING MODES
[Subaddress 4Ah]
Mode 0 (CCIR-656): Slave Option
(Timing Register 0 TR0 = X X X X X 0 0 0)
The ADV7304A/ADV7305A is controlled by the start active video (SAV) and end active video (EAV) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. $\overline{\text{S\_VSYNC}}$, $\overline{\text{S\_HSYNC}}$, and $\overline{\text{S\_BLANK}}$ (if not used) pins should be tied high during this mode. Blank output is available.

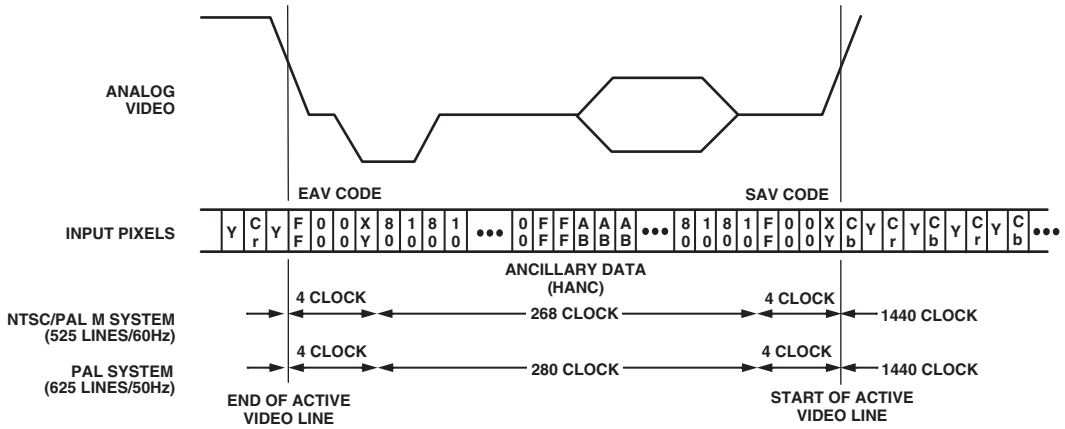


Figure 94. SD Slave Mode 0

Mode 0 (CCIR-656): Master Option
(Timing Register 0 TR0 = X X X X X 0 0 1)
The ADV7304A/ADV7305A generates H, V, and F signals required for the SAV and EAV time codes in the CCIR-656 standard. The H Bit is output on the $\overline{\text{S\_HSYNC}}$ pin, the V Bit is output on the $\overline{\text{S\_BLANK}}$ pin, and the F Bit is output on the $\overline{\text{S\_VSYNC}}$ pin.

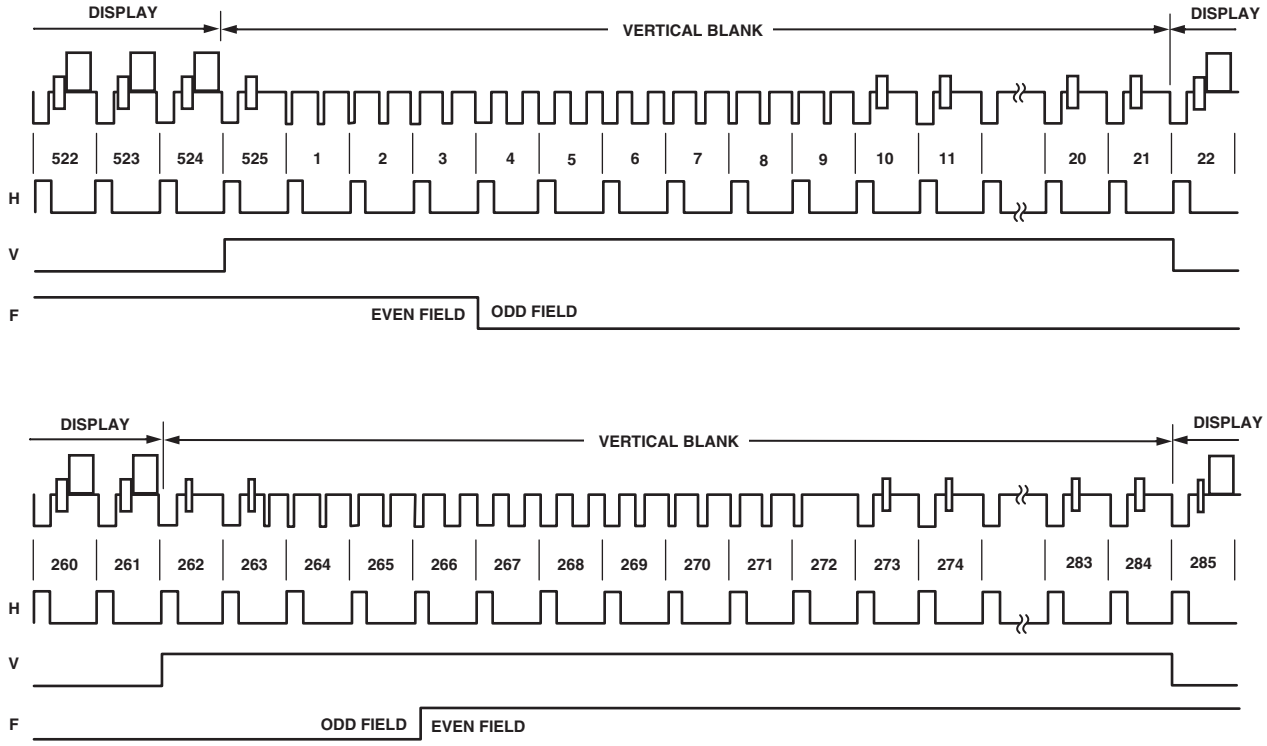


Figure 95. SD Master Mode 0, NTSC

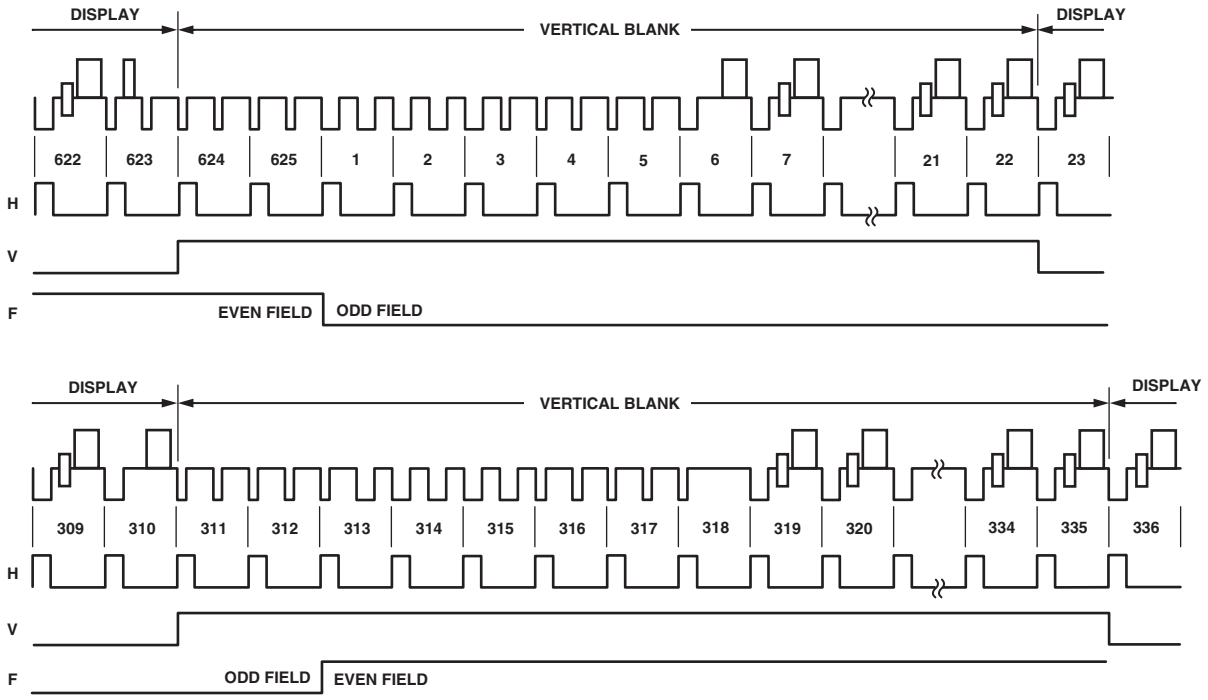


Figure 96. SD Master Mode 0, PAL

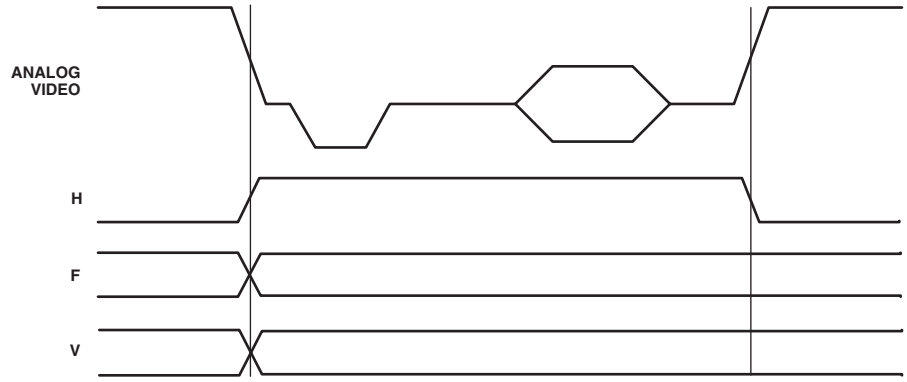


Figure 97. SD Master Mode 0 Data Transitions

Mode 1: Slave Option
HSYNC, BLANK, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 0)
In this mode, the ADV7304A/ADV7305A accepts horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when HSYNC is low indicates a new frame, i.e., vertical retrace. The BLANK signal is optional. When the BLANK input is disabled, the ADV7304A/ADV7305A automatically blanks all normally blank lines as per CCIR-624. HSYNC is input on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

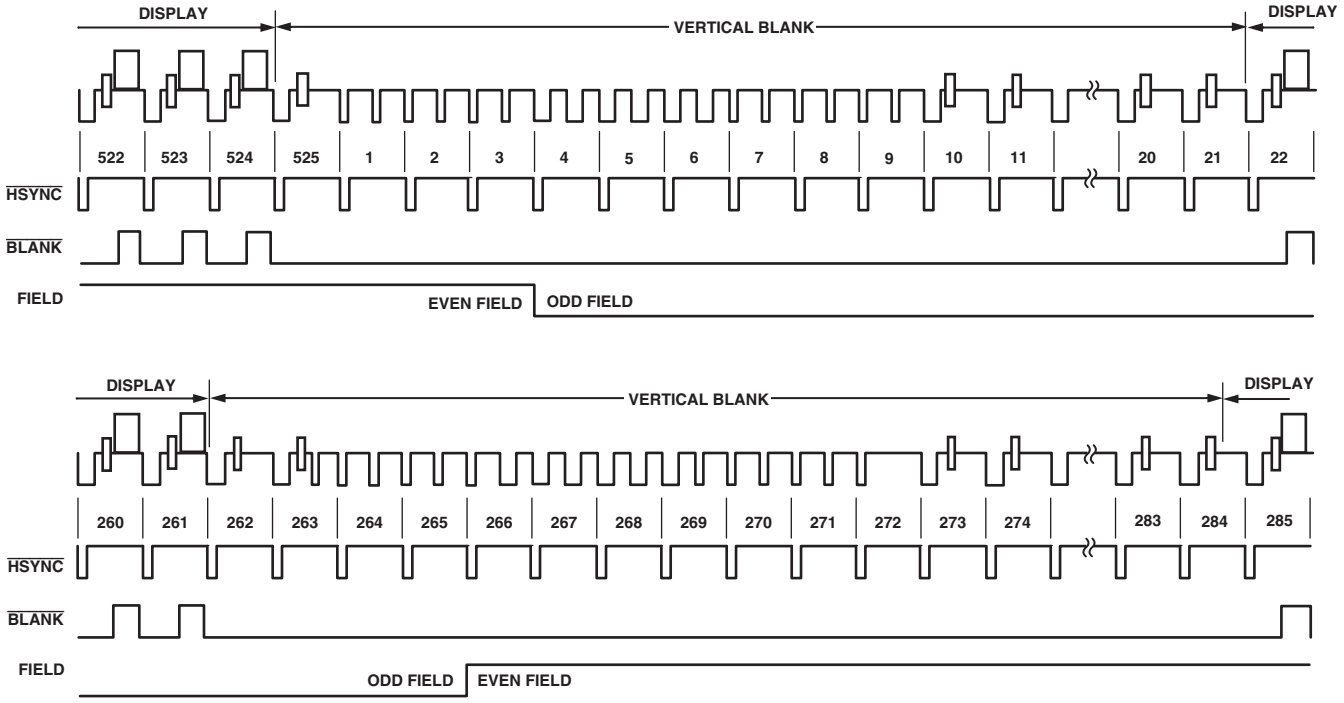


Figure 98. SD Slave Mode 1, NTSC

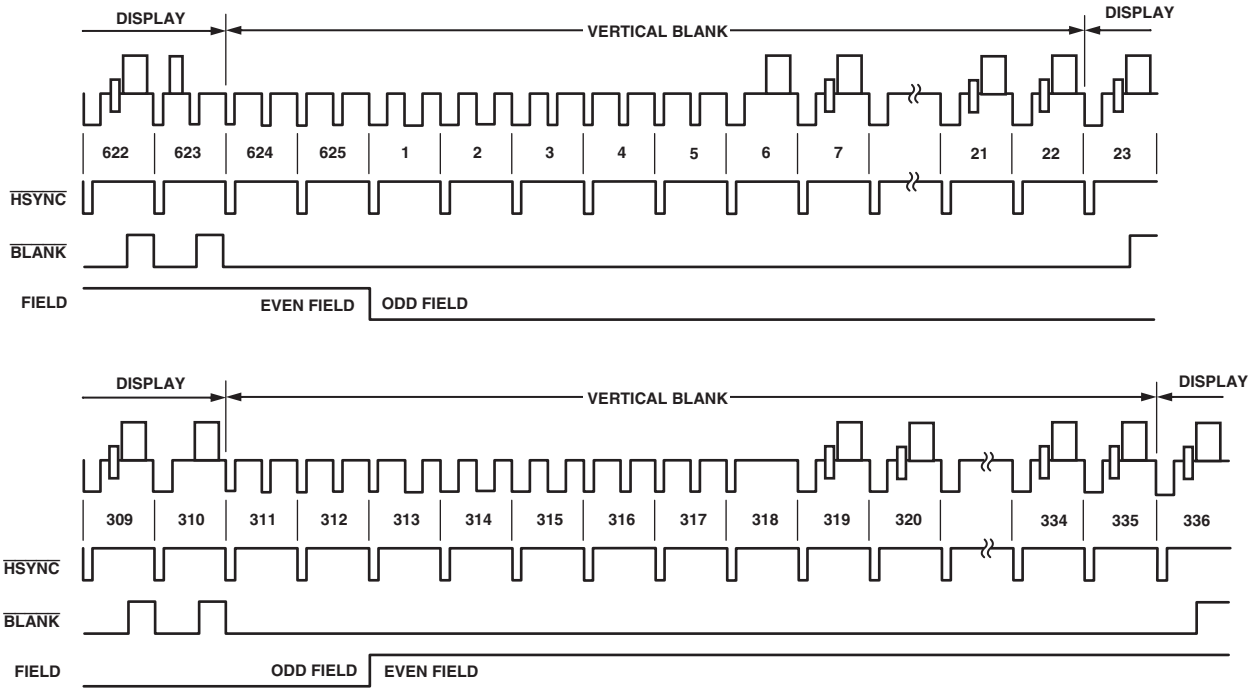


Figure 99. SD Slave Mode 1, PAL

Mode 1: Master Option
$\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode, the ADV7304A/ADV7305A can generate horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., vertical retrace. The blank signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7304A/ADV7305A automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. $\overline{\text{HSYNC}}$ is output on the $\overline{\text{S\_HSYNC}}$ pin, $\overline{\text{BLANK}}$ on the $\overline{\text{S\_BLANK}}$ pin, and FIELD on the $\overline{\text{S\_VSYNC}}$ pin.

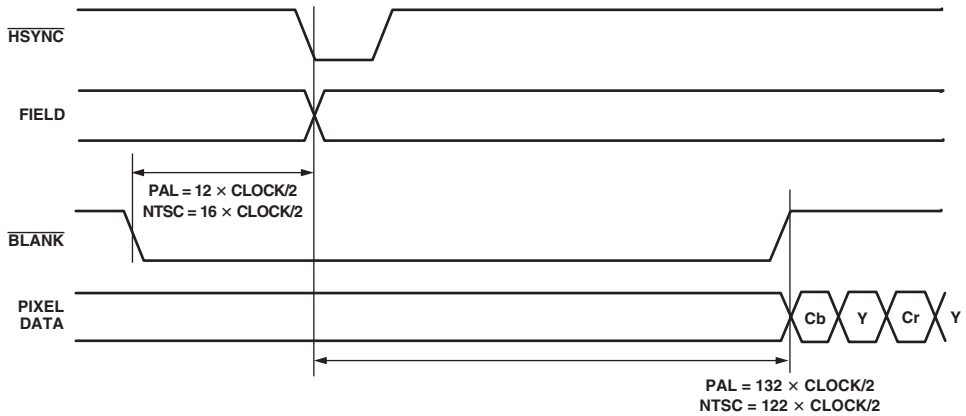


Figure 100. SD Timing Mode 1 Odd/Even Field Transitions, Master/Slave

Mode 2: Slave Option
HSYNC, VSYNC, BLANK
(Timing Register 0 TR0 = X X X X X 1 0 0)
In this mode, the ADV7304A/ADV7305A accepts horizontal and vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled, the ADV7304A/ADV7305A automatically blanks all normally blank lines as per CCIR-624. HSYNC is input on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

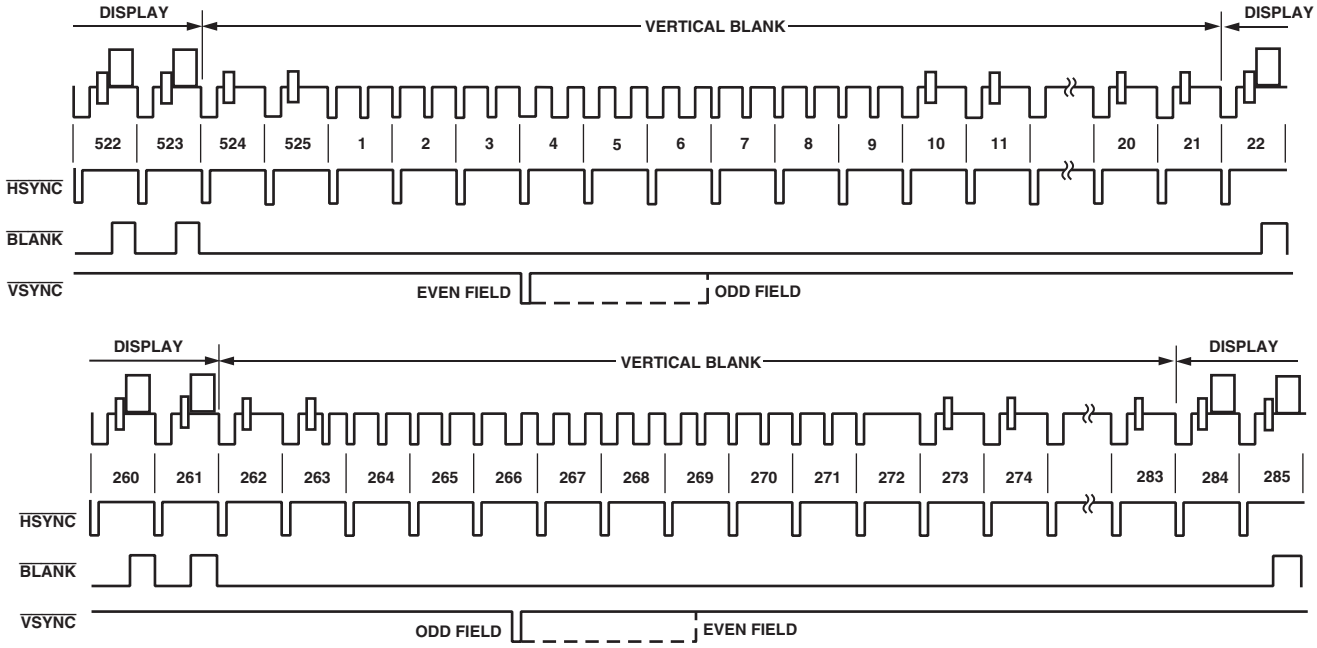


Figure 101. SD Slave Mode 2, NTSC

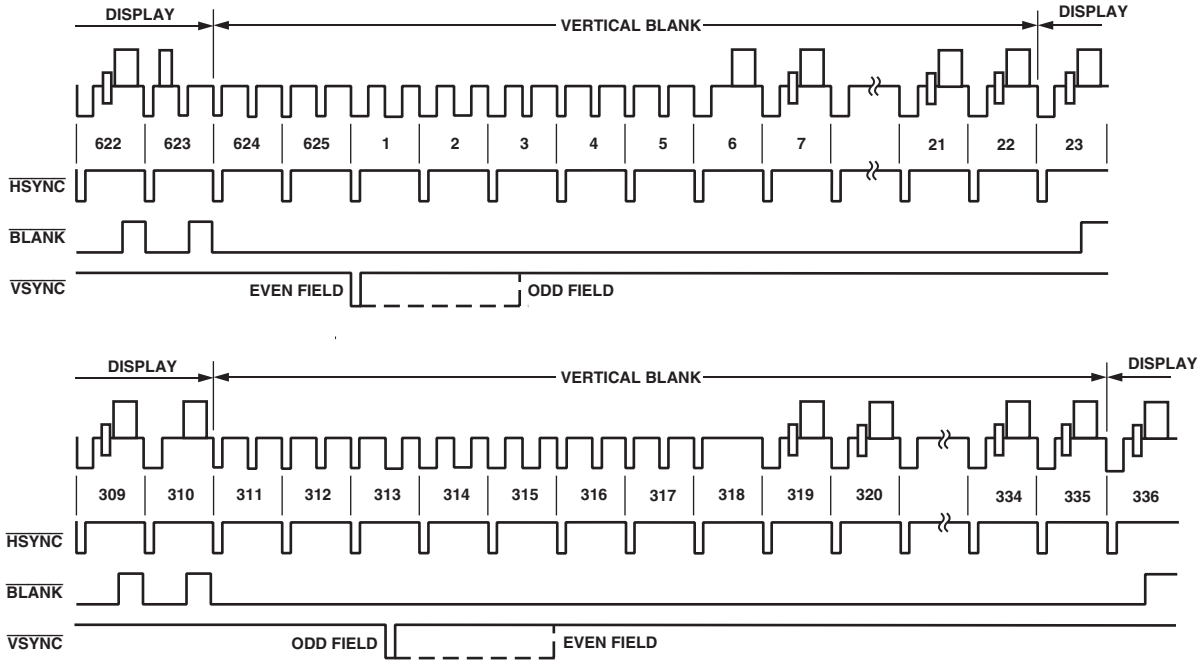


Figure 102. SD Slave Mode 2, PAL

Mode 2: Master Option
HSYNC, VSYNC, BLANK
(Timing Register 0 TR0 = X X X X X 1 0 1)
In this mode, the ADV7304A/ADV7305A can generate horizontal and vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled, the ADV7304A/ADV7305A automatically blanks all normally blank lines as per CCIR-624. HSYNC is output on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

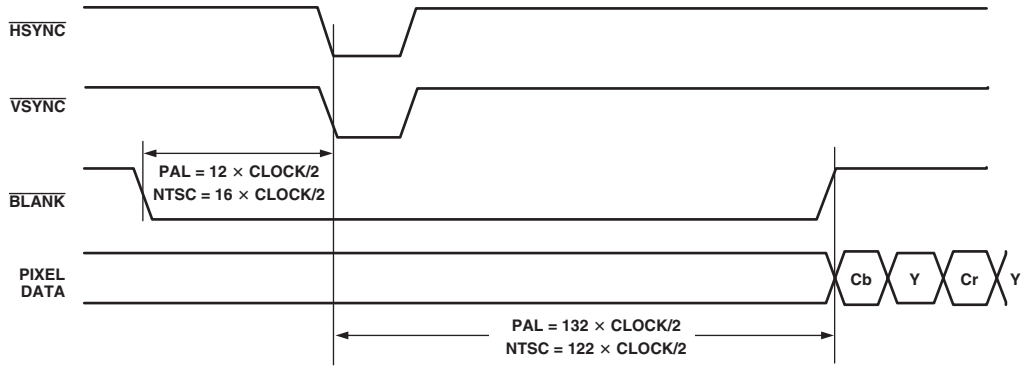


Figure 103. SD Timing Mode 2 Even to Odd Field Transition, Master/Slave

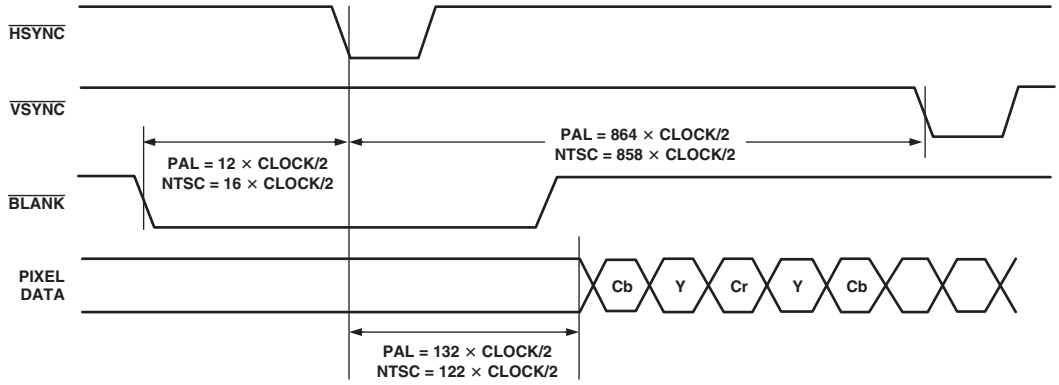


Figure 104. SD Timing Mode 2 Odd to Even Field Transition, Master/Slave

Mode 3: Master/Slave Option
HSYNC, BLANK, FIELD
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)
In this mode, the ADV7304A/ADV7305A accepts or generates horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when HSYNC is high indicates a new frame, i.e., vertical retrace. The BLANK signal is optional. When the BLANK input is disabled, the ADV7304A/ADV7305A automatically blanks all normally blank lines as per CCIR-624. HSYNC is interfaced on the S_HSYNC pin, BLANK on the S_BLANK pin, and FIELD on the S_VSYNC pin.

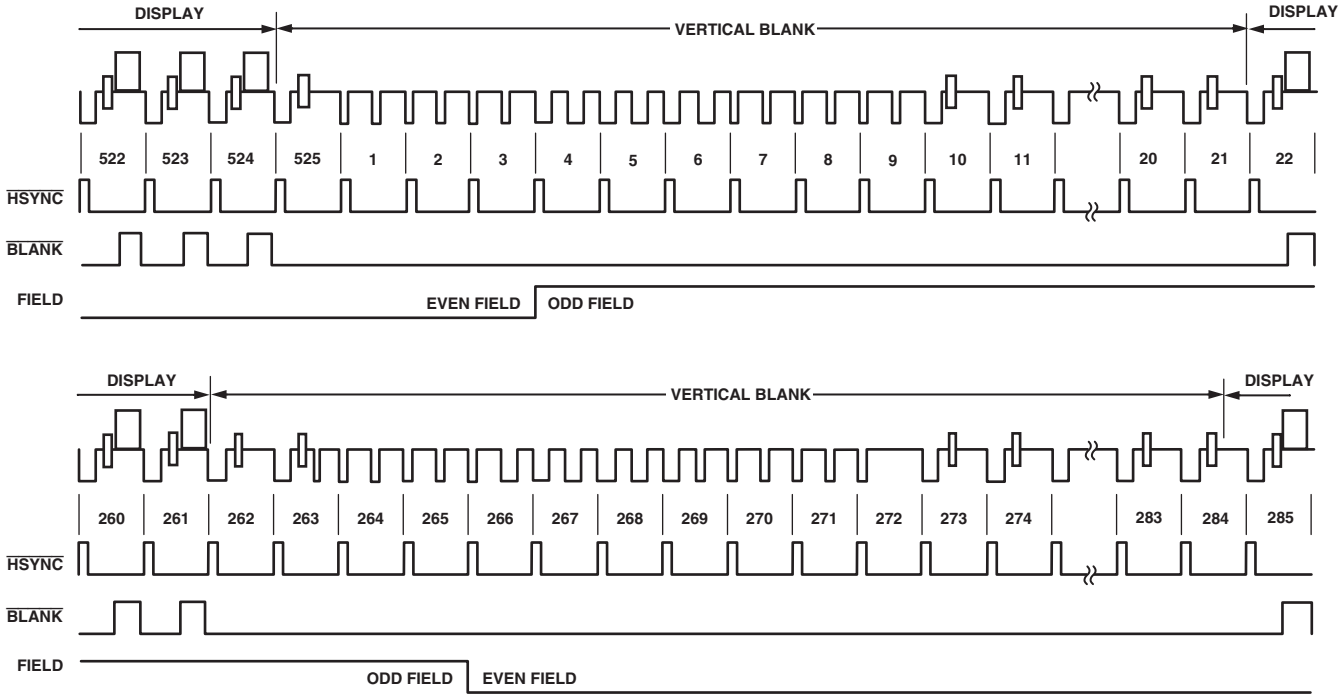


Figure 105. SD Timing Mode 3, NTSC

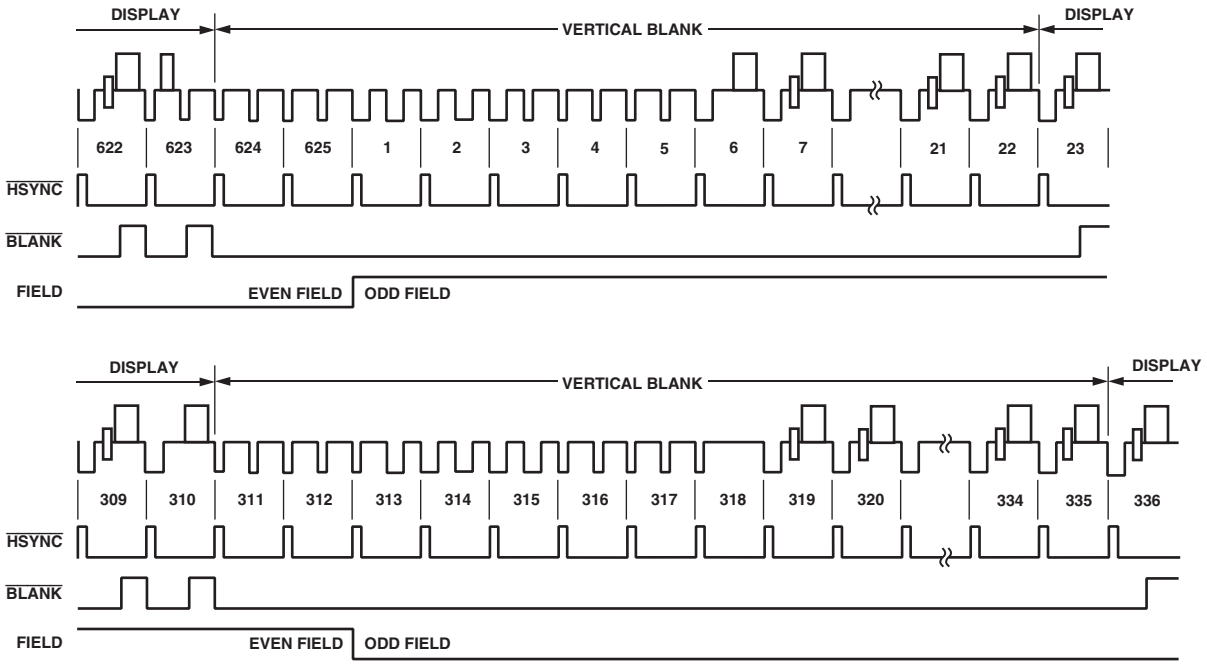


Figure 106. SD Timing Mode 3, PAL

Appendix F

VIDEO OUTPUT LEVELS

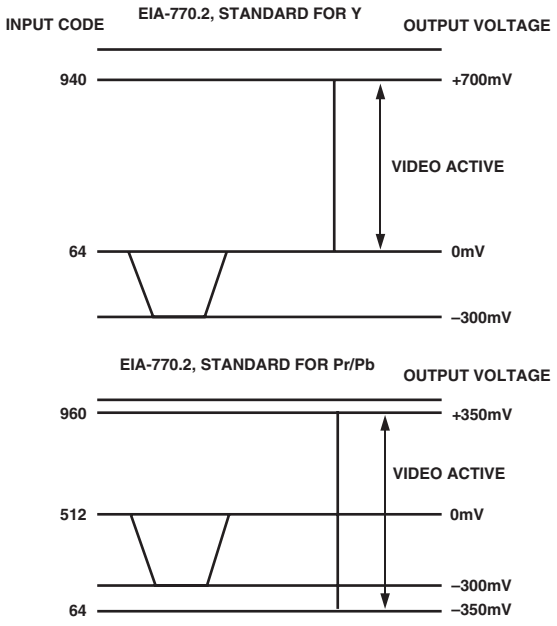


Figure 107. EIA-770.2 Standard Output Signals (525 p)

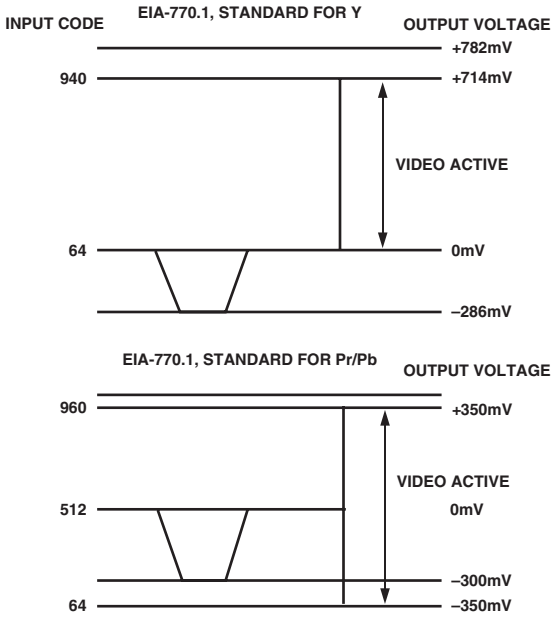


Figure 108. EIA-770.1 Standard Output Signals (525 p)

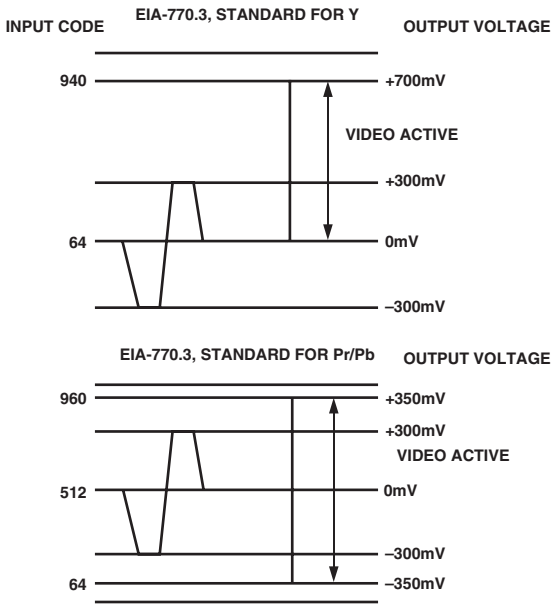


Figure 109. EIA-770.3 Standard Output Signals (1080 i, 720 p)

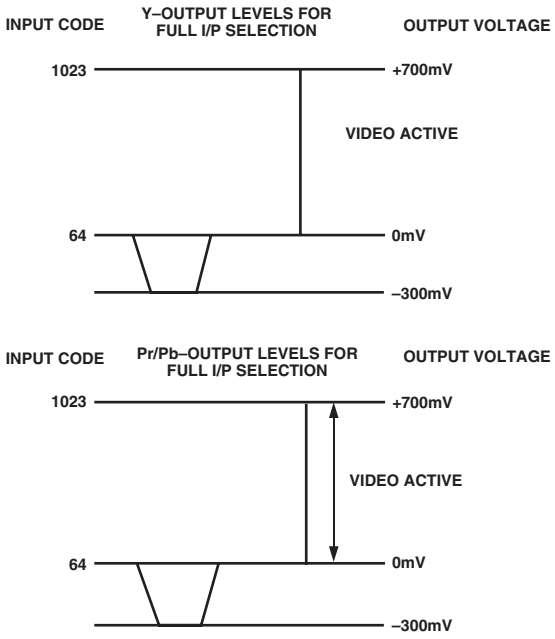
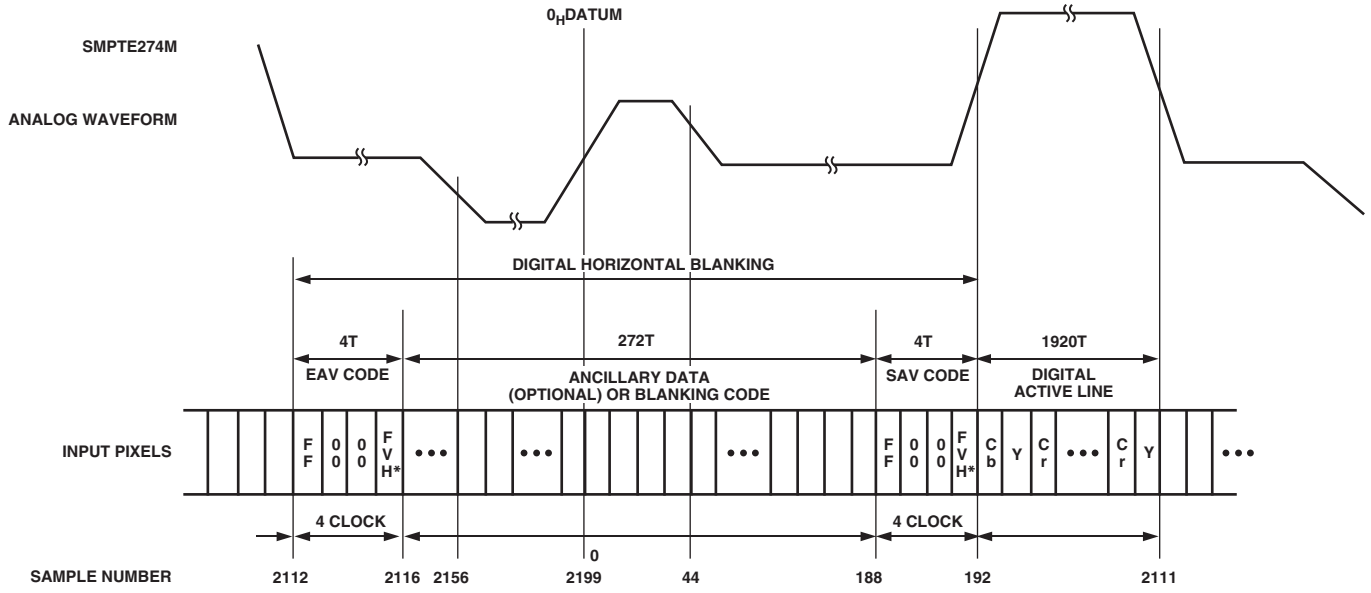


Figure 110. Output Levels for Full Input Selection

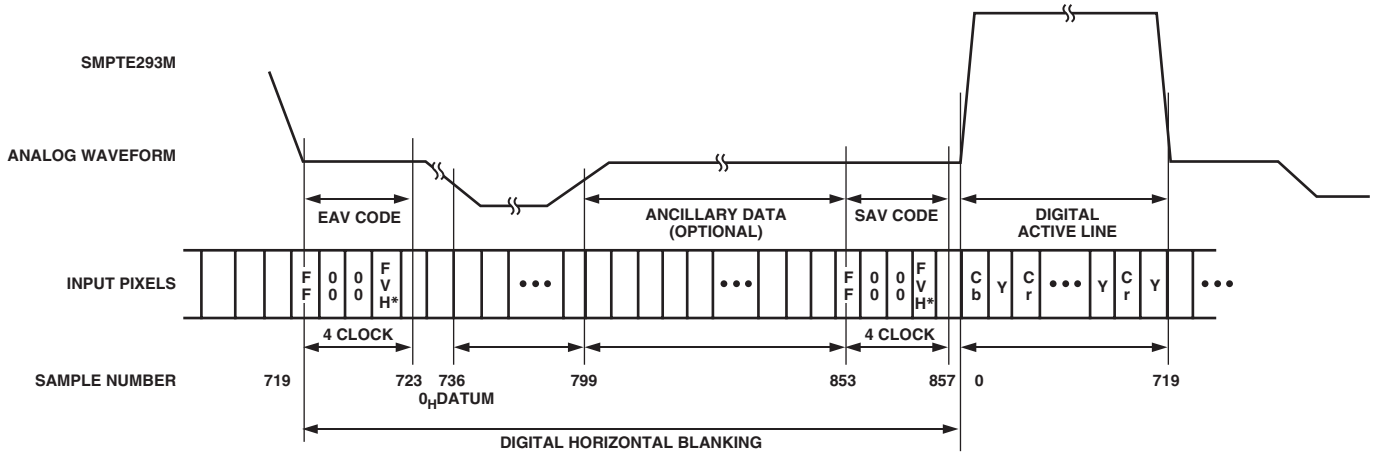
Appendix G

VIDEO STANDARDS



FVH* = FVH AND PARITY BITS
SAV/EAV: LINE 1–562: F = 0
SAV/EAV: LINE 563–1125: F = 1
SAV/EAV: LINE1–20; 561–583; 1124–1125: V = 1
SAV/EAV: LINE 21–560; 584–1123: V = 0

Figure 111. EAV/SAV Input Data Timing Diagram, SMPTE274M



FVH* = FVH AND PARITY BITS
SAV: LINE 43–525 = 200H
SAV: LINE 1–42 = 2AC
EAV: LINE43–525 = 274H
EAV: LINE 1–42 = 2D8

Figure 112. EAV/SAV Input Data Timing Diagram, SMPTE293M

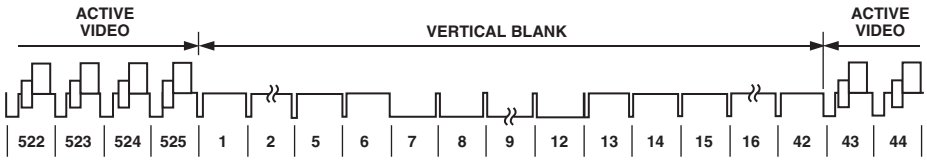


Figure 113. SMPTE293M

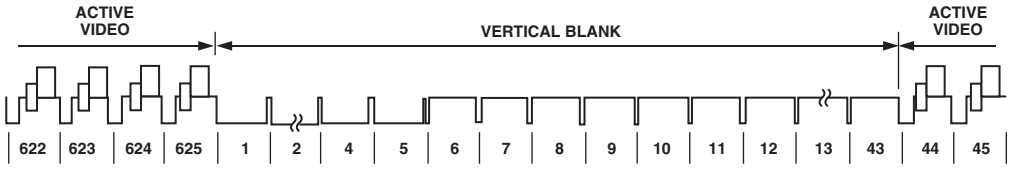


Figure 114. ITU-R.BT1358 (625 p)

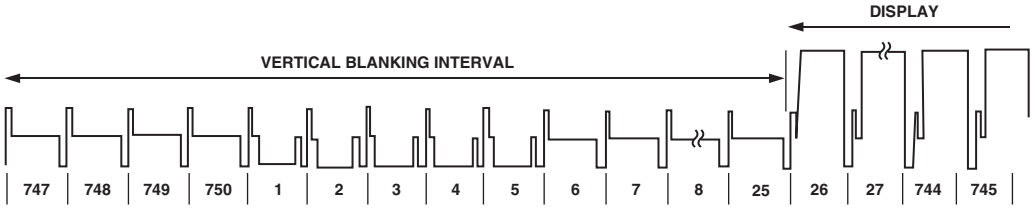


Figure 115. SMPTE296M (720 p)

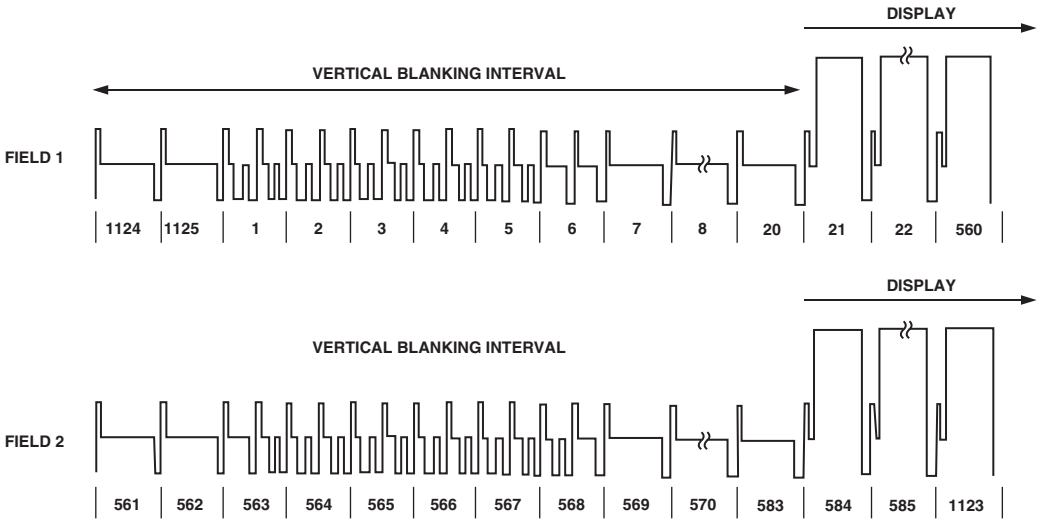
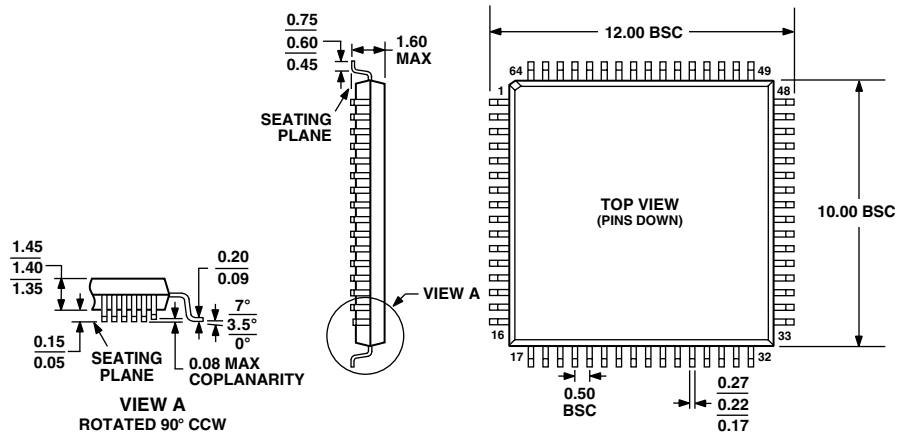


Figure 116. SMPTE274M (1080 i)

OUTLINE DIMENSIONS

64-Lead Thin Plastic Quad Flatpack [LQFP]
(ST-64B)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BCD

C02864–0–11/02(A)

Revision History

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Changes to Table XIII	32
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