



**DS Series  
Encoder/Decoder Module  
Data Guide**

**Wireless made simple<sup>®</sup>**

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**All RF products are susceptible to RF interference that can prevent communication.** RF products without frequency agility or hopping implemented are more subject to interference. This module does not have a frequency hopping protocol built in.

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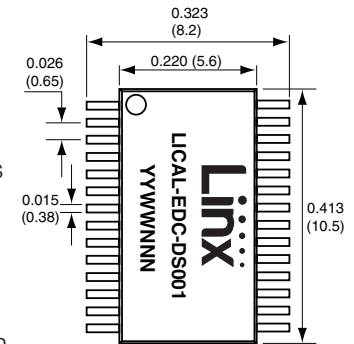
# DS Series Encoder/Decoder

## Data Guide



### Description

The DS Series encoder/decoder is ideal for remote control applications. It is used to transfer the status of up to eight buttons or contacts across a wireless link. Addressing is accomplished by the logic state of 10 pins, typically connected to DIP switches. The encoder and decoder are in the same part, selected by the state of one pin, which is a benefit for volume purchasing and production.



The DS Series also has two protocols built into the same part, selected by the state of a single pin. One is compatible with Holtek® devices, such as the HT640 and HT658. The other protocol is a serial data structure that is much more immune to noise and edge jitter. This protocol offers much more range and reliability than the Holtek® protocol while keeping the simple DIP-switch addressing.

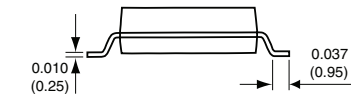


Figure 1: Package Dimensions

The DS Series is configured through hardware, so no programming or software is required. Housed in a tiny 28-pin SSOP package, DS Series parts feature low supply voltage and current consumption.

### Features

- 10 address lines
- 8 data lines
- 2.2 to 5.5V operating voltage
- Low supply current (250µA @ 3V encoder, 400µA @ 3V decoder)
- Ultra-low 0.3µA standby current
- No programmer required
- Small SMD package
- Valid transmission indicator

### Applications

- Door and Gate Openers
- Remote Device Control
- Car Alarms / Starters
- Home / Industrial Automation
- Remote Status Monitoring
- Lighting Control

## Ordering Information

| Ordering Information |                           |
|----------------------|---------------------------|
| Part Number          | Description               |
| LICAL-EDC-DS001      | DS Series Encoder/Decoder |
| EVAL-xxx-DS          | DS Series Evaluation Kit  |

Encoder/Decoders are supplied in tubes of 18 pcs.

Figure 2: Ordering Information

## Absolute Maximum Ratings

| Absolute Maximum Ratings            |      |    |                |     |  |
|-------------------------------------|------|----|----------------|-----|--|
| Supply Voltage $V_{CC}$             | -0.3 | to | +6.5           | VDC |  |
| Any Input or Output Pin             | -0.3 | to | $V_{CC} + 0.3$ | VDC |  |
| Max. Current Sourced By Output Pins |      |    | 25             | mA  |  |
| Max. Current Sunk By Output Pins    |      |    | 25             | mA  |  |
| Max. Current Into $V_{CC}$          |      |    | 250            | mA  |  |
| Max. Current Out Of GND             |      |    | 300            | mA  |  |
| Operating Temperature               | -40  | to | +85            | °C  |  |
| Storage Temperature                 | -65  | to | +150           | °C  |  |

Exceeding any of the limits of this section may lead to permanent damage to the device. Furthermore, extended operation at these maximum ratings may reduce the life of this device.

Figure 3: Absolute Maximum Ratings



**Warning:** This product incorporates numerous static-sensitive components. Always wear an ESD wrist strap and observe proper ESD handling procedures when working with this device. Failure to observe this precaution may result in module damage or failure.

## Electrical Specifications

| DS Series Encoder/Decoder Specifications |             |                |      |                |         |       |
|--|-------------|----------------|------|----------------|---------|-------|
| Parameter                                | Symbol      | Min.           | Typ. | Max.           | Units   | Notes |
| Operating Voltage                        | $V_{CC}$    | 2.2            |      | 5.5            | VDC     |       |
| Encoder Supply Current                   | $I_{CCENC}$ |                |      |                |         |       |
| At 2.2V                                  |             |                | 200  |                | $\mu A$ | 1     |
| At 3.3V                                  |             |                | 250  |                | $\mu A$ | 1     |
| At 5.0V                                  |             |                | 400  |                | $\mu A$ | 1     |
| Decoder Supply Current                   | $I_{CCDEC}$ |                |      |                |         |       |
| At 2.2V                                  |             |                | 300  |                | $\mu A$ | 1     |
| At 3.3V                                  |             |                | 400  |                | $\mu A$ | 1     |
| At 5.0V                                  |             |                | 675  |                | $\mu A$ | 1     |
| Power-Down Current                       | $I_{PDN}$   |                |      |                |         |       |
| At 2.2V                                  |             |                | 0.3  |                | $\mu A$ |       |
| At 3.3V                                  |             |                | 0.3  |                | $\mu A$ |       |
| At 5.0V                                  |             |                | 0.4  |                | $\mu A$ |       |
| Input Low                                | $V_{IL}$    | 0.0            |      | $0.2 * V_{CC}$ | V       | 2     |
| Input High                               | $V_{IH}$    | $0.8 * V_{CC}$ |      | $V_{CC}$       | V       | 3     |
| Output Low                               | $V_{OL}$    | 0.0            |      | 0.6            | V       |       |
| Output High                              | $V_{OH}$    | $V_{CC}-0.7$   |      | $V_{CC}$       | V       |       |
| Input Sink Current                       |             |                |      | 25             | mA      | 4     |
| Output Drive Current                     |             |                |      | 25             | mA      | 4     |
| Operating Temp. Range                    |             | -40            |      | +85            | °C      |       |
| Response Time                            |             |                |      |                |         |       |
| Holtek Protocol                          |             |                | 135  |                | ms      |       |
| Serial Protocol                          |             |                | 40   |                | ms      |       |

- Current consumption with no active loads.
- For 3V supply,  $(0.15 * 3.0) = 0.45V$  max.
- For 3V supply,  $(0.8 * 3.0) = 2.4V$  min.
- Total current = 300mA

Figure 4: Electrical Specifications

## Pin Assignments

|    |                   |         |    |
|----|-------------------|---------|----|
| 1  | P_SEL             | DOUT/VT | 28 |
| 2  | D0                | TE/DIN  | 27 |
| 3  | D1                | A9      | 26 |
| 4  | D2                | A8      | 25 |
| 5  | D3                | A7      | 24 |
| 6  | D4                | A6      | 23 |
| 7  | D5                | A5      | 22 |
| 8  | GND               | A4      | 21 |
| 9  | D6                | VCC     | 20 |
| 10 | D7                | GND     | 19 |
| 11 | E/ $\bar{D}$ _SEL | A3      | 18 |
| 12 | D_CFG             | A2      | 17 |
| 13 | A_CFG0            | A1      | 16 |
| 14 | A_CFG1            | A0      | 15 |

Figure 5: DS Series Encoder/Decoder Pinout (Top View)

## Pin Descriptions

| Pin Descriptions                       |                   |     |  |
|--|-------------------|-----|--|
| Pin Number                             | Name              | I/O | Description  |
| 1                                      | P_SEL             | I   | Protocol Selection. The state of this line determines the data structure and protocol used by the encoder / decoder. Pull low to use the Holtek data structure, pull high to use the serial structure.   |
| 2, 3, 4, 5, 6, 7, 9, 10                | D0 – D7           | I/O | Data Lines. When in Encoder Mode, the states of these lines are captured when the TE line goes high and are encoded for transmission. When in Decoder Mode, these lines reproduce the states of the encoder's data lines upon reception of a valid packet.   |
| 8, 19                                  | GND               |     | Ground   |
| 11                                     | E/ $\bar{D}$ _SEL | I   | Encoder/Decoder Select. The state of this line determines if the DS is an encoder or a decoder. If the line is high, then the DS enters Encoder Mode. If the line is low, then it enters Decoder Mode. This line is checked once upon power up.  |
| 12                                     | D_CFG             | I   | Data Line Configuration. Determines whether a low on a data line is interpreted as a zero bit or an open bit. See the Input Type Selection section.  |
| 13                                     | A_CFG0            | I   | Address Configuration 0. With A_CFG1, determines the address bit type interpretation. See the Input Type Selection section.  |
| 14                                     | A_CFG1            | I   | Address Configuration 1. With A_CFG0, determines the address bit type interpretation. See the Input Type Selection section.  |
| 15, 16, 17, 18, 21, 22, 23, 24, 25, 26 | A0–A9             | I   | Address Lines. The DS has ten address lines that are used to set a local address.  |
| 20                                     | VCC               |     | This is the positive power supply.   |
| 27                                     | TE/DIN            | I   | When in Encoder Mode, this line is the Transmit Enable line. When it is pulled high, the encoder records the states of the data and address lines, assembles them into a packet, and outputs the packet on the DOUT line three times. When in Decoder Mode, this line is the data input from the receiver. |
| 28                                     | DOUT/VT           | O   | When in Encoder Mode, this line is the data output that is connected to the transmitter. When in Decoder Mode, this line is the Valid Transmit indicator and goes high when a valid packet is received.  |

Figure 6: DS Series Encoder/Decoder Pin Descriptions

**Warning:** None of the input lines have internal pull-up or pull-down resistors. The input lines must always be in a known state (either GND or  $V_{CC}$ ) at all times or the operation may not be predictable. The designer must ensure that the input lines are never floating, either by using external resistors, by tying the lines directly to GND or  $V_{CC}$ , or by use of other circuits to control the line state.

## Theory of Operation

The DS Series is a remote control encoder and decoder that offers two protocols in one part based on the state of the P\_SEL line. The first protocol operates with the Holtek® HT640 encoder and HT658 decoder. The second is a serial protocol that offers more noise immunity and faster response time while keeping the simple addressing. The DS can operate as either an encoder or decoder based on the state of the E/ $\overline{D}$ \_SEL line. It does not operate as both simultaneously.

When set as an encoder it monitors the state of the TE line. When the line is high the DS records the states of the data and address lines, assembles them into a packet and outputs the packet three times. The data lines can be connected to switches or contacts. The address lines can be set with DIP switches or cut traces on a PCB.

When set as a decoder the DS receives packets and validates them. The validation includes checking the bit timings and comparing the received address to the local address line settings. Two matching packets must be received consecutively. If the timings are good and the addresses match, the DS sets its data lines to match the received states. These lines can be connected to the application circuitry to be controlled.

When the TE/DIN line is low, the DS goes into a low power sleep mode.

**Note:** The input lines on the DS are not tri-state. They must be pulled high or low and cannot be left floating. This is a key difference between the DS and the Holtek® parts.

## Setting the Address

The DS Series has ten address lines. This allows the formation of up to 1,022 ( $2^{10} - 2$ ) unique transmitter-receiver relationships.

**Note:** The DS decoder rejects packets with addresses set to all high or all low. At least one address line must be different from the rest. The encoder does transmit all addresses, but the decoder rejects packets with all address lines set the same.

These lines may be hardwired or configured via a microprocessor, DIP switch or jumpers. The receiver's address line states must match the transmitter's exactly for a transmission to be recognized. If the addresses do not match, then the decoder takes no action.

## Initial Operation

On power-up, the E/ $\overline{D}$ \_SEL line is tested to determine if the DS operates as an encoder or a decoder. If the line is high, the DS enters Encoder Mode. If low, it enters Decoder Mode. This is checked once on power-up. Once the operating mode is selected, the data-line direction is set. In either mode a rising edge on the TE/DIN line wakes the device from low-power sleep.

## Encoder Mode

Once the DS enters Encoder Mode, it tests the state of the TE line. If it is high, the P\_SEL line is checked to determine which protocol to use. Then the encoder records the states of the Data and Address lines and assembles a packet. When the Holtek® protocol is selected, the DS outputs the packet on the DOUT line three times. With the Serial protocol, it sends two packets, checking the states of the data lines each time. The second packet is the logical inversion of the first packet, ensuring a 50% duty cycle, which is an advantage for FCC testing. The DS then checks the state of the TE line again. It repeats this process for as long as the TE line is high. Once it goes low, the DS goes to sleep until TE is pulled high.

## Decoder Mode

When the DS enters Decoder Mode, it checks the state of the DIN line. If it is high, the P\_SEL line is checked to set which protocol is used and the decoder receives the data. It compares the address in the received packet to its local address lines. If they match, the data is stored and a second packet is received. With the Holtek® protocol, the decoder compares the two packets. If they match, the received data bits are output on the data lines and the VT line is pulled high. This protocol compares each packet with the previous one looking for a match. The serial protocol requires two matching packets for initial activation, then updates the lines on each subsequent packet. The DS then looks for the next packet on the DIN line.

With the Holtek® protocol, once no valid data is received (there is a mismatch of address, data, or bit timings), the Data and VT lines are pulled low and the DS goes to sleep until DIN is pulled high. The Serial protocol holds the output states until a 130ms timer runs out.

The Holtek® protocol compares two packets and, if they match, sets the outputs. If a data line is toggled during a transmission (D1 is activated while D0 is already active) then the received packet does not match the previous packet and the output lines are pulled low until the next packet arrives. This causes all of the outputs to briefly cut out when a line is toggled. The serial protocol uses a timer to prevent this cut out.

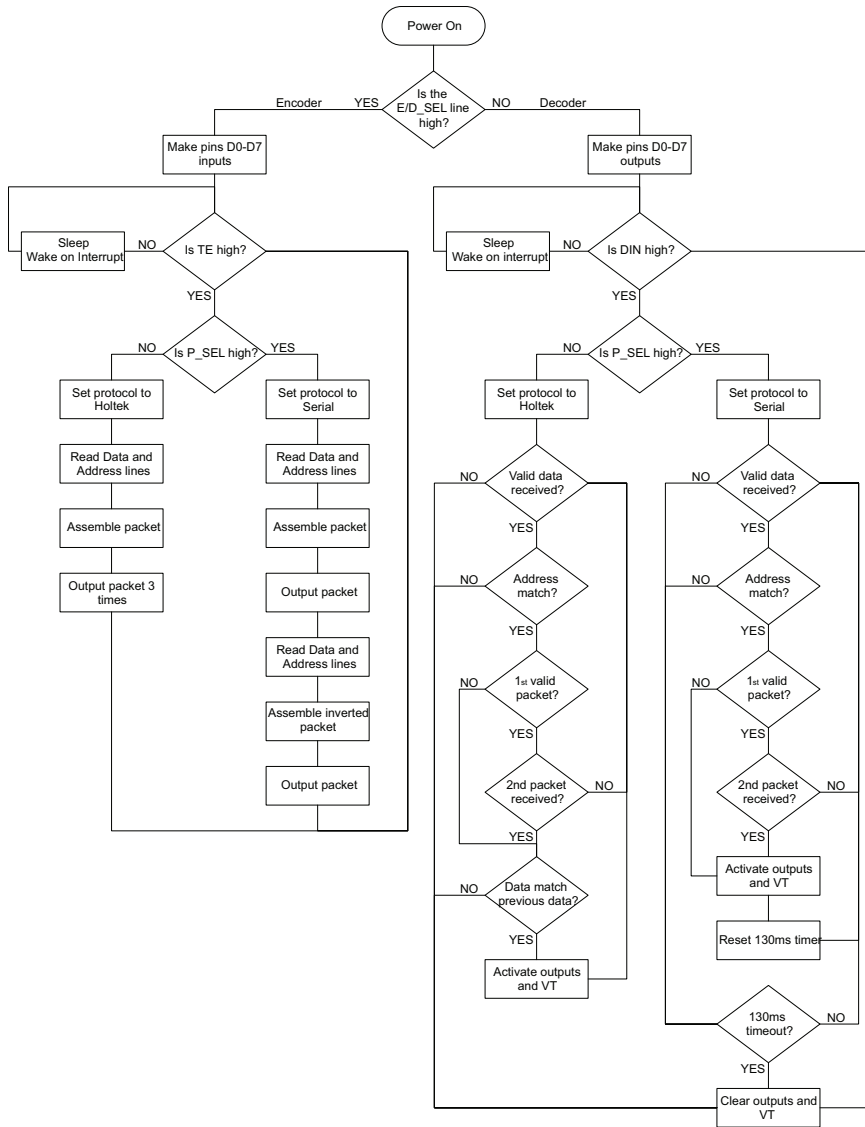


Figure 7: DS Series Encoder/Decoder Flowchart

## Holtek Data and Packet Structure

The Holtek® encoders and decoders have tri-state input lines. They recognize three distinct states: one, zero and open. A one bit is set when the line is at  $V_{CC}$ . A zero bit is set when the line is at ground. An open bit is set when the line is not connected or floating.

The Holtek® encoders and decoders use a pattern of two logic high pulses and two logic low pulses for each bit. Two of the pulses are double sized and the pattern indicates the type of bit. This is shown in Figure 8.

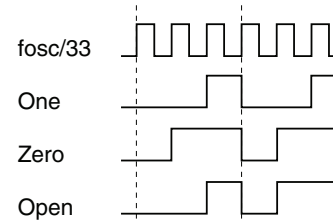


Figure 8: Holtek® Protocol Input Interpretation

Each data packet consists of 6-bit pilot period (logic low), 2-bit SYNC period, and 18-bit code period, as shown in Figure 9.

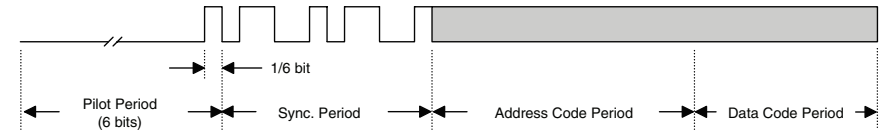


Figure 9: Holtek® Protocol Packet Structure

Example packets are shown in Figure 10 with all lines set in a specific state.

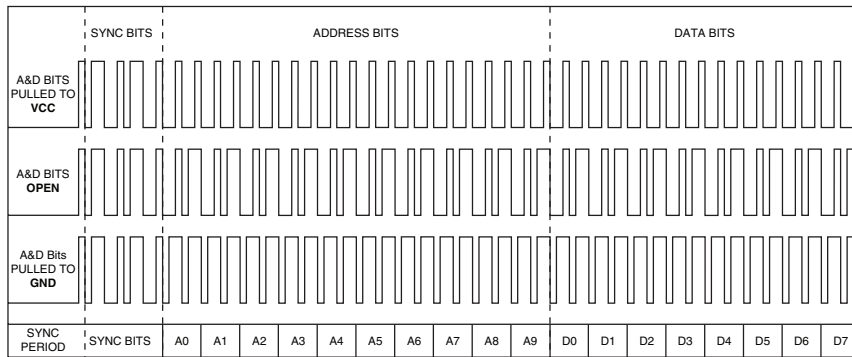


Figure 10: Holtek® Protocol Timing

Figure 11 shows the timings associated with the Holtek® protocol.

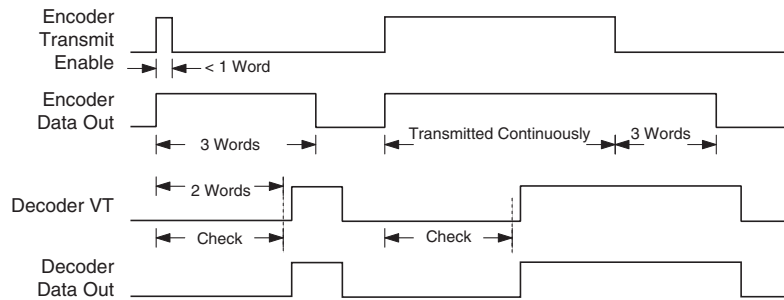


Figure 11: DS Series Timing

## Input Type Selection

The DS Series is designed to be operable with Holtek® encoders and decoders, but there is one key condition. The Holtek® encoders and decoders have tri-state input lines but the DS has bi-state lines. Tri-state inputs are connected to ground for zero bits,  $V_{CC}$  for one bits, or left unconnected for open bits. Since the DS cannot match this operation the D\_CFG, A\_CFG0 and A\_CFG1 lines are provided to select the desired interpretation. The settings must match on both ends.

Pulling D\_CFG high configures the data inputs as one and zero. A high on a data line is interpreted as a one bit and a low on the line is interpreted as a zero bit. Pulling D\_CFG low configures the data inputs as one and open. A high on a data line is interpreted as a one bit and a low on the line is interpreted as an open bit. The decoder outputs open data bits as logic low. This is shown in Figure 12.

| D_CFG Configuration |                    |      |     |
|---------------------|--------------------|------|-----|
| Configuration       | Bit Interpretation |      |     |
|                     | D_CFG              | High | Low |
| 0                   | One                | Open |     |
| 1                   | One                | Zero |     |

Figure 12: D\_CFG Configuration

A\_CFG0 and A\_CFG1 are used to select the bit type for the address lines. These are shown in Figure 13.

| A_CFG0 and A_CFG1 Configuration |        |                    |      |
|---------------------------------|--------|--------------------|------|
| Configuration                   |        | Bit Interpretation |      |
| A_CFG1                          | A_CFG0 | High               | Low  |
| 0                               | 0      | One                | Zero |
| 0                               | 1      | One                | Open |
| 1                               | 0      | Open               | Zero |
| 1                               | 1      | One                | Zero |

Figure 13: A\_CFG0 and A\_CFG1 Configuration

Products that need to operate with the older Holtek products need to set these configuration lines according to how the Holtek® encoders and decoders are implemented in the product.



## Serial Data and Packet Structure

The serial protocol encodes the address and data lines as binary bits that follow logic low and logic high voltage levels. The logic states of each line are recorded and placed into bytes. A checksum is calculated on the bytes and appended to the end of the packet. A preamble and a noise filter are added to the front. The packet is shown in Figure 14.

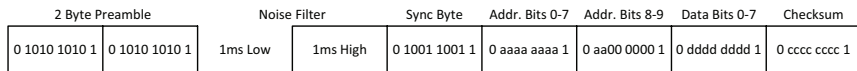


Figure 14: Serial Protocol Packet Structure

The bytes are output in serial fashion at 4,800bps. The DS outputs the packet twice, with the second packet being the logical inversion of the first. This ensures that the duty cycle of the data is always 50%. Adding in the blanking period between packets lowers the duty cycle. This is important for FCC certification where the transmitter output power level is a function of the data duty cycle.

This protocol only uses binary states, so the D\_CFG, A\_CFG0 and A\_CFG1 lines are ignored.

The serial protocol is much more immune to bit edge jitter than the Holtek® protocol. This gives much better range and performance within that range. This also gives the DS better immunity to noise from motors, switching power supplies, high current drivers and other noise sources.

This protocol updates the data line states on every packet. This, combined with a faster data rate, give the serial protocol a much faster response time than the Holtek® protocol (36.5ms typical compared to 135ms).

The serial protocol compares two packets as part of the data validation, but also includes a timer that keeps the outputs stable in the case of mismatched packets. This prevents the outputs from turning off at the loss of one packet or when a data line is toggled while another one is active. This helps prevent chattering of relays and other electro-mechanical devices that are not designed for rapid switching. The outputs turn off after 130ms with no valid data.

## Operation with the Holtek® HT640 and HT658

The DS is fully compatible with the Holtek® HT640 encoder and the HT658, and HT648L decoders. The primary operational difference is that the DS Series has bi-state address lines (high or low) while the Holtek® parts have tri-state lines (high, low or floating). Since these are distinct states for the Holtek® parts, three configuration lines are used to select how the inputs are interpreted. This accommodates most applications using the Holtek® parts.

**Note:** Contact Linx for compatibility with other Holtek® encoder/decoder products.

The states of the A\_CFG0 and A\_CFG1 lines determine how the DS Series interprets the states of its address lines. These lines allow for the use of any two of Holtek®'s three states at a time. The states are outlined in Figure 13.

The state of the D\_CFG line determines how the DS Series interprets the states of its data lines when in Encoder Mode. This allows for the use of any two of Holtek®'s three states at a time. The states are outlined in Figure 12.

While the DS Series is not fully compatible with the Holtek® parts because of the lack of tri-state lines, the use of the configuration lines allows most applications to make a seamless transition to the DS.

## Encoder Typical Application

Figure 15 shows a circuit using the DS Series configured as a Holtek® encoder. This configuration matches the Linx OEM products.

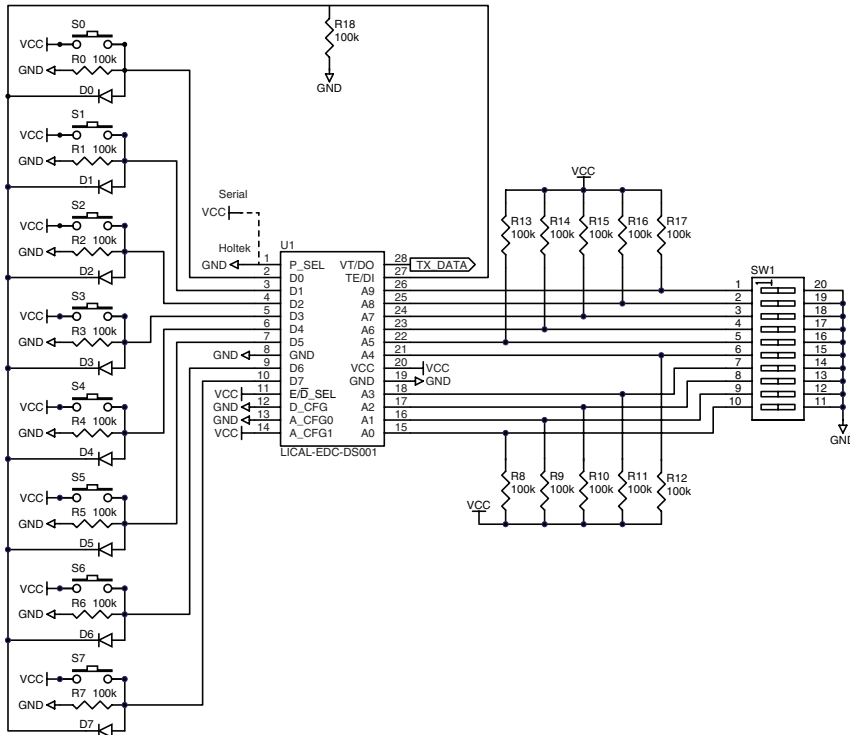


Figure 15: DS Series Typical Application as an Encoder

The P\_SEL line is set to Holtek® data (pulling it to Vcc selects the Serial protocol). The E/D\_SEL line is pulled high to place the DS into Encoder Mode. The D\_CFG is set so that a high on a data line is transmitted as a one bit and a low on the line is transmitted as an open bit. The A\_CFG0 and A\_CFG1 lines are set to give a high on an address line as an open bit and a low as a zero bit.

The data lines are bi-state, so they have to be high or low. They cannot be floating. Resistors to ground pull the lines low and buttons pull the lines high when pressed. Diodes are used to pull TE high when any button is pressed without activating any other line. This way, pushing any button causes the encoder to start outputting data.

The address lines are bi-state, so they have to be high or low. They cannot be floating. Resistors pull the lines high and DIP switches pull them low.

## Decoder Typical Application

Figure 16 shows a circuit using the DS Series configured as a Holtek® decoder. This configuration matches the Linx OEM products.

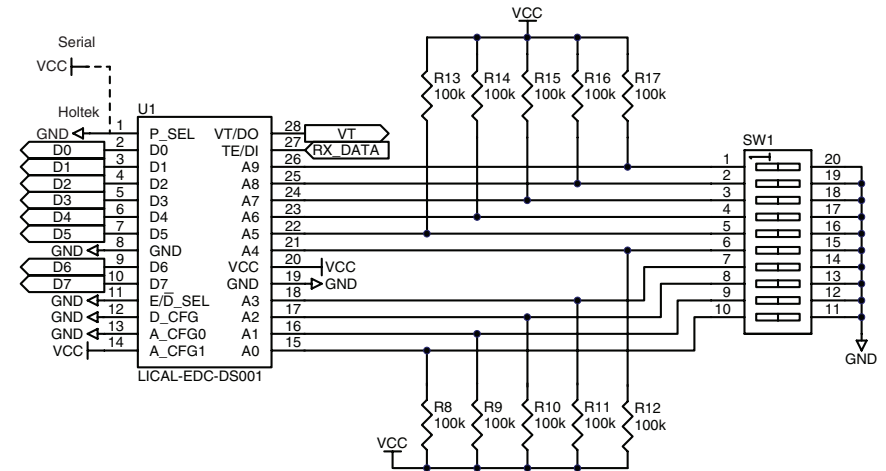


Figure 16: DS Series Typical Application as a Decoder

The P\_SEL line is set to Holtek® data. The E/D\_SEL line is pulled low to place the DS into decoder mode. The A\_CFG0 and A\_CFG1 lines are set to give a high on an address line as an open bit and a low as a zero bit.

The address lines are bi-state, so they have to be high or low. They cannot be floating. Resistors are used to pull the lines high and DIP switches pull them low when on.

Pulling the P\_SEL line to Vcc enables the serial protocol. The rest of the application circuit is the same, though the D\_CFG, A\_CFG0 and A\_CFG1 lines are ignored and can be tied to Vcc or GND with no effect on the operation. They should not be left open.

## Recommended Pad Layout

The DS Series encoder/decoder is implemented in a 28-pin Shrink Small Outline Package (28-SSOP). The recommended layout dimensions are in Figure 17.

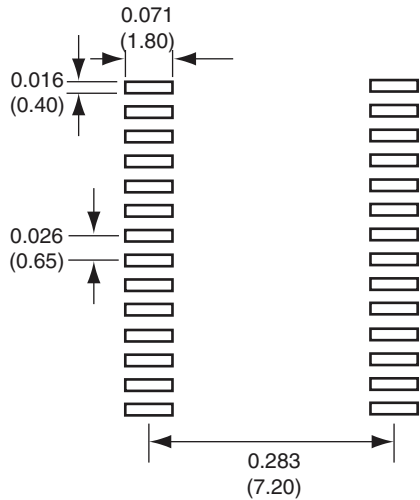


Figure 17: Recommended Footprint

## Production Guidelines

These surface-mount components are designed to comply with standard reflow production methods. The recommended reflow profile is shown in Figure 18 and should not be exceeded, as permanent damage to the part may result.

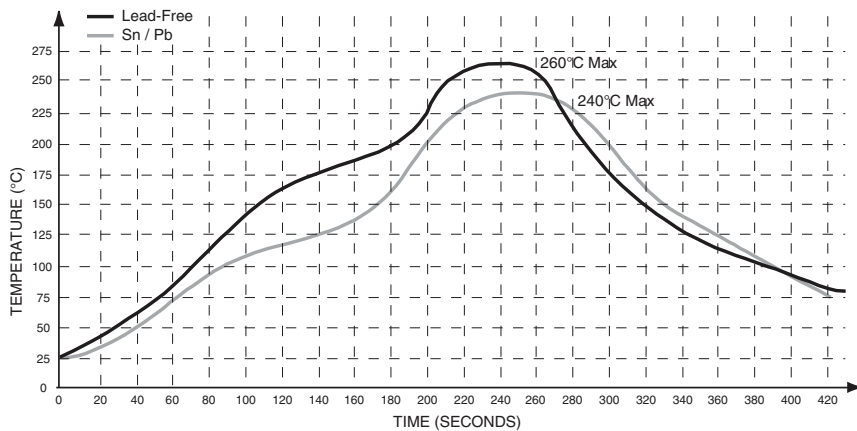


Figure 18: Recommended Solder Profile

## Helpful Application Notes from Linx

It is not the intention of this manual to address in depth many of the issues that should be considered to ensure that the modules function correctly and deliver the maximum possible performance. As you proceed with your design, you may wish to obtain one or more of the following application notes which address in depth key areas of RF design and application of Linx products. These application notes are available online at [www.linxtechnologies.com](http://www.linxtechnologies.com) or by contacting Linx.

| Helpful Application Note Titles |   |
|---------------------------------|---|
| Note Number                     | Note Title  |
| AN-00300                        | Addressing Linx OEM Products                          |
| AN-00310                        | Encoder and Decoder Comparison                        |
| AN-00320                        | The Basics of Remote Control and Remote Keyless Entry |

Figure 19: Helpful Application Notes

## Resources

### Support

For technical support, product documentation, application notes, regulatory guidelines and software updates, visit [www.linstechnologies.com](http://www.linstechnologies.com)

### RF Design Services

For customers who need help implementing Linx modules, Linx offers design services including board layout assistance, programming, certification advice and packaging design. For more complex RF solutions, Apex Wireless, a division of Linx Technologies, creates optimized designs with RF components and firmware selected for the customer's application. Call +1 800 736 6677 (+1 541 471 6256 if outside the United States) for more information.

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## Notes



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