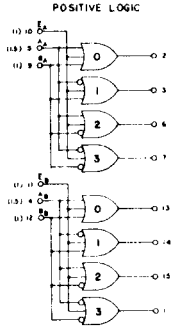
MC1042

Advance Information

POSITIVE LOGIC



2 = 10 + 9 + 5
3 = 10 + 9 + $\overline{5}$
6 = 10 + $\overline{9}$ + 5
7 = 10 + $\overline{9}$ + $\overline{5}$

13 = 11 + 12 + 4
14 = 11 + $\overline{12}$ + 4
15 = 11 + $\overline{12}$ + $\overline{4}$
1 = 11 + $\overline{12}$ + $\overline{4}$

Numbers In Parenthesis = DC Input Loading Factor
DC Output Loading Factor = 25
Power Dissipation = 245 mW typ

The MC1042 is a dual monolithic device that converts a 2-bit binary code to one-line of four decimal output. An enable line is provided to inhibit decoding when it is raised to a high level. MC1042 is packaged in a 16-pin dual in-line package.

TRUTH TABLE

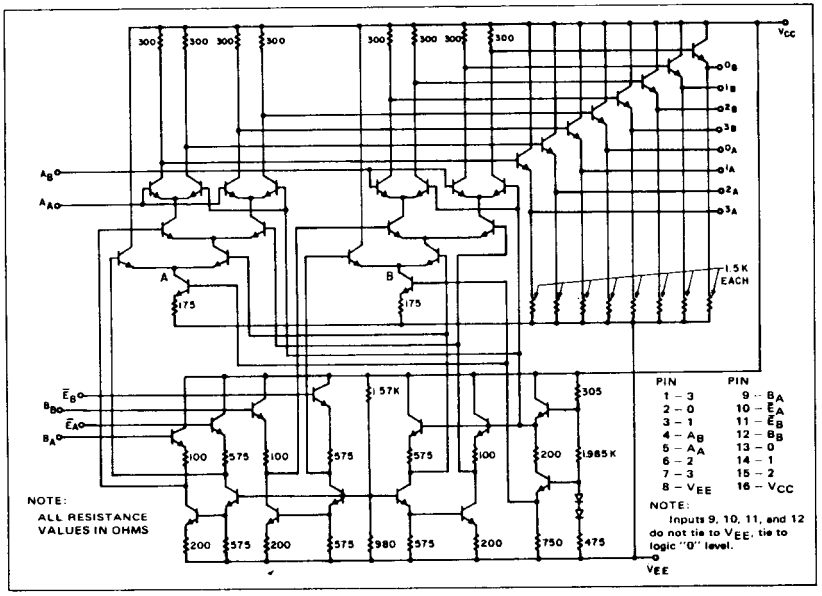
Inputs			Outputs			
E_A	B_A	A_A	0_A	1_A	2_A	3_A
10	9	5	2	3	6	7
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	*	*	1	1	1	1

Pin No.

Inputs			Outputs			
E_B	B_B	A_B	0_B	1_B	2_B	3_B
11	12	4	13	14	15	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	*	*	1	1	1	1

*either state

CIRCUIT SCHEMATIC



NOTE:
ALL RESISTANCE VALUES IN OHMS

PIN	PIN
1 – 3	9 – B_A
2 – 0	10 – $\overline{E}_A$
3 – 1	11 – $\overline{E}_B$
4 – A_B	12 – B_B
5 – A_A	13 – 0
6 – 2	14 – 1
7 – 3	15 – 2
8 – V_{EE}	16 – V_{CC}

NOTE:
Inputs 9, 10, 11, and 12 do not tie to V_{EE}, tie to logic "0" level.

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MC1042 (continued)

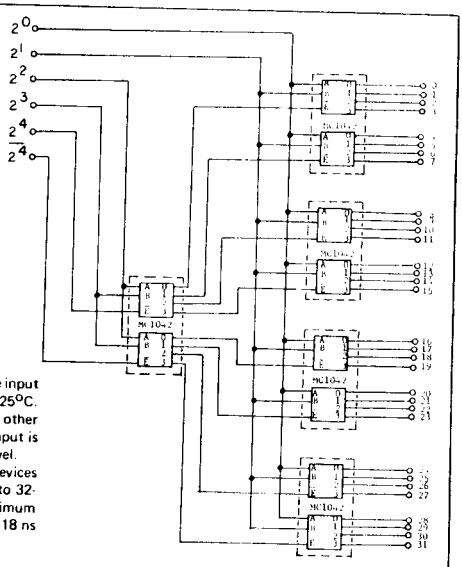
ELECTRICAL CHARACTERISTICS @ 25°C						TEST VOLTAGE VALUES (Volts)					
Characteristics	Symbol	Pin Under Test	Test Limits min.	Test Limits max.	Unit	-1.500	-5.2	-5.2	-5.2	Gnd	-5.2
						VIL	VIH	OR max.	VEE	VCC	VB
Power Supply Drain Current	IE	8	-	61	mAdc	4,5,9,10,11,12	-	-	8	16	-
Input Current	1.5 I_{in}	5	-	150	μAdc	4,10,11,12	5	5	8	16	-
		5	-	150	μAdc	4,9,10,11,12	5	5	8	16	-
	**I_{in}	9,10	-	100	μAdc	4,5,11,12	-	9,10	8	16	-
Input Leakage Current	**IR	5,9,10	-	1.0	μAdc	4,11,12	-	-	8,5,9,10	16	-
Logic "1" Output Voltage	VOH	2,3 6,7	-0.850	-0.700	Vdc	Apply Input Conditions per Truth Table			8	16	2,3,6,7
Logic "0" Output Voltage	VOL	2,3 6,7	-1.800	-1.500	Vdc				8	16	-

* Logic "1" Limits Apply From No Load to Full Load (-2.5 mAdc)

Note: Test Procedures are shown for only one 2-4 Line Decoder, other Decoder is tested in a Similar Manner.

**Individually test each input using the pin connections shown.

Switching Speed (Fan-Out = 15pF)	Symbol	Pin Under Test	AC Parameters (Typical)	Unit	VIL +1.2 Vdc	VIH +1.2 Vdc	Pulse In	VEE -4.0 Vdc	VCC +1.2 Vdc	Pulse Out
Propagation Delay	t5-2-	2,5	6.0	nsec	9,10		5	8	16	2
	t9-2-	2,9	8.0		5,10		9			
	t10-2-	2,10	12.0		5,9		10			
	t5+2+	2,5	5.0		9,10		5			
	t9+2+	2,9	6.5		5,10		9			
	t10+2+	2,10	9.0		5,9		10			
Rise Time	t2+	2	4.0		9,10		5			
Fall Time	t2-	2	9.0		9,10		5			
Propagation Delay	t5+7-	5,7	6.0		10	9	5			7
	t9+7-	7,9	7.0		10	5	9			
	t5-7+	5,7	5.0		10	9	5			
	t9-7+	7,9	6.5		10	5	9			
Rise Time	t7+	7	4.0		10	9	5			
Fall Time	t7-	7	9.0		10	5	9			



APPLICATION INFORMATION

The MC1042 dual 2-4 line decoder with an enable input has very fast decoding time, typically 6.0 ns @ +25°C. When the selected output is at a logic "0" level all other outputs are at a logic "1" level. When the enable input is at a logic "1" level all outputs will be at logic "1" level.

The illustrated application shows five MC1042 devices connected to perform fast decoding of 5-bit binary to 32-line decimal by utilizing the enable inputs. Maximum delay time on this 5 to 32-line decoder is typically 18 ns @ +25°C.