AK8859VQ

NTSC/PAL/SECAM Digital Video Decoder

Overview

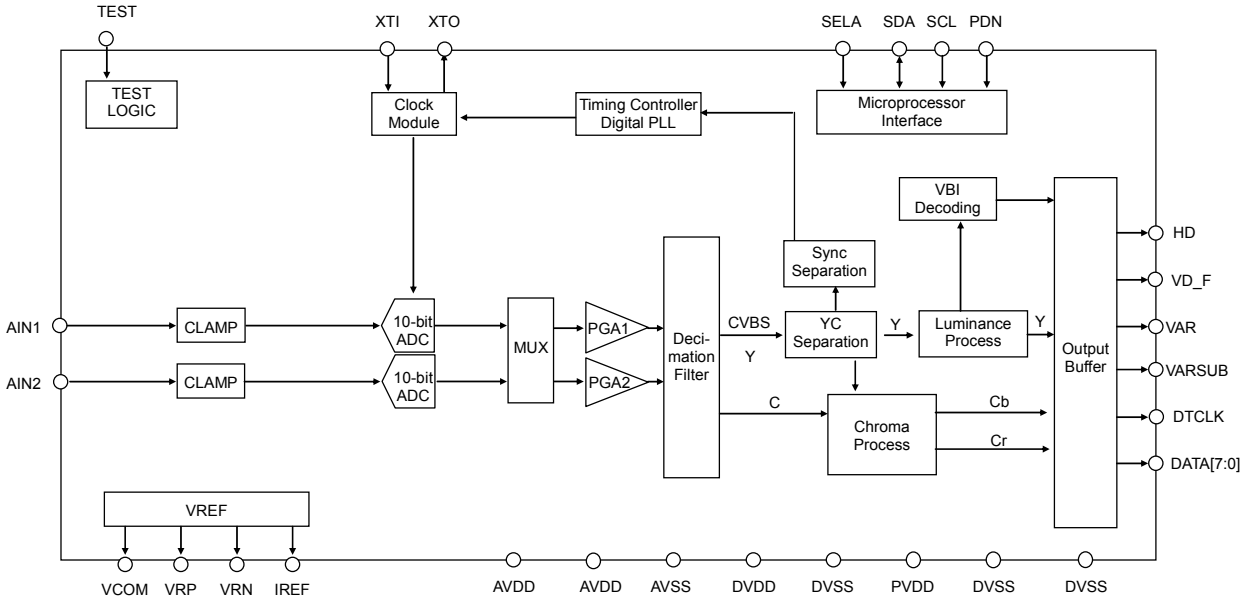
The AK8859VQ is a single-chip digital video decoder for composite and S-video signals. Its output data is in YCbCr format and compliant with ITU-R BT.601 and ITU-R BT.656 standard interface. Its output also included HD / VD / FIELD and DVALID signals. Its operational temperature is between ranges of -40°C ~ 105°C. Microprocessor access is via I^2C interface.

Features

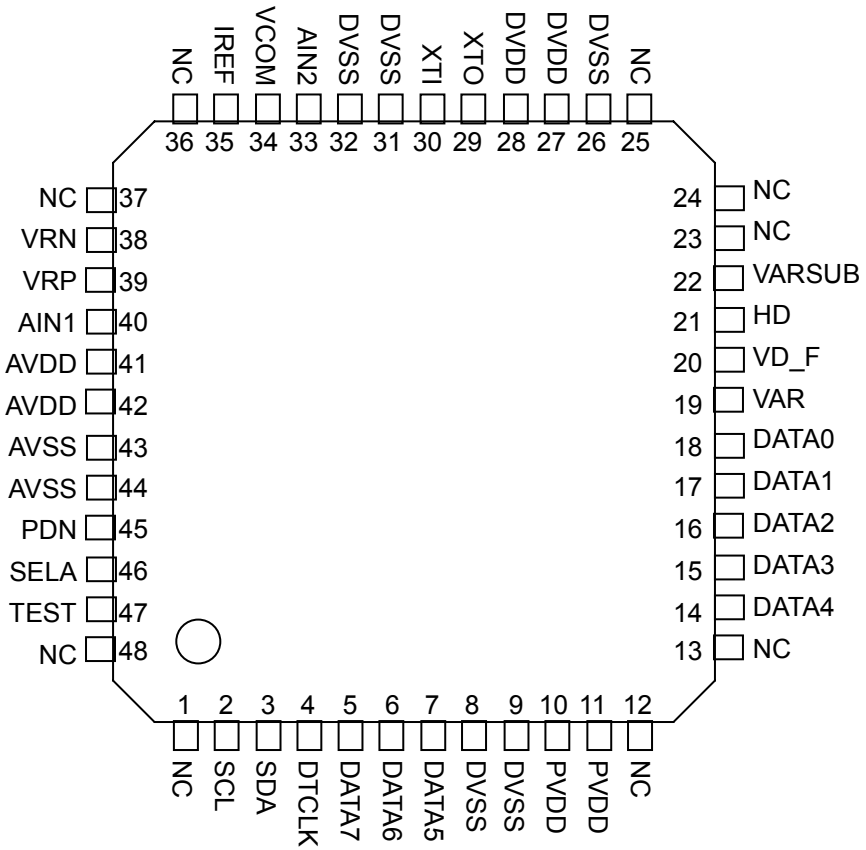
- Decodes composite and S-Video signals NTSC-J, M, 4.43 / PAL-B, D, G, H, I, N, Nc, M, 60 / SECAM
- 2 input channel
- 10-bit 27MHz ADC 2 channel
- Digital PGA
- Adaptive Automatic Gain Control (AGC)
- Auto Color Control (ACC)
- Image adjustment (Contrast, Saturation, Brightness, Hue, Sharpness)
- Automatic input signal detection
- Adaptive 2-D Y/C separation
- Output data format: ITU-R BT.601 (YCbCr, 4:2:2, 8bit)
- Output interface: ITU-R BT.656 (4:2:2, 8bit parallel) with EAV/SAV
  HD, VD, FIELD and DVALID signal timing output
- Closed Caption signal decoding (output via register)
- VBID (CGMS-A) signal decoding (output via register)
- WSS signal decoding (output via register)
- Macrovision signal detection (Macrovision certification)
- Powerdown function
- I^2C control
- Core supply voltage: 1.70 ~ 2.00V
- I/O power supply: 1.70 ~ 3.60V
- Operating temperature: -40°C ~ 105°C
- 48-pin LQFP package (7.0mm x 7.0mm)

Contents

[1.] Functional block diagram



[2.] Pin assignment



[3.] Pin function description
[3.1.] Pin function

Pin No.	Symbol	P/S	I/O	Functional Description
1	NC	-	-	Open
2	SCL	P	I	I^2C clock input pin. Connect to PVDD via a pull-up register. Hi-z input possible when PDN=L.
3	SDA	P	I/O	I^2C data pin. Connect to PVDD via a pull-up register. Hi-z input possible when PDN=L.
4	DTCLK	P	O	Data clock output pin. The output clock is approximately 27MHz.
5	DATA7	P	O (I/O)	DATA output pin (MSB).
6	DATA6	P	O (I/O)	DATA output pin.
7	DATA5	P	O (I/O)	DATA output pin.
8	DVSS	D	G	Digital ground pin.
9	DVSS	D	G	Digital ground pin.
10	PVDD	P	P	I/F power supply pin.
11	PVDD	P	P	I/F power supply pin.
12	NC	-	-	Open
13	NC	-	-	Open
14	DATA4	P	O (I/O)	DATA output pin.
15	DATA3	P	O (I/O)	DATA output pin.
16	DATA2	P	O (I/O)	DATA output pin.
17	DATA1	P	O (I/O)	DATA output pin.
18	DATA0	P	O (I/O)	DATA output pin (LSB).
19	VAR	P	O (I/O)	DVALID / FIELD / NSIG / LINE signal output pin. DVALID/FIELD/NSIG/LINE signal output can be selected by register setting.
20	VD_F	P	O (I/O)	VD / FIELD signal output pin. VD/ FIELD signal output can be selected by register setting.
21	HD	P	O (I/O)	HD signal output pin.
22	VARSUB	P	O	DVALID / FIELD / NSIG / LINE signal output pin. DVALID/FIELD/NSIG/LINE signal output can be selected by register setting.
23	NC	-	-	Open
24	NC	-	-	Open

[Power Supply]: A-AVDD, D-DVDD, P-PVDD
[I/O]: I–Input pin, O–Output pin, I/O–In Out pin, P–Power Supply pin, G–Ground pin
See section [3.2.](Output pin state) for relationship between PDN-pin and each register.

Pin No.	Symbol	P/S	I/O	Functional Description
25	NC	-	-	Open
26	DVSS	D	G	Digital ground pin.
27	DVDD	D	P	Digital power supply pin.
28	DVDD	D	P	Digital power supply pin.
29	XTO	D	O	Crystal connection pin. Use 24.576 MHz crystal. When PDN=L, output level is DVSS. If crystal is not used, connect to NC or DVSS.
30	XTI	D	I	Crystal connection pin. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.
31	DVSS	D	G	Digital ground pin.
32	DVSS	D	G	Digital ground pin.
33	AIN2	A	I	Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
34	VCOM	A	O	Common internal voltage for AD converter. Connect to AVSS via ≥0.1μF (+/−5% accuracy) ceramic capacitor.
35	IREF	A	O	Analog circuit reference current setting pin. Connect to AVSS via 6.8KΩ (+/−1% accuracy) resistor.
36	NC	-	-	Open
37	NC	-	-	Open
38	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via ≥0.1 μF (+/−1% accuracy) ceramic capacitor.
39	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via ≥0.1 μF (+/−1% accuracy) ceramic capacitor.
40	AIN1	A	I	Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
41	AVDD	A	P	Analog power supply pin.
42	AVDD	A	P	Analog power supply pin.
43	AVSS	A	G	Analog ground pin.
44	AVSS	A	G	Analog ground pin.
45	PDN	P	I	Power-down control pin. Hi-z input is prohibited. Low: Power-down. High: Normal operation.
46	SELA	P	I	I^2C bus address selector pin.
47	TEST	P	I	Pin for test mode setting. Connect to DVSS.
48	NC	-	-	Open

[Power Supply]: A-AVDD, D-DVDD, P-PVDD

[I/O]: I–Input pin, O–Output pin, I/O–In Out pin, P–Power Supply pin, G–Ground pin

See section [3.2.](Output pin state) for relationship between PDN-pin and each register.

[3.2.] Output pin state

PDN -pin	Register setting					Digital output pins state					
	OEN -bit	DL -bit	VD_FL -bit	VAR -bit	HL -bit	DATA[7:0]	VD_F	VAR	VARSUB	HD	DTCLK
L	X	X	X	X	X	Low					
H	H	X	X	X	X	Hi-z					
H	L	L	L	L	L	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT
H	L	H	H	H	H	Low	Low	Low	Low	Low	DOUT

[4.] Electrical characteristics

[4.1.] Absolute maximum ratings

Parameter		Min.	Max.	Unit	Notes
Supply voltage	AVDD, DVDD	-0.3	2.2	V	
	PVDD	-0.3	4.2		
Analog input pin voltage		-0.3	AVDD+0.3(≦2.2)	V	
Digital input pin voltage D		-0.3	DVDD+0.3(≦2.2)	V	XTI,XTO pin
Digital output pin voltage P		-0.3	PVDD+0.3(≦4.2)	V	(*1)
Input pin current (Iin)		-10	10	mA	Power supply pin is not included.
Storage temperature		-40	125	°C	

(*1) Collective term for DTCLK, DATA[7:0], HD, VD_F, VAR, VARSUB, SELA, PDN, SDA, SCL, TEST pins.

- The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
- All power supply grounds (AVSS, DVSS) should be at the same electric potential.
- If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above from the digital output pin.
- The setting other than above may cause the eternal destruction to the device.
- Normal operational is not guaranteed for the above setting.

[4.2.] Recommended operating conditions

Parameter	Min.	Typ.	Max.	Unit	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD=DVDD
I/F supply voltage (PVDD)	1.70	1.80	3.60	V	PVDD≧DVDD
Operating temperature (Ta)	-40		105	°C	

- The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
- All power supply grounds (AVSS, DVSS) should be at the same electric potential.

[4.3.] DC characteristics

(Ta: -40°C~105°C / DVDD=AVDD=1.7V~2.0V / PVDD=DVDD~3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Digital input high voltage(*1)	VIH	0.7PVDD			V	
Digital input low voltage(*1)	VIL			0.3PVDD	V	
Digital input leak current(*1)	IL			±10	uA	
Digital output high voltage(*2)	VOH	0.8PVDD			V	IOH = -600uA
Digital output low voltage(*2)	VOL			0.2PVDD	V	IOL = 1mA
Digital output Hi-z leak current(*2)	HIL			±10	uA	
I^2C (SDA)L output	VOLC			0.4 0.2PVDD	V	IOLC = 3mA PVDD≧2.0V PVDD＜2.0V
XTI input high voltage	VXIH	0.8DVDD			V	
XTI input low voltage	VXIL			0.2DVDD	V	

(*1) Collective term for SELA, PDN, SDA, SCL, TEST pins.

(*2) Collective term for DTCLK, DATA[7:0], HD, VD_F, VAR and VARSUB pins.

[4.4.] Analog characteristics

(AVDD=1.8V, Ta=25˚C)

[4.4.1.] Input range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input range	VIMX	0	0.50	0.60	Vpp	

[4.4.2.] ADC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	RES		10		bit	
Operating clock frequency	FS		27		MHz	
Integral nonlinearity	INL		±1.0	±2.0	LSB	
Differential nonlinearity	DNL		±0.5	±1.0	LSB	
S/N	SN		53		dB	Fin=1MHz*, FS=27MHz, Input range=0.6Vpp
S/(N+D)	SND		51		dB	Fin=1MHz*, FS=27MHz, Input range=0.6Vpp
ADC internal common voltage	VCOM		0.96		V	
ADC internal positive VREF	VRP		1.36		V	
ADC internal negative VREF	VRN		0.56		V	

[4.4.3.] Current consumption

(AVDD = DVDD = PVDD = 1.8V, Ta = -40 ~ 105˚C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
（Active mode）						
Total	IDD		45	62	mA	S(Y/C) video signal input
Analog block	AIDD		27		mA	S(Y/C) video signal input
			19		mA	Composite video signal input*
			10		mA	No-signal input*
Digital block	DIDD		13		mA	S(Y/C) video signal input With crystal (Xtal) connected. Load condition: CL=15pF
I/F block	PIDD		5		mA	
（Power down mode）						
Total	SIDD		≦1	200	uA	
Analog block	ASIDD		≦1		uA	
Digital block	DSIDD		≦1		uA	
I/F block	PSIDD		≦1		uA	

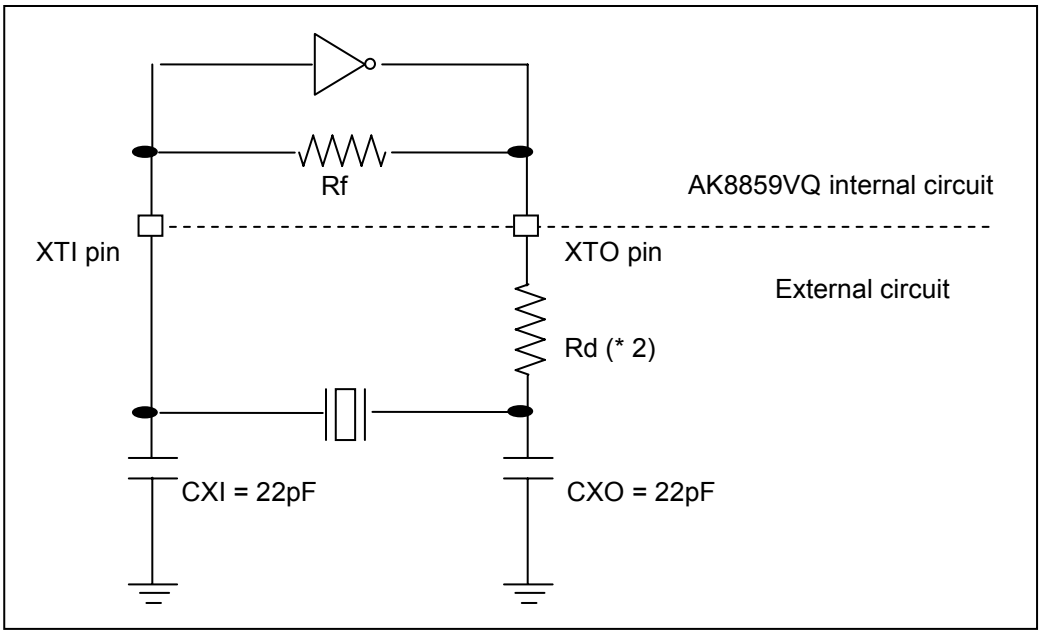
*Reference value.

[4.4.4.] Crystal circuit block

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Frequency	f0		24.576		MHz	
Frequency tolerance	Δf / f			±100	ppm	
Load capacitance	CL		15		pF	
Effective equivalent resistance	Re			100	Ω	(*1)
Crystal parallel capacitance	CO		0.9		pF	
XTI terminal external connection load capacitance	CXI		22		pF	If CL=15pF
XTO terminal external connection load capacitance	CXO		22		pF	If CL=15pF

(*1) Effective equivalent resistance generally may be taken as Re = R1 x $(1+CO/CL)^2$, where R1 is the crystal series equivalent resistance.

Example connection

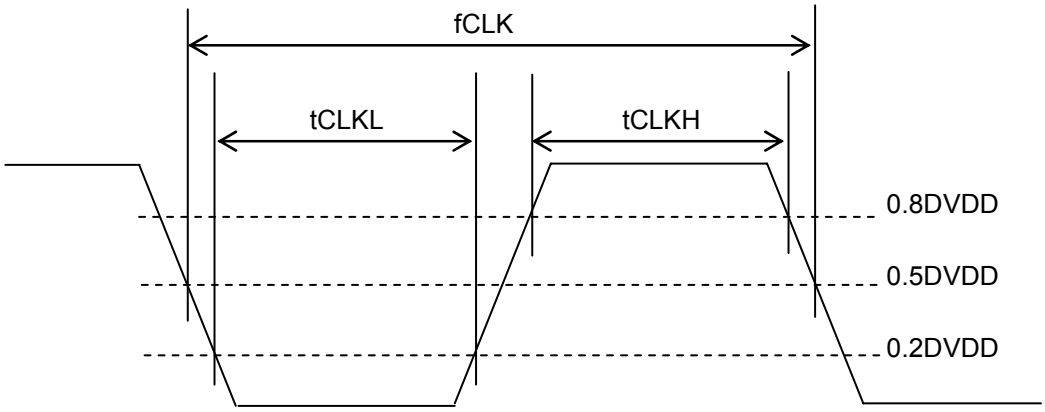


(*2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

[5.] AC Timing

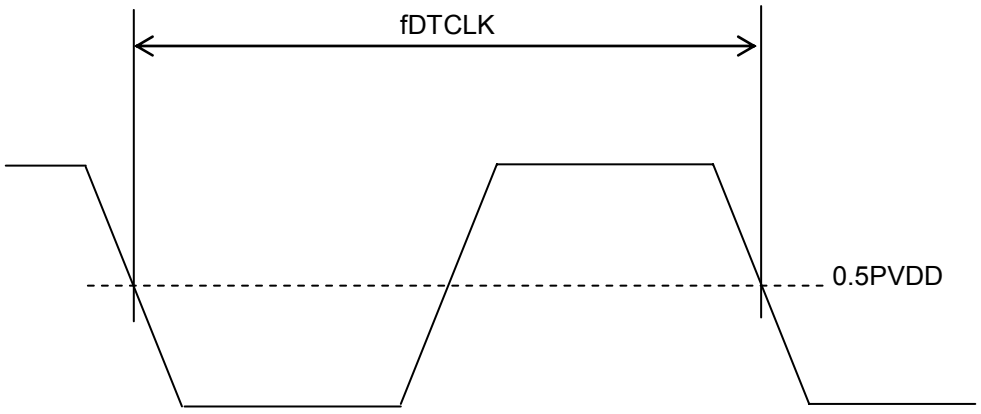
(1.70≦DVDD≦2.00, DVDD≦PVDD≦3.60, Load condition: CL=15pF)

[5.1.] External clock input



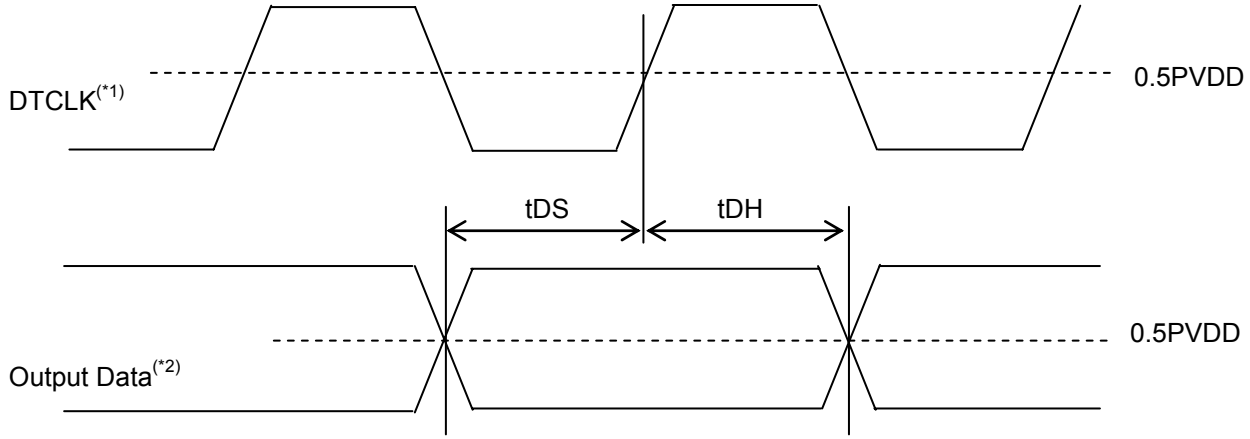
Parameter	Symbol	Min.	Typ.	Max.	Unit
Input CLK	fCLK		24.576		MHz
CLK pulse width H	tCLKH	16			nsec
CLK pulse width L	tCLKL	16			nsec
Frequency tolerance				±100	ppm

[5.2.] Clock output (DTCLK)



Parameter	Symbol	Min.	Typ.	Max.	Unit
DTCLK	fDTCLK		27		MHz

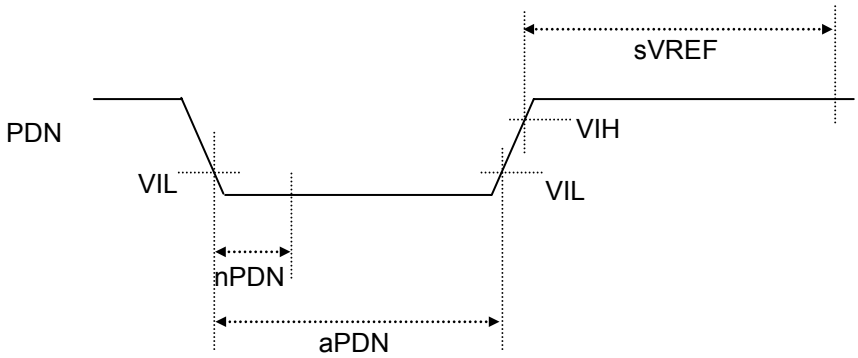
[5.3.] Output data timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
Output Data Setup Time	tDS	10			nsec
Output Data Hold Time	tDH	10			nsec

(*1) It is possible to invert the polarity of DTCLK via register setting.
(*2) Output Data is general term of DATA[7:0], HD, VD_F, VAR and VARSUB.

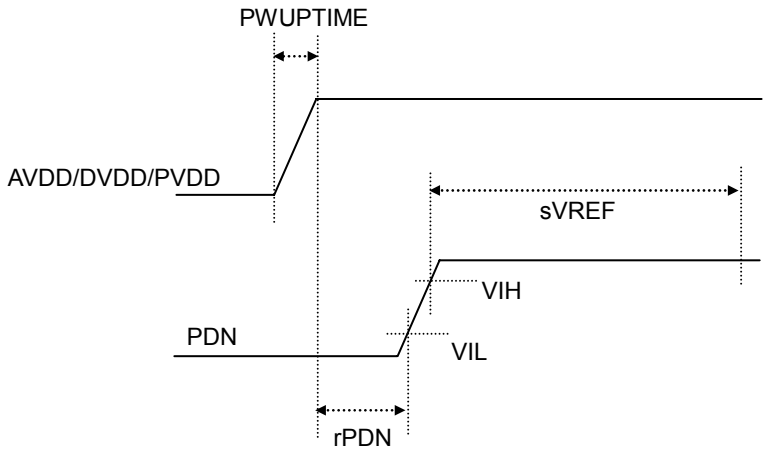
[5.4.] Power down sequence



Parameter	Symbol	Min.	Typ.	Max.	Unit
Power down pulse removal period	nPDN			50	nsec
Power down pulse width	aPDN	500			nsec
VREF stabilization period	sVREF	10			msec

At power down, DTCLK pin, DATA[7:0] pin, HD pin, VD_F pin, VAR pin and VARSUB pin is Low output. After power down released, DATA[7:0] pin, HD pin, VD_F pin, VAR pin and VARSUB pin is stay Low output if no register setting apply. Register setting only apply after VREF stabilization period.

[5.5.] Power-on sequence

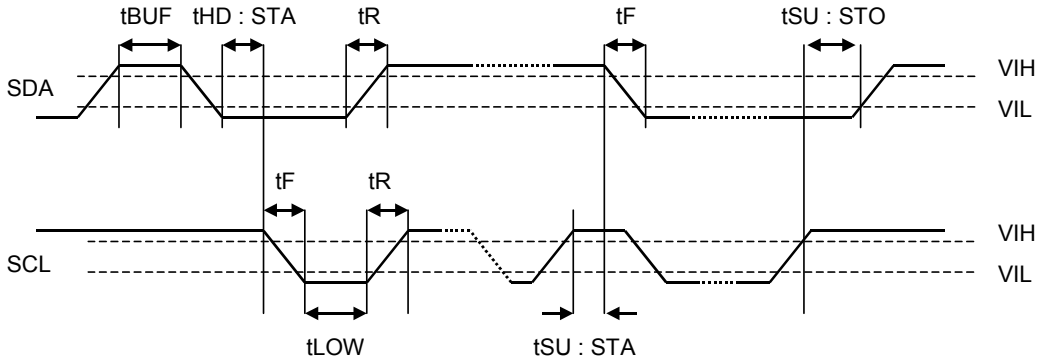


Parameter	Symbol	Min.	Typ.	Max.	Unit
POWERUP TIME	PWUPTIME			100	msec
Power down release	rPDN	500			nsec
VREF stabilization period	sVREF	10			msec

At power-on, PDN must be set to ground level (PDN=Low).
AVDD/DVDD/PVDD should be raised at power-on less than 100msec.
After power down released, DATA[7:0] pin, HD pin, VD_F pin, VAR pin and VARSUB pin is stay Low output if no register setting apply. Register setting only apply after VREF stabilization period.

[5.6.] I²C bus input timing

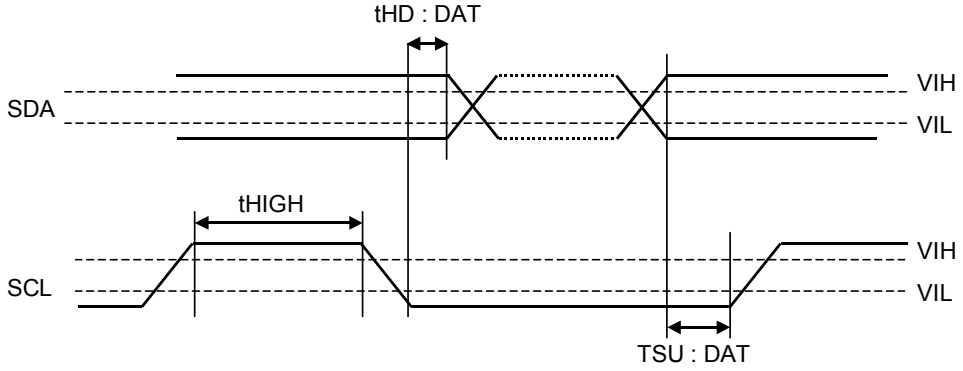
[5.6.1.] Timing 1



Parameter	Symbol	Min.	Typ.	Unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

Note : The timing relating to the I²C bus is as stipulated by the I²C bus specification, and not determined by the device itself. For details, see I²C bus specification.

[5.6.2.] Timing 2



Parameter	Symbol	Min.	Max.	Unit
Data Setup Time	tSU:DAT	100(*1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9(*2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(*1) If I²C is used in standard mode, tSU: DAT ≥250ns is required.

(*2) This condition must be met if the AK8859VQ is used with a bus that does not extend tLOW (to use tLOW at minimum specification).

[6.] Functional overview

○ It accepts composite video signal (CVBS) and S-Video with 2 input pins available for this purpose. The decode signal is selected via register setting.

○ It can decode the following input video signal via register setting:
- NTSC-M, J / NTSC-4.43 / PAL-B,D,G,H,I,N / PAL-Nc / PAL-M / PAL-60 / SECAM
- In addition, it has auto detection mode via register setting which automatically recognizes the input signal category.

○ It output interface is ITU-R BT.656 compliant.
(It may not be possible, however to meet these requirement if the input signal quality is poor.)

○ For connection of devices having no ITU-R BT.656 interface, it shows the active video region by DVALID signal output.

○ Its analog circuit of the AK8859VQ clamps the input signal to the sync tip. Its digital circuit clamps the digitized input data to the pedestal level.

○ Its VBI data slicing function enables output of the slicing results as ITU-R BT.601 format digital data.

○ It has digital PGA built internally and can be adjusted in the range of −4.06dB～6.90dB by register setting.

○ Its adaptive AGC function enables measurement of the input signal size and determination of the input signal level.

○ It performs adaptive two-dimensional Y/C separation, in which its phase detector selects the best correlation from among vertical, horizontal, and diagonal samples and optimum Y/C separation mode.

○ Its digital pixel spacing adjustor can align vertical positions by vertical pixel positioning.

○ Its operates in line-locked, frame-locked, or fixed clock mode with automatic transition and optimum mode selection by automatic scanning.

○ Its ACC function enables measurement of the input signal color burst size and determination of the appropriate color burst level.

○ It judges the chroma signal quality from the color burst of the input signal, and can apply color kill if the signal quality is judged insufficient. It can also apply color kill if the color decode PLL clock control.

○ Its image quality adjustment function includes contrast, brightness, hue and color saturation adjustment.

○ It can decode conflated Closed Caption Data, Closed Caption Extended Data, WSS, VBID(CGMS-A) and write them separately to the storage register.

○ Its monitoring register enables monitoring of a number of internal functions.

○ Its enables Macrovision signal type notification, in cases where the Macrovision signal is included in the decoded data.

[7.] Functional Description

[7.1.] Analog interface

The AK8859VQ accepts composite (CVBS) and S-Video (Y/C) signals, with 2 input pins available for this purpose. The decode signal is selected via the register.

Input signal selection Sub Address: 0x00 [1:0]

Name	Definition	Notes
AINSEL0 ~ AINSEL1	[AINSEL1 : AINSEL0] [00]: AIN1 (CVBS) [01]: AIN2 (CVBS) [10]: AIN1(Y) / AIN2(C) (S-Video) [11]: No-signal input (Analog circuit is set to power-down*)	

*Clamp and ADC block is power-downed.

In used with AINSEL[1:0]=[11], Ouput data is depend on NSIGMD[1:0]–bit. However, in used with NSIGMD[1:0]=[10], DATA[7:0]-pin, HD-pin, VD_F-pin, VAR-pin and VARSUB-pin output Low.

[7.2.] Clock mode

The AK8859VQ input clock can be selected between internal built crystal and external clock input via register setting. The input clock frequency is 24.576MHz.

Clock mode setting Sub Address: 0x00 [7]

Name	Definition	Notes
CLKMD	[0]: For crystal [1]: External clock input (clock generator)	

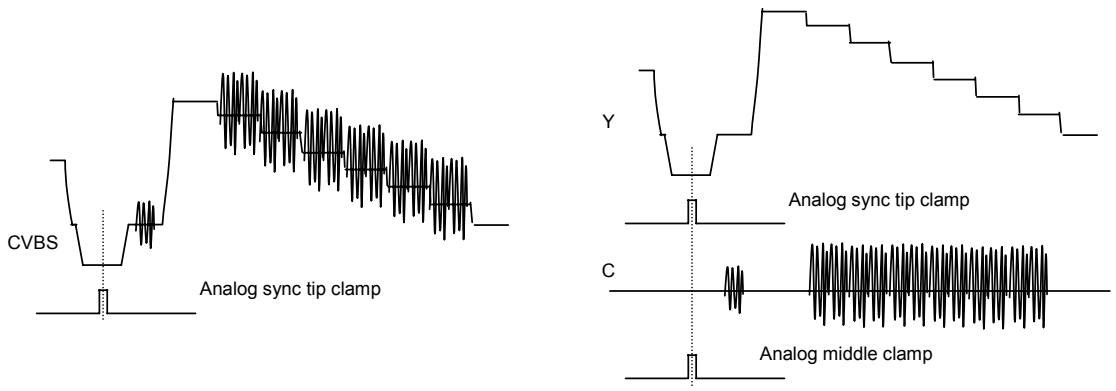
[7.3.] Analog clamp circuit

The analog circuit of AK8859VQ clamps the input signal to the reference level. The way to clamp the input signal is show as follows.

○ When decode composite (CVBS) video signal
Clamp timing is performs by sync tip clamp (analog sync tip clamp).
The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.

○ When decode S-Video (Y/C) signal
(Y signal): Clamp timing is performs by sync tip clamp (analog sync tip clamp).
The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.
(C signal): Clamp timing is performs by middle clamp (analog middle clamp).
The clamp timing pulse is generated exactly at the same timing of Y signal clamp pulse.

Clamp timing pulse



Furthermore, the AK8859VQ can change the position, width, and current value of clamp pulse via register.

Set the current value of clamp in analog block Sub Address: 0x01 [1:0]

Name	Definition	Notes
CLPG0 ~ CLPG1	[00]: Min. [01]: Middle 1 {=(Min. x 3)} [10]: Middle 2 {=(Min. x 5)} [11]: Max. {=(Min. x 7)}	Default setting is [00]

Set the clamp pulse width Sub Address: 0x01 [4]

Name	Definition	Notes
CLPWIDTH	[0]: 275nsec [1]: 555nsec	Default setting is [0]

[7.4.] Input video signal categorization

The AK8859VQ video input signal categorization can be selected via register. The AK8859VQ can decode the following video signal:

NTSC-M, J
NTSC-4.43
PAL-B, D, G, H, I, N
PAL-Nc
PAL-M
PAL-60
SECAM

Input video signal categorization register setting is show as follows.

Subcarrier frequency setting Sub Address: 0x02 [1:0]

Name	Definition	Notes
VSCF0 ~ VSCF1	[VSCF1 : VSCF0] (MHz) [00]: 3.57954545 (NTSC-M,J) [01]: 3.57561149 (PAL-M) [10]: 3.58205625 (PAL-Nc) [11]: 4.43361875(PAL-B,D,G,H,I,N,60, NTSC-4.43, SECAM)	

Color encode format setting Sub Address: 0x02 [3:2]

Name	Definition	Notes
VCEN0 ~ VCEN1	[VCEN1 : VCEN0] [00]: NTSC [01]: PAL [10]: SECAM [11]: Reserved	

Line frequency setting Sub Address: 0x02 [4]

Name	Definition	Notes
VLF	[0]: 525-Line (NTSC-M,J, NTSC-4.43, PAL-M,60) [1]: 625-Line (PAL-B,D,G,H,I,N, PAL-Nc, SECAM)	

Monochrome mode setting Sub Address: 0x02 [5]

Name	Definition	Notes
BW	[0]: Not monochrome (monochrome mode OFF) [1]: Decode as monochrome signal (monochrome mode ON)	

When composite video signal decode is selected, in the monochrome mode (BW=1), the input signal is treated as a monochrome signal, and all sampling data digitized the AD converter passes through the luminance process and is processed as luminance signal, and the CbCr code is output as 0x80 (601 level data) regardless of the input. When S-video (Y/C) signal decode is selected, only luminance signal is decode as an output.

Setup processing setting Sub Address: 0x02 [6]

Name	Definition	Notes
SETUP	[0]: Setup absent setting [1]: Setup present setting	

With the Setup present setting, the luminance and color signals are processed as follows:
Yout = (Yin-7.5)/0.925
Uout = Uin/0.925, Vout = Vin/0.925

[7.5.] Auto detection mode of input signal

The video input signal of the AK8859VQ can be automatically detected (auto detection mode) via register.

Settings for auto detection mode of input signal Sub Address: 0x02 [7]

Name	Definition	Notes
AUTODET	[0]: OFF (manual setting) [1]: ON	

In auto detection mode, the AK8859VQ can detect the following parameters.

Number of lines per frame:
525 (Line)
625 (Line)

Subcarrier frequency:
3.57954545 (MHz)
3.57561149 (MHz)
3.58205625 (MHz)
4.43361875 (MHz)

Color encoding formats:
NTSC
PAL
SECAM

Monochrome signal*:
Not monochrome
Monochrome

(*Note: Automatic monochrome detection is active if the color kill setting is ON.)

The detected result of auto detection mode is reflected to Input Video Status Register.
This enables the host to distinguish among the formats NTSC-M,J / NTSC-4.43 / PAL-B,D,G,H,I,N / PAL-M / PAL-Nc / PAL-60 / SECAM and monochrome.
It should be noted that it does not detect NTSC-M, NTSC-J or PAL-B,D,G,H,I,N formats.

Sub Address: 0x18 “Input Video Status Register”

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIXED	UNDEF	ST_B/W	ST_VLF	ST_VCEN1	ST_VCEN0	ST_VSCF1	ST_VSCF0

[7.6.] Limiting auto detection candidates of input signal

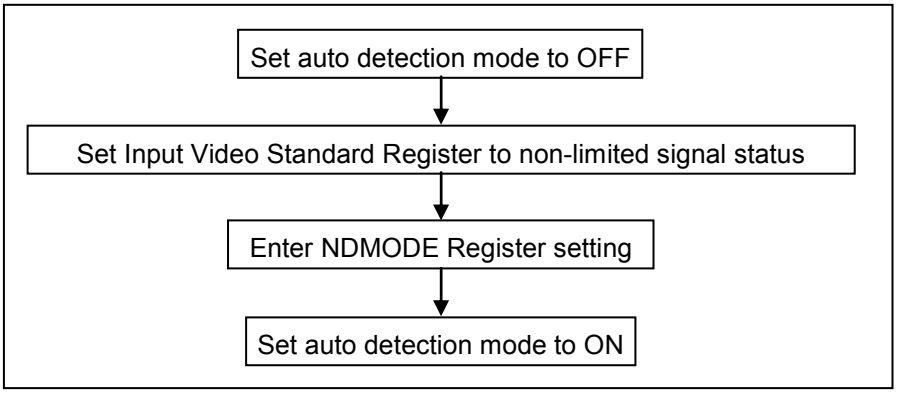
In auto detection mode, the candidates for detection can be limited via register.

Sub Address: 0x03 “NDMODE Register”

Name	Definition	Notes
NDPALM	[0]: PAL-M candidate [1]: PAL-M non-candidate	
NDPALNC	[0]: PAL-Nc candidate [1]: PAL-Nc non-candidate	
NDSECAM	[0]: SECAM candidate [1]: SECAM non-candidate	
Reserved	Reserved	
NDNTSC443	[0]: NTSC-4.43 candidate [1]: NTSC-4.43 non-candidate	
NDPAL60	[0]: PAL-60 candidate [1]: PAL-60 non-candidate	
ND525L	[0]: 525Line candidate [1]: 525Line non-candidate	
ND625L	[0]: 625Line candidate [1]: 625Line non-candidate	

In making the above register settings, the following restrictions apply.

1. Setting both NDNTSC443-bit and NDPAL60-bit to 1 is prohibited.
2. Setting both ND525L-bit and ND625L-bit to 1 is prohibited.
3. To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.



[7.7.] VBI blanking interval data output

In the AK8859VQ, the settings for the output code and vertical blanking intervals for the output signal are as follows.

Setting vertical blanking intervals (VBLANK) Sub Address: 0x04 [2:0]

Name	Setting value	525/625	Vertical blanking interval	Notes
VBIL0 ~ VBIL2	[001]	525	Line1~Line20 及び Line263.5~Line283.5	+1Line
		625	Line623.5~Line24.5 及び Line311~Line336	
	[010]	525	Line1~Line21 及び Line263.5~Line284.5	+2Lines
		625	Line623.5~Line25.5 及び Line311~Line337	
	[011]	525	Line1~Line22 及び Line263.5~Line285.5	+3Lines
		625	Line623.5~Line26.5 及び Line311~Line338	
	[000]	525	Line1~Line19 及び Line263.5~Line282.5	default
		625	Line623.5~Line23.5 及び Line311~Line335	
	[101]	525	Line1~Line16 及び Line263.5~Line279.5	-3Lines
		625	Line623.5~Line20.5 及び Line311~Line332	
	[110]	525	Line1~Line17 及び Line263.5~Line280.5	-2Lines
		625	Line623.5~Line21.5 及び Line311~Line333	
	[111]	525	Line1~Line18 及び Line263.5~Line281.5	-1Line
		625	Line623.5~Line22.5 及び Line311~Line334	
	[100]	Reserved	Reserved	

As indicated in this table, the default values are:

(525i) Line1~Line19 and Line263.5~Line282.5

(625i) Line623.5~Line23.5 and Line311~Line335

The other specific values are set by entering the difference from these default values.

[7.8.] Output data code Min/Max

The AK8859VQ data code output format (Y:Cb:Cr=4:2:2) is compliant with ITU-R BT.601.
All internal calculating operations are made with Min = 1, Max = 254.
With LIMIT601-bit set to [1], codes 1~15 and 236~254 are respectively clipped to 16, 235.

Setting for output data code Min/Max Sub Address: 0x04 [3]

Name	Setting value	Output data code Min.~Max.	Notes
LIMIT601	[0]	Y: 1~254 Cb, Cr: 1~254	Default
	[1]	Y: 16~235 Cb, Cr: 16~240	

In case of LIMIT601=[0] and EAVSAVN-bit=[1]*, the output code Min/Max is 0～255.

*Sub Address: 0x08 [2]

[7.9.] V-bit

In the AK8859VQ, the settings for V-bit handling in ITU-R BT.656 format are as follows.

Setting for V-bit handling in ITU-R BT.656 format Sub Address: 0x04 [4]

Name	Setting value	525-line		625-line	
		V-bit=0	V-bit=1	V-bit=0	V-bit=1
TRSVSEL	[0] BT. 656-3	Line10~Line263 Line273~Line525	Line1~Line9 Line264~Line272	Line23~Line310 Line336~Line623	Line1~Line22 Line311~Line335 Line624~Line625
	[1] BT. 656-4 and SMPTE125M	Line20~Line263 Line283~Line525	Line1~Line19 Line264~Line282		

These values are unaffected by the VBIL[2:0]-bit setting.

[7.10.] Slice function

The results of VBI slicing by the AK8859VQ slicing function are output as ITU-R BT.601 digital data. The VBI interval is set via VBIL[2:0]-bits. VBI slicing is performed in the luminance in the luminance signal processing path, so that the Cb/Cr value of the effective line 601 output code is output at the same level as the corresponding luminance signal.

Setting for slice level Sub Address: 0x04 [5]

Name	Definition
SLLVL	[0]: 25IRE [1]: 50IRE

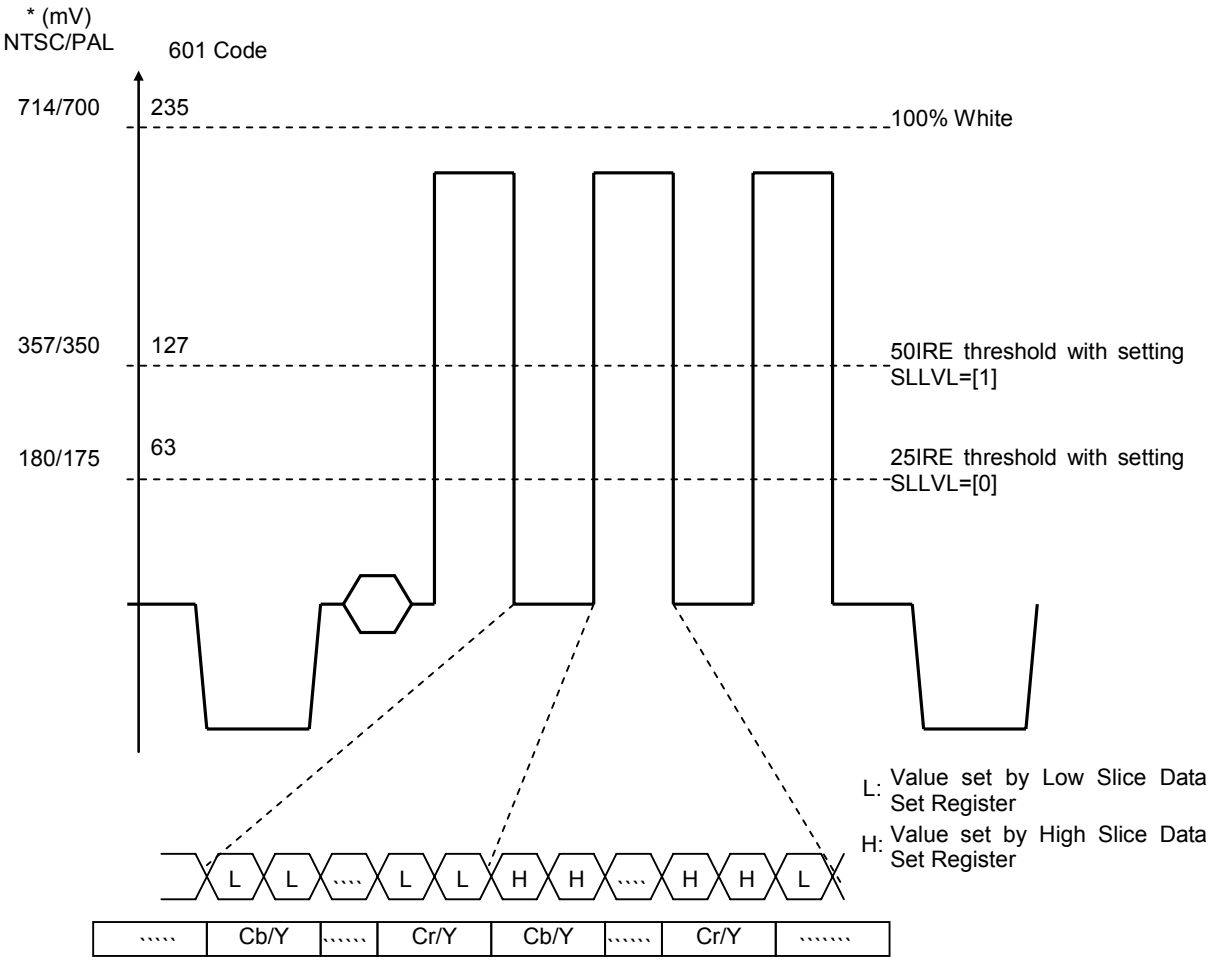
Hi/Low Slice Data Set Register of output data, as follows.

Setting for higher of two values resulting from slicing Sub Address: 0x11

Name	Definition
H0 ~ H7	Default: 0xEB(235) Note that a setting of 0x00 or 0xFF corresponds to a special 601 code.

Setting for lower of two values resulting from slicing Sub Address: 0x12

Name	Definition
L0 ~ L7	Default: 0x10(16) Note that a setting of 0x00 or 0xFF corresponds to a special 601 code.



*Threshold values (mV) are approximate

High/Low conversion is performed for either the Cb/Y or the Cr/Y combination. The above figure is an example of the conversion points for Cb/Y.

[7.11.] VBI period decode data

The AK8859VQ decode data during VBI period can be selected via register.

Settings for decode data in the VBI period Sub Address: 0x04 [7:6]

Name	Setting value	Decode data	Notes
VBIDEC0 ~ VBIDEC1	[00]	Black level output	Y = 0x10 Cb/Cr = 0x80
	[01]	Monochrome mode	Y = data converted to 601 level Cb/Cr = 0x80
	[10]	Sliced data output	Y/Cb/Cr = value corresponding to slice level (Value set at Hi/Low Slice Data Set Register)
	[11]	Reserved	Reserved

Note: (525i) Lne1～Line9 and Line263.5～Line272.5
(625i) Line623.5～Line6.5 and Line311～Line388
During the above period, these values are unaffected by the VBIDEC[1:0]-bits setting.
The output code during this period is black level code (Y=0x10, Cb/Cr=0x80).

[7.12.] Output pin status

The AK8859VQ output from the DATA[7:0]-pin, VD_F-pin, VAR-pin, VARSUB-pin and HD-pin can each be fixed at Low via register.

Setting each digital output pins fixed to Low output Sub Address: 0x05 [3:0]

Name	Definition	Notes
DL	[0]: Normal output [1]: [D7: D0] pin output fixed at Low.	Default: Low output
VD_FL	[0]: Normal output [1]: VD_F pin output fixed at Low.	Default: Low output
VARL	[0]: Normal output [1]: VAR and VARSUB pin output fixed at Low.	Default: Low output
HL	[0]: Normal output [1]: HD pin output fixed at Low.	Default: Low output

In addition, the output from the DTCLK, DATA[7:0], VD_F, VAR, VARSUB and HD pins can be set to Hi-z output via register.

Setting digital output pins* to Hi-z output Sub Address: 0x05 [4]

Name	Definition	Notes
OEN	[0]: Normal output [1]: Hi-Z output	Default: [0] Normal output

*Collective term for DTCLK, DATA[7:0], HD, VD_F, VAR and VARSUB pins.

However, the PDN pin states will have priority regardless of these register setting. When PDN pin is Low output, the output from the DTCLK, DATA[7:0], VD_F, VAR, VARSUB and HD pins is Low output.

The relation between PDN pin and digital output pin status is show as follows:

PDN -pin	Register setting					Digital output pins status					
	OEN -bit	DL -bit	VD_FL -bit	VAR -bit	HL -bit	DATA[7:0]	VD_F	VAR	VARSUB	HD	DTCLK
L	X	X	X	X	X	Low					
H	H	X	X	X	X	Hi-z					
H	L	L	L	L	L	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT
H	L	H	H	H	H	Low	Low	Low	Low	Low	DOUT

*DOUT is normal output.

[7.13.] HD pin output

The Horizontal Sync signal of the AK8859VQ is output from HD pin.

Pin name	525-Line	625-Line
HD	Low for 4.7us at 15.734 kHz interval.	Low for 4.7us at 15.625 kHz interval.

[7.14.] VD_F, VAR and VARSUB pin output selection

The output signal from VD_F, VAR and VARSUB pins is show as follows by register setting.

Pin name	Output signal	Notes	
VD_F	VD	525-Line	625-Line
		Line4~Line6 and Line266.5~Line269.5: Low	Line1~Line3.5 and Line313.5~Line315: Low
	FIELD	ODD-Field: Low, EVEN-Field: High	
VAR VARSUB	DVALID	Active video data period. Active-Low	
	FIELD	ODD-Field: Low, EVEN-Field: High	
	NSIG	Sync status of video input signal Low: Signal present (synchronized) High: Signal absent (not synchronized)	
	LINE	In auto detection mode, it shows the result of line number detected in input video signal. 525LINE: Low, 625LINE: High If the auto detection mode is OFF, the setting of current VLF-bit* is output through this pin. (*Sub-address:0x02-"bit4")	

The output signal of VD_F, VAR and VARSUB pins is show as follows.

Settings for VD/FIELD signals selection Sub Address: 0x05 [5]

Name	Definition	Notes
VD_FSEL	[0]: VD signal output [1]: FIELD signal output	

Settings for VAR and VARSUB pin output signals selection Sub Address: 0x05 [7:6]

Name	Definition		Notes
VARSEL0 ~ VARSEL1	VAR-pin [VARSEL1 : VARSEL0]	VARSUB-pin [VARSEL1 : VARSEL0]	
	[00]: DVALID signal output [01]: FIELD signal output [10]: NSIG signal output [11]: LINE signal output	[00]: NSIG signal output [01]: LINE signal output [10]: FIELD signal output [11]: DVALID signal output	

[7.15.] Output pin polarity

The output signals from each digital output pin can be inverted via register.

Setting for output pin polarity Sub Address: 0x06 [7:5]

Name	Pin name	Output signal	Setting value	
			[0]	[1]
HDP	HD	HD	Active Low	Active High
VD_FP	VD_F	VD	Active Low	Active High
		Field	Low: Odd-Field High: Even-Field	Low: Even-Field High: Odd-Field
VARP	VAR VARSUB	DVALID	Active Low	Active High
		Field	Low: Odd-Field High: Even-Field	Low: Even-Field High: Odd-Field
		NSIG	High: Signal absent	Low: Signal absent
		LINE	Low: 525Line High: 625Line	Low: 625Line High: 525Line

In addition, it is possible to invert the output signal from the DTCLK pin.

Setting for polarity of DTCLK signal output Sub Address: 0x06 [4]

Name	Definition
CLKINV	[0]: Normal output (write in data at rising edge) [1]: Phase of data and clock is invert (write in data at falling edge)

[7.16.] Phase correction

In PAL-B, D, G, H, I, N, Nc, 60, and M decoding, the AK8859VQ performs phase correction for each line. With this function ON, color averaging is performed for each line. In the adaptive phase correction mode, interline phase correlation is sampled and color averaging is performed for correlated samples.
Interline color averaging is also performed in NTSC-M and J decoding.
No phase correction or color averaging is performed in SECAM decoding.

Settings for phase correction Sub Address: 0x07 [1:0]

Name	Definition
DPAL0 ~ DPAL1	[DPAL1 : DPAL0] [00]: Adaptive phase correction mode [01]: Phase correction ON [10]: Phase correction OFF [11]: Reserved

[7.17.] No signal output

If no input signal is found (as shown by control bit NOSIG-bit), the output signal is black-level, blue-level (blueback), or input-state (sandstorm), depending on the register setting. (*Sub-address:0x15-"bit0")

Settings for output signals for no input signal Sub Address: 0x07 [3:2]

Name	Definition
NSIGMD0 ~ NSIGMD1	[NSIGMD1 : NSIGMD0] [00]: Black-level output [01]: Blue-level (blueback) output [10]: Input-state (sandstorm) output [11]: Reserved

In case of S-Video (Y/C) signal input, no signal output is only on Y signal.
It should be noted that there is no signal output detect on C signal.

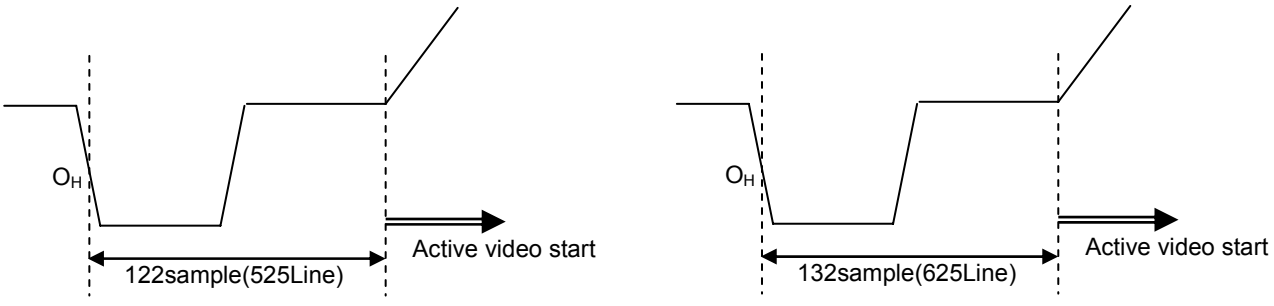
[7.18.] Active video data start position

The start position of active video data of the AK8859VQ can be advance/delay via register. 1 sample advance/delay of data rate is 13.5MHz.

Setting for start position of active video data Sub Address: 0x07 [6:4]

Name	Definition
ACTSTA0 ~ ACTSTA2	[ACTSTA2 : ACTSTA0] [001]: 1Sample delay [010]: 2Sample delay [011]: 3Sample delay [000]: Normal start position [101]: 3Sample advance [110]: 2Sample advance [111]: 1Sample advance [100]: Reserved

The default position of start position is shown below (ITU-R BT.601 standard interface).



[7.19.] VLOCK mechanism

The AK8859VQ synchronizes internal operation with the input signal frame structure. If, for example, the frame structure of the input signal comprises 524 lines, the internal operation will have structure of 524 lines per frame. This mechanism is termed the VLOCK mechanism. If an input signal changes from a structure of 525 lines per frame to one of 524 lines per frame, internal operation will change accordingly, and the VLOCK mechanism will go to UnLock via a pull-in process. In such case, the UnLock status can be confirmed via the control register [VLOCK-bit*]. Note that the time required for locking of the VLOCK mechanism upon channel or other input signal switching will be about 4 frames (*Sub-address:0x15-"bit1")

Furthermore, the AK8859VQ synchronizes internal operation with the vertical SYNC of the input signal. This mechanism is termed the direct LOCK mechanism.

Setting for Vertical SYNC mechanism Sub Address: 0x07 [7]

Name	Definition
VERTS	Vertical SYNC mechanism [0]: VLOCK mechanism [1]: Direct LOCK mechanism

[7.20.] Y/C separation

The adaptive two-dimensional Y/C separation of the AK8859VQ utilizes a co-relation detector to select the best-correlated direction from among vertical, horizontal, and diagonal samples, and selects the optimum Y/C separation mode.

For NTSC-4.43, PAL-60, and SECAM inputs, the Y/C separation is one-dimensional only, regardless of the setting.

Setting for Y/C separation Sub Address: 0x08 [1:0]

Name	Setting Value	YC separation mode	Notes
YCSEP0 ~ YCSEP1	[00]	Adaptive	
	[01]	1-D	1-D (BPF)
	[10]	2-D	(NTSC-M,J, PAL-M): 3 Line 2-D (PAL-B,D,G,H,I,N,Nc): 5 Line 2-D
	[11]	Reserved	

[7.21.] EAV/SAV code

The EAV/SAV code of ITU-R BT.656 standard interface can be output with the output data DATA[7:0] by the register setting.

Setting for EAV/SAV code output Sub Address: 0x08 [2]

Name	Definition
EAVSAVN	[0]: EAV/SAV code is fed to the output data. [1]: EAV/SAV code is not output.

In case of LIMIT601=[0]*, if EAVSAVN is setting to [1], the output code range is limit to 0～255.

*Sub Address: 0x04 [3]

[7.22.] Output Interface

[7.22.1.] 656 interface

[7.22.1.1.] Line-locked and frame-locked clock modes

The AK8859VQ data output in both of these modes are compliant with ITU-R BT.656, which is requires the following samples and line numbers.

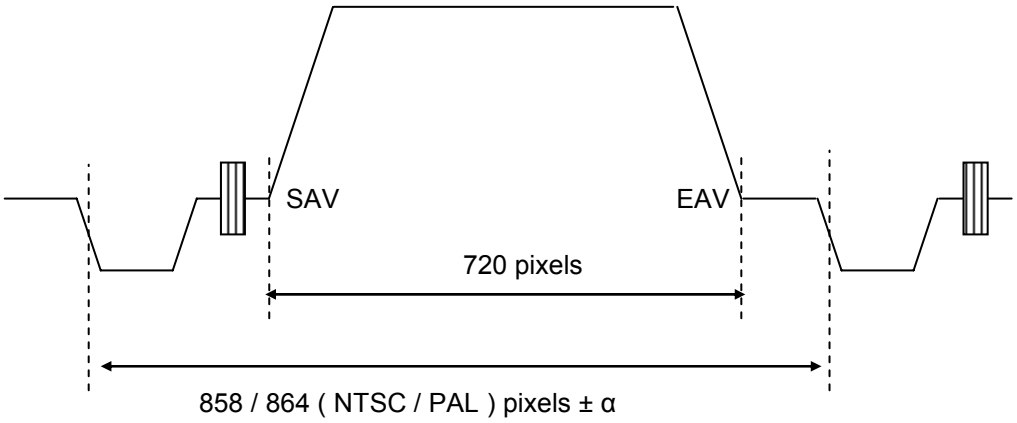
- Number of samples for 1 line:
  858 samples (525i) / 864 samples (625i)
- Number of lines for 1 frame: 525 lines / 625 lines

It may not be possible, however to meet these requirement if the input signal quality is poor.
In the event of output-stage buffer failure, line drop/repeat processing will be performed.

A line drop or a line repeat will result in output signal with 524/624 or 526/626 lines per frame respectively. Line drop/repeat processing may be performed at any line in the frame.

[7.22.1.2.] Fixed-clock mode

In fixed-clock mode, operation is at an internally generated 27 MHz clock, from a 24.576 MHz input clock. The output signal is therefore not synchronized with the input signal, and thus not ITU-R BT.656 compliant. Data is output in SAV format. As shown in the following figure, EAV is guaranteed for 720 pixels from SAV, but the number of pixels from EAV to SAV is not.



When the fixed-clock mode is performed, the active area of the output data is determined by SAV standard.

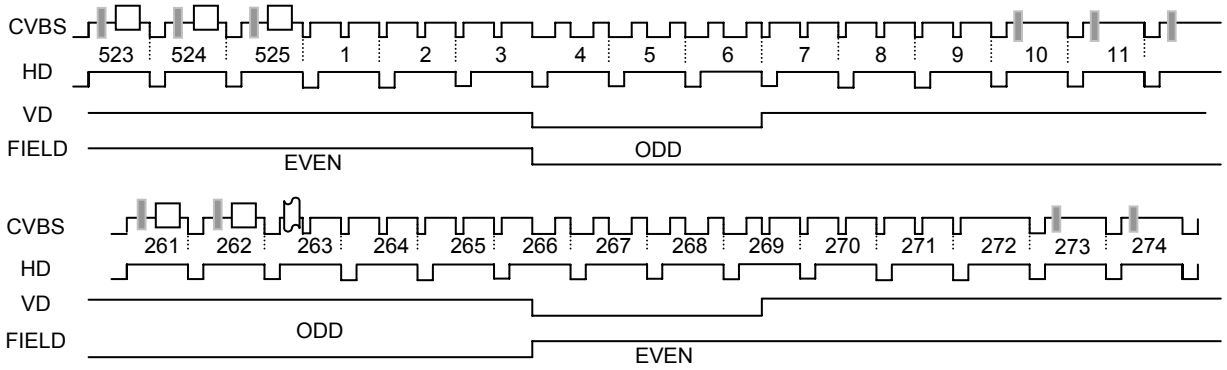
[7.22.2] Output timing signal diagram

[7.22.2.1.] Line-locked and frame-locked clock modes

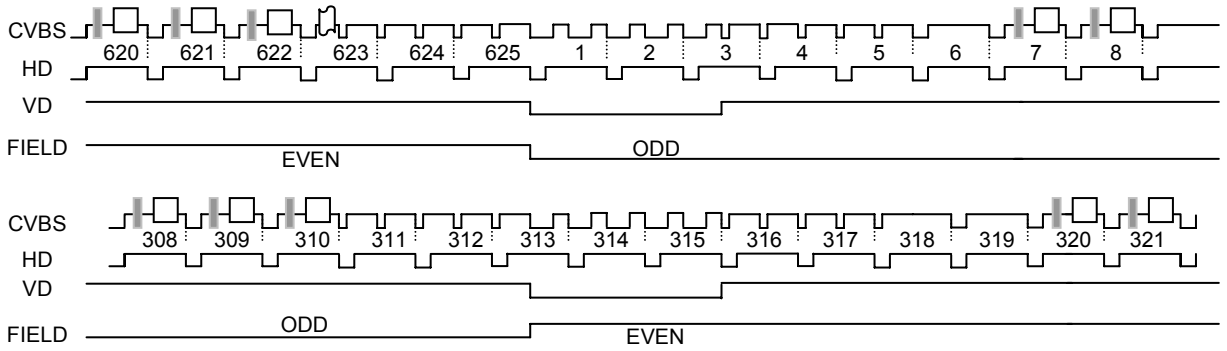
When the AK8859VQ is connected to the system with no ITU-R BT.656 interface, HD, VD, DVALID and FIELD signals is output.

The relations between HD, VD and FIELD signals are shown as follow.

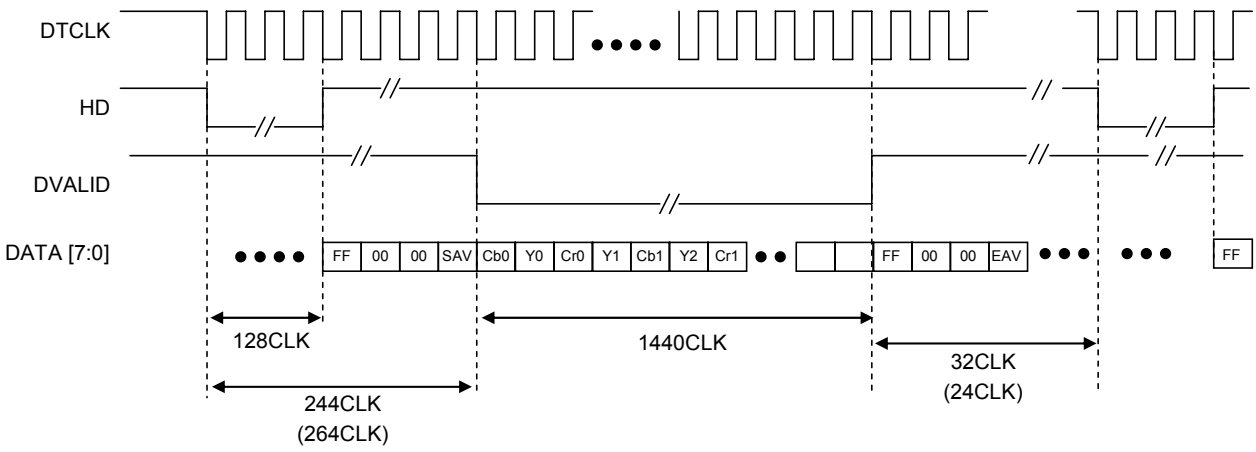
525-Line input (For example, composite video signal input timing is shown below)



625-Line input (For example, composite video signal input timing is shown below)



The relations between HD signal, DVALID signal and EAV/SAV code are shown in the following timing diagram.

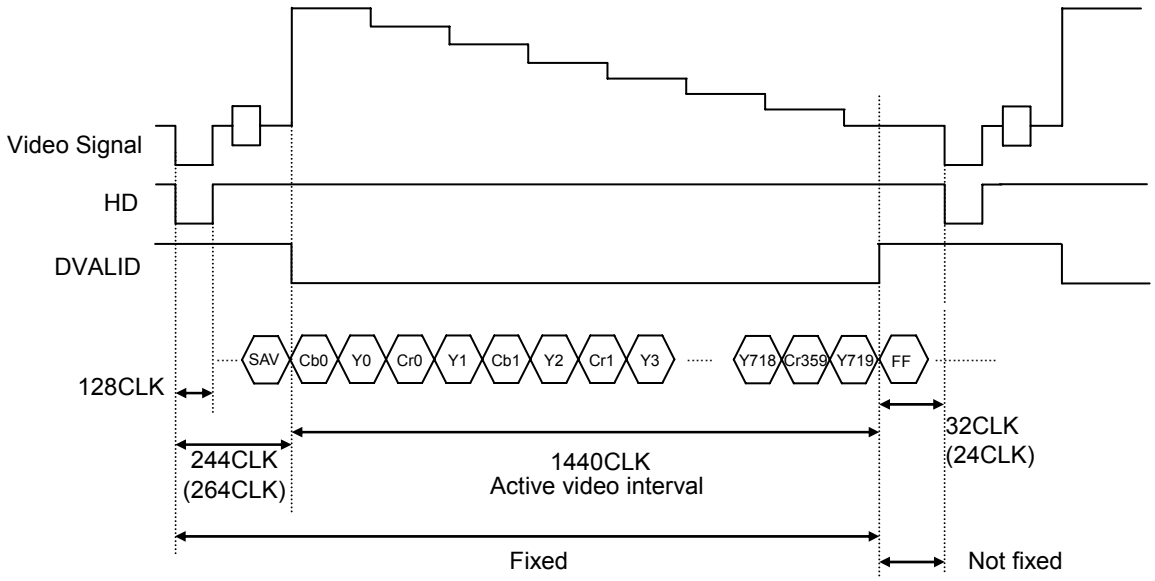


*The numbers shown in the ( ) is refer to clock number of 625-Line.

[7.22.2.2.] Fixed-clock mode

In fixed-clock mode, the internal clock is not synchronized with the output signal, but a space of 122/132 (NTSC/PAL) pixels is guaranteed between the horizontal sync signal and the start of the active video interval.

(For example, composite video signal input timing is shown below and 1pixel = 2CLK)



[7.23] Digital Pixel interpolator

The digital pixel interpolator of the AK8859VQ aligns vertical pixel positions in both frame-lock and fixed-clock operating modes. The pixel interpolator can be set to ON or OFF via register. With a register setting of AUTO, the pixel interpolator is OFF or ON depending on the clock mode, as follows.

Line-locked clock mode	OFF
Frame-locked clock mode	ON
Fixed-clock mode	ON

Settings for pixel interpolator operation Sub Address: 0x08 [5:4]

Name	Setting Value	Interpolator operation	Notes
INTPOL0 ~ INTPOL1	[00]	Auto	Dependent on clock mode.
	[01]	ON	
	[10]	OFF	
	[11]	Reserved	

[7.24] Clock generation

The AK8859VQ operates in the following three clock modes:

[7.24.1.] Line-locked clock mode

The “line-locked clock” is generated by PLL using horizontal sync signal within the input signal. If no input signal is present, the AK8859VQ will switch from this mode to fixed-clock mode.

[7.24.2.] Frame-locked clock mode

The “frame-locked clock” is generated by PLL using vertical sync signal within the input signal. If no signal is present, the AK8859VQ will switch from this mode to fixed-clock mode.

[7.24.3.] Fixed-clock mode

No PLL control is applied in this mode, which is enabled only when either it is set via the register or no input signal is present. The sampling clock in this mode is 27MHz or 54MHz. In this mode, data capture cannot be performed in EAV (end of active video), and must be performed in SAV (start of active video) format. The number of pixels per line is not guarantee in this mode, but data guarantee is performed in the interval from SAV to EAV.

[7.24.4.] Auto transition mode

The AK8859VQ transition function automatically switches among the above modes and selects the optimum one, and when no input signal is present, it switches to the fixed-clock mode.

Setting for selection of clock generation mode Sub Address: 0x08 [7:6]

Name	Setting value	Clock generation mode	Notes
CLKMODE0 ~ CLKMODE1	[00]	Automatic	
	[01]	Line-locked	
	[10]	Frame-locked	
	[11]	Fixed-clock	

[7.25.] PGA (Programmable Gain Amp)

The AK8859VQ digital PGA is built internally.
The digital PGA value can be set in range −4.06dB～6.90dB.
Default gain setting is $0x3C_{(HEX)}$=0.00dB.

PGA gain equation:

$$\text{Gain(dB)} = 20LOG\left(\frac{(2.5\times PGA)+251.5}{401.5}\right)$$

**PGA*:PGA1orPGA2 register value$_{(Dec.)}$*

At the default setting, when the composite video signal input with 0.5Vpp is input to the AIN pin, the decode gain setting is set to appropriate range.

PGA1 is used for CVBS and Y signals gain processing. PGA2 is used for C signal gain processing.

Setting for PGA1 value Sub Address: 0x0A [7:0]

Name	Definition
PGA1_0 ~ PGA1_7	PGA1 gain setting. PGA gain is set by above equation.

Setting for PGA2 value Sub Address: 0x0B [7:0]

Name	Definition
PGA2_0 ~ PGA2_7	PGA2 gain setting. PGA gain is set by above equation.

This register also can be used to read the current setting of the AGC setting.
If AGC is enable, PGA1[7:0]-bit and PGA2[7:0]-bit setting value has no effect.
If AGC is disable, PGA1[7:0]-bit and PGA2[7:0]-bit setting is effective and the gain setting can be manually entered.

[7.26.] AGC (Auto Gain Control)

The AGC of the AK8859VQ measures the size of the input signal (i.e. the difference between the sync tip and pedestal levels), and adjusts the PGA value to bring the sync signal level to 286mV/300mV.
The AGC function in the AK8859VQ is adaptive, and thus includes peak AGC as well as sync AGC. Peak AGC is effective for input signals in which the sync signal level is appropriate and only the active video signal is large.

Sync signal level of composite video signal and S (Y/C) video signal input are shown as follows.

NTSC-M,J, NTSC-4.43, PAL-M……286mV
PAL-B,D,G,H,I,N, PAL-Nc, PAL-60, SECAM…… 300mV

Setting for ON/OFF of AGC Sub Address: 0x0C [0]

Name	Definition
AGC	[0]: AGC OFF [1]: AGC ON

Setting for AGC non-sensing range Sub Address: 0x0C [3:2]

Name	Definition
AGCC0 ~ AGCC1	[AGCC1 : AGCC0] [00]: ±2LSB [01]: ±3LSB [10]: ±4LSB [11]: None

[7.27.] ACC (Auto Color Control)

The ACC of the AK8859VQ measures the level of the input signal color burst and adjusts to the appropriate level. The ACC is not applicable to SECAM input signal.

NTSC-M,J, NTSC-4.43, PAL-M……286mV
PAL-B,D,G,H,I,N, PAL-Nc, PAL-60…… …… 300mV

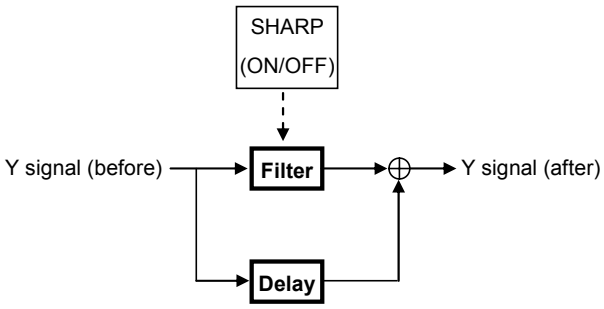
Setting for ON/OFF of ACC Sub Address: 0x0C [5]

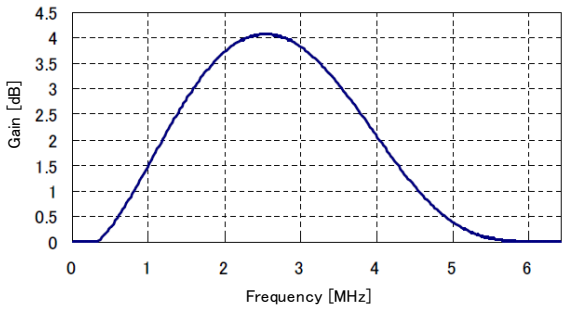
Name	Definition
ACC	[0]: ACC OFF [1]: ACC ON

The ACC and Color saturation functions operate independently. If ACC is enabled, the color saturation adjustment is applied to the signal that has been adjusted to the appropriate level by the ACC.

[7.28.] Sharpness adjustment

Sharpness adjustment is performed on the luminance signal. The filter characteristic is shown in the following diagram. A sharp image can be obtained by selection of the filter with the appropriate characteristics.





Setting for sharpness adjustment Sub Address: 0x0C [4]

Name	Definition
SHARP	[0]: No filtering [1]: Filter

[7.29.] Color Killer

In CVBS or S-video input, the chroma signal quality of the input signal is determined by comparison of its color burst level against the threshold setting in the color killer control register. If the level is below the threshold, the color killer is activated, resulting in processing of the input as a monochrome signal and thus with CbCr data fixed at 0x80.

Setting for color killer (Enable/Disable) activation Sub Address: 0x0C [7]

Name	Definition
CKILLDIS	[0]: Enable [1]: Disable

[7.30.] Image quality adjustment

Image quality adjustments consist of contrast, brightness, color saturation, and hue adjustment.

[7.30.1.] Contrast adjustment

Setting for contrast adjustment inclination Sub Address: 0x0D [6:0]

Register	Definition
CONT0 ~ CONT6	[CONTSEL-bit =[0]*] YOUT = (CONT / 64) x (YIN - 128) +128 [CONTSEL-bit =[1]*] YOUT = (CONT / 64) X YIN YOUT: Contrast obtained by the calculation YIN: Contrast before the calculation CONT: Contrast gain factor (register setting value) The gain factor can be set in the range {0~ (127 / 64)} in 1/64 step. Default setting value is 0x40.

As the register setting shown in the above table, contrast adjustment inclination can be selected between 50% and 0%.

Setting for contrast adjustment inclination Sub Address: 0x0C [6]

Register	Definition
CONTSEL	[0]: 50% [1]: 0%

[7.30.2.] Brightness adjustment

Setting for brightness adjustment Sub Address: 0x0E [6:0]

Name	Definition
BR0 ~ BR6	YOUT = YIN + (BR x 2) YOUT: Brightness obtained by the calculation YIN: Brightness before the calculation BR: Brightness gain factor (register setting value) The gain factor can be set in the range {-128 ~ 126} in step of 2. The setting is in 2's complement.

[7.30.3.] Color saturation adjustment

Setting for color saturation adjustment Sub Address: 0x0F [6:0]

Name	Definition
SAT0 ~ SAT6	COUT = (SAT / 64) X CIN COUT: Saturation obtained by the calculation CIN: Saturation before the calculation SAT: Saturation gain factor (register setting value) The gain factor can be set in the range {0~ (127 / 64)} in 1/64 step. Default setting value is 0x40.

[7.30.4.] HUE adjustment

Setting for HUE adjustment Sub Address: 0x10 [6:0]

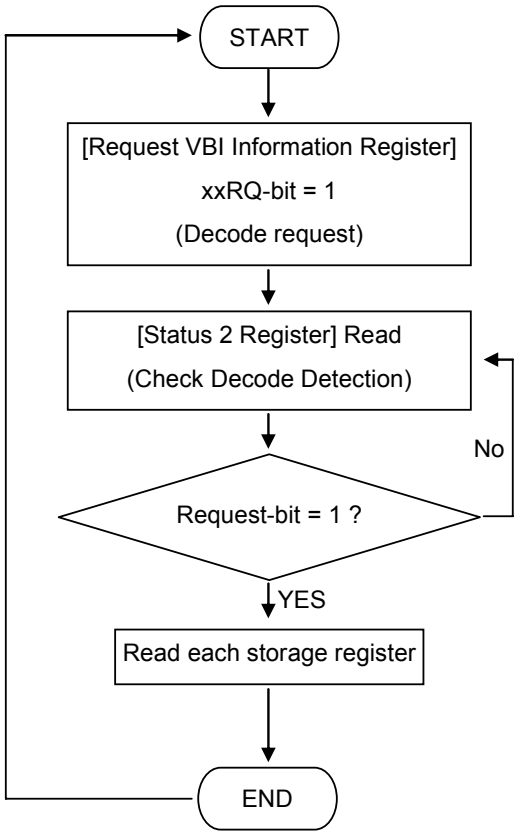
Name	Definition
HUE0 ~ HUE 6	The phase rotation can be set in the range of ±45° in 1/128step (about 0.70step). The setting is in 2's complement.

[7.31.] VBI information decoding

The AK8859VQ decodes closed-caption, closed-caption-extended, VBID(CGMS), and WSS signals on the vertical blanking signal, and writes the decoded data into a storage register. The AK8859VQ reads each data bit in Request VBI Information Register (Sub Address: 0x13 [3:0]) as a decoding request and thereupon enters a data wait state. Data detection and decoding to the storage register are then performed which indicates the presence or absence of data at STATUS 2 Register (Sub Address: 0x16 [3:0]) for host. The host can therefore determine the stored values by reading the respective storage registers. The value in each storage register is retained until a new value is written in by data renewal. For VBID data (CGMS-A), the CRCC code is decoded and only the arithmetic result is stored in the register.

Signal	Superimposed line	Notes
Closed Caption	Line21	525-Line
Closed Caption Extended Data	Line284	525-Line
VBID	Line20 / 283 Line20 / 333	525-Line 625-Line
WSS	Line23	625-Line

The storage registers for each of the signal types are as follows. For storage bit allocations, please refer to the respective register setting descriptions (Sub Address: 0x19 ~ 0x20).
Closed Caption 1 Register, Closed Caption 2 Register, WSS 1 Register, WSS 2 Register, Extended Data 1 Register, Extended Data 2 Register, VBID 1 Register, VBID 2 Register.



[7.32.] Internal status indicator

The AK8859VQ internal status can be acknowledged by reading the following registers.

[7.32.1.] Input signal indicator

Indicates presence or absence of signal Sub Address: 0x15 [0]

Name	Setting value	Definition	Notes
NOSIG	[0]	Signal detected	
	[1]	No signal detected	

[7.32.2.] Status of VLOCK mechanism

Indicates status of VLOCK Sub Address: 0x15 [1]

Name	Setting value	Definition	Notes
VLOCK	[0]	Synchronized	
	[1]	Not synchronized	

[7.32.3.] Interlace signal indicator

Indicates interlace or non-interlace of input signal Sub Address: 0x15 [2]

Name	Setting value	Definition	Notes
FRMSTD	[0]	Input signal 525/625 interlaced	
	[1]	Input signal not 525/625 interlaced	

[7.32.4.] Color killer operational

Indicates status of color killer (ON/OFF) Sub Address: 0x15 [3]

Name	Setting value	Definition	Notes
COLKILON	[0]	Not operation	
	[1]	Operation	

[7.32.5.] Clock mode

Indicates status of clock mode Sub Address: 0x15 [5:4]

Name	Setting value	Definition	Notes
SCLKMODE	[00]	Fixed-clock	
	[01]	Line-locked clock	
	[10]	Frame-locked clock	
	[11]	Reserved	

[7.32.6.] Luminance decode overflow

Indicates status of luminance decode result after passage through AGC block.

Sub Address: 0x15 [6]

Name	Setting value	Definition	Notes
PKWHITE	[0]	Normal	
	[1]	Overflow	

[7.32.7.] Color decode overflow

Indicates status of color decode result after passage through ACC block.

Sub Address: 0x15 [7]

Name	Setting value	Definition	Notes
OVCOL	[0]	Normal	
	[1]	Overflow	

[7.32.8.] AGC status

Indicates status of adaptive AGC Sub Address: 0x16 [5]

Name	Setting value		Notes
AGCSTS	[0]	Sync AGC operation	
	[1]	Peak AGC operation	

[7.33.] Macrovision signal detection

The AK8859VQ can detect a decode signal contains Macrovision signal.
The detection result can be confirmed via register.

Status of Macrovision signal detection. Sub Address: 0x17 [2:0]

Name	Definition
AGCDET	[0]: No Macrovision AGC process detected. [1]: Macrovision AGC process detected.
CSDET	[0]: No color stripe process detected. [1]: Color Stripe process detected.
CSTYPE	[0]: Color Stripe Type2 in input signal. [1]: Color Stripe Type3 in input signal.

[7.34.] Auto detection result of input video signal

In auto detection mode, the result can be acknowledged by reading the following register.

Indicates result and status of auto detection mode Sub Address: 0x18 [7:0]

Name	Definition
ST_VSCF0 ~ ST_VSCF1	Input video signal subcarrier frequency indicator [ST_VSCF1 : ST_VSCF0] (MHz) [00]: 3.57954545 (NTSC-M,J) [01]: 3.57561149 (PAL-M) [10]: 3.58205625 (PAL-Nc) [11]: 4.43361875 (PAL-B,D,G,H,I,N,60 , NTSC-4.43)
ST_VCEN0 ~ ST_VCEN1	Input signal color encode format indicator [ST_VCEN1 : ST_VCEN0] [00]: NTSC [01]: PAL [10]: SECAM [11]: Reserved
ST_VLF	Input signal line number indicator [0]: 525-Line (NTSC-M,J , NTSC-4.43 , PAL-M,60) [1]: 625-Line (PAL-B,D,G,H,I,N,Nc , SECAM)
ST_BW	Input signal monochrome indicator* [0]: Not monochrome [1]: Monochrome
UNDEF	Input signal detection indicator [0]: Input signal detected [1]: Input signal not detected
FIXED	Input signal detection process status [0]: Detection process in progress [1]: Detection process completed

*Monochrome auto detection is enabled if the color killer setting is ON(COLKILL-bit = [1]).
If the user has deliberately entered the B/W-bit setting, input signal detection is limited to 525/625 line detection only.

[8.] Device control interface

The AK8859VQ is controlled via I²C bus control interface, as described below.

[8.1.] I²C bus SLAVE Address

The I²C slave address can be selected by a SELA pin setting of either [1000100] and [1000101].

	Slave Address							
SELA pin status	MSB							LSB
Pulldown [Low]	1	0	0	0	1	0	0	R/W
Pullup [High]	1	0	0	0	1	0	1	R/W

[8.2.] I²C control sequence

[8.2.1.] Write sequence

After receiving a write-mode slave address first byte, the AK8859VQ receives the sub-address in the second byte and data in the subsequent bytes. The write sequence may be single-byte or multi-byte.

(a) Single-byte Write sequence

S	Slave Address	w	A	Sub Address	A	Data	A	stp
	8-bit		1-bit	8-bit	1-bit	8-bit	1-bit	

(b) Multi-byte (m-bytes) Write sequence (Sequential Write Operation)

S	Slave Address	w	A	Sub Address(n)	A	Data(n)	A	Data (n+1)	A	,,,,,,	Data (n+m)	A	stp
	8-bit		1-bit	8-bit	1-bit	8-bit	1-bit	8-bit	1-bit		8-bit	1-bit	

[8.2.2.] Read sequence

After receiving a read-mode slave address as first byte, the AK8859VQ sends data in the second and subsequent bytes.

S	Slave Address	w	A	Sub Address(n)	A	rS	Slave Address	R	A	Data1	A	Data2	A	Data3	A	,,,,
	8-bit		1	8-bit	1		8-bit		1	8-bit	1	8-bit	1	8-bit	1	

,,,,,,,,	,,,	Data n	!A	stp
		8-bit	1	

[8.2.3.] I²C General Call

AK8859VQ respond to General Call of I²C.

If second byte after receiving General Call is $0x06_{(HEX)}$, AK8859VQ initialize its register.

S	General Call Address	A	Second Byte	A	stp
	0x00 (Hex. 8-bit)	1-bit	0x06 (Hex. 8-bit)	1-bit	

DATA[7:0]-pin output:	Normal data output	H/L indefinite data output	Low output(Default State)

Abbreviations are follows.

S: Start Condition	rS: repeated Start Condition
A: Acknowledge (SDA Low)	!A: Not Acknowledge (SDA High)
stp: Stop Condition	R/W 1: Read 0: Write

: Received from master device (normally microprocessor)

: Output by slave device (AK8859VQ)

[9.] Register definitions

Sub Address	Register	Default	R/W	Function
0x00	Input Channel Select Register	0x00	R/W	Input channel setting
0x01	Clamp Control Register	0x00	R/W	Analog clamp circuit setting register
0x02	Input Video Standard Register	0x00	R/W	Input video signal setting
0x03	NDMODE Register	0x00	R/W	Auto detection limit setting
0x04	Output Format Register	0x00	R/W	Output data format setting
0x05	Output Pin Control Register	0x0F	R/W	Output pin status setting
0x06	Output Pin Polarity Set Register	0x00	R/W	Output pin polarity setting
0x07	Control 0 Register	0x00	R/W	Control register
0x08	Control 1 Register	0x00	R/W	Control register
0x09	Reserved Register	0x00	R/W	Reserved Register
0x0A	PGA1 Control Register	0x3C	R/W	PGA1 gain setting
0x0B	PGA2 Control Register	0x3C	R/W	PGA2 gain setting
0x0C	AGC and Color Control Register	0x00	R/W	AGC and Color Control
0x0D	Contrast Control Register	0x40	R/W	Contrast adjustment
0x0E	Brightness Control Register	0x00	R/W	Brightness adjustment
0x0F	Saturation Control Register	0x40	R/W	Color saturation adjustment
0x10	HUE Control Register	0x00	R/W	HUE adjustment
0x11	High Slice Data Set Register	0xEB	R/W	VBI Slice Data High setting
0x12	Low Slice Data Set Register	0x10	R/W	VBI Slice Data Low setting
0x13	Request VBI Information Register	0x00	R/W	VBI interval decode request setting
0x14	Reserved Register	0x00	R/W	Reserved Register
0x15	Status 1 Register		R	Internal status indicator
0x16	Status 2 Register		R	Internal status indicator
0x17	Macrovision Status Register		R	Input Macrovision signal indicator
0x18	Input Video Status Register		R	Input signal detection indicator
0x19	Closed Caption 1 Register		R	Closed Caption data indicator
0x1A	Closed Caption 2 Register		R	Closed Caption data indicator
0x1B	WSS 1 Register		R	WSS data indicator
0x1C	WSS 2 Register		R	WSS data indicator
0x1D	Extended Data 1 Register		R	Closed Caption Extended data indicator
0x1E	Extended Data 2 Register		R	Closed Caption Extended data indicator
0x1F	VBID 1 Register		R	VBID data indicator
0x20	VBID 2 Register		R	VBID data indicator
0x21	Device and Revision ID Register		R	Device ID and Revision ID

Sub Address	Register	Default	R/W	Function
0x22 ~ 0x2F	Reserved Register	0x00	R/W	Reserved Register
0x30	Reserved Register	0x0E	R/W	Reserved Register
0x31 ~ 0x3F	Reserved Register	0x00	R/W	Reserved Register

For all other registers, write-in is prohibited.
For all reserved registers, write-in must be limited to the default value.

[9.1.] Register setting overview

[9.1.1.] Sub Address 0x00 "Input Channel Select Register (R/W)"

Input signal channel selection and clock mode selection register.

Sub Address: 0x00 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMD	Reserved	Reserved	Reserved	Reserved	Reserved	AINSEL1	AINSEL0
Default Value							
0	0	0	0	0	0	0	0

Input Channel Select Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	AINSEL0 ~ AINSEL1	Analog Input Select	R/W	Input video signal selection [AINSEL1 : AINSEL0] [00]: AIN1 (CVBS) [01]: AIN2 (CVBS) [10]: AIN1(Y) / AIN2(C) (S-video) [11]: No input setting (Analog circuit is set to power-down*)
bit 2 ~ bit 6	Reserved	Reserved	R/W	Reserved
bit 7	CLKMD	Clock Mode	R/W	Clock mode selection [0]: For crystal [1]: External clock input (clock generator etc.)

*Clamp and ADC block is power-downed.

In used with AINSEL[1:0]=[11], Ouput data is depend on NSIGMD[1:0]–bit. However, in used with NSIGMD[1:0]=[10], DATA[7:0]-pin, HD-pin, VD_F-pin, VAR-pin and VARSUB-pin output Low.

[9.1.2.] Sub Address 0x01 “Clamp Control Register (R/W)”

Analog clamps circuit setting register.

Sub Address: 0x01 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	CLPWIDTH	Reserved	Reserved	CLPG1	CLPG0
Default Value							
0	0	0	0	0	0	0	0

Clamp Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	CLPG0 ~ CLPG1	Clamp Gain	R/W	Current value of clamp in analog circuit setting [00]: Min. [01]: Middle 1 {=(Min. x 3)} [10]: Middle 2 {=(Min. x 5)} [11]: Max. {=(Min. x 7)}
bit 2 ~ bit 3	Reserved	Reserved	R/W	Reserved
bit 4	CLPWIDTH	Clamp Pulse Width	R/W	Clamp pulse width setting. [0]: 275nsec [1]: 555nsec
bit 5 ~ bit 7	Reserved	Reserved	R/W	Reserved

[9.1.3.] Sub Address 0x02 “Input Video Standard Register (R/W)”

Input signal setting

Sub Address: 0x02 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AUTODET	SETUP	BW	VLF	VCEN1	VCEN0	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

Input Video Standard Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	VSCF0 ~ VSCF1	Video Sub-Carrier Frequency	R/W	Input video signal subcarrier frequency setting [VSCF1 : VSCF0] (MHz) [00]: 3.57954545 (NTSC-M,J) [01]: 3.57561149 (PAL-M) [10]: 3.58205625 (PAL-Nc) [11]: 4.43361875(PAL-B,D,G,H,I,N,60, NTSC-4.43, SECAM*)
bit 2 ~ bit 3	VCEN0 ~ VCEN1	Video Color Encode	R/W	Input signal color encode format setting [VCEN1 : VCEN0] [00]: NTSC [01]: PAL [10]: SECAM [11]: Reserved
bit 4	VLF	Video Line Frequency	R/W	Input signal line frequency setting [0]: 525-Line (NTSC-M,J, NTSC-4.43, PAL-M,60) [1]: 625-Line (PAL-B,D,G,H,I,N, PAL-Nc, SECAM)
bit 5	BW	Black & White	R/W	Monochrome mode (ON/OFF) setting [0]: Monochrome mode OFF [1]: Monochrome mode ON
bit 6	SETUP	Setup	R/W	Setup process setting [0]: Process as input signal with no setup [1]: Process as input signal with setup
bit 7	AUTODET	Video Standard Auto Detect	R/W	Input signal auto detection setting [0]: OFF (auto detection disabled; set manually) [1]: ON (auto detection enabled)

*For SECAM input signal, change VSCF[1:0] setting to [11].

[9.1.4.] Sub Address 0x03 "NDMODE Register (R/W)"

Limiting auto input video signal detection candidates register setting.

Sub Address: 0x03 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ND625L	ND525L	NDPAL60	NDNTSC443	Reserved	NDSECAM	NDPALNC	NDPALM
Default Value							
0	0	0	0	0	0	0	0

NDMODE Register Definition

Bit	Register Name		R/W	Definition
bit 0	NDPALM	No Detect PAL-M	R/W	[0]: PAL-M candidate [1]: PAL-M non-candidate
bit 1	NDPALNC	No Detect PAL-Nc	R/W	[0]: PAL-Nc candidate [1]: PAL-Nc non-candidate
bit 2	NDSECAM	No Detect SECAM	R/W	[0]: SECAM candidate [1]: SECAM non-candidate
bit 3	Reserved	Reserved	R/W	Reserved
bit 4	NDNTSC443	No Detect NTSC-4.43	R/W	[0]: NTSC-4.43 candidate [1]: NTSC-4.43 non-candidate
bit 5	NDPAL60	No Detect PAL-60	R/W	[0]: PAL-60 candidate [1]: PAL-60 non-candidate
bit 6	ND525L	No Detect 525Line	R/W	[0]: 525 line candidate [1]: 525 line non-candidate
bit 7	ND625L	No Detect 625Line	R/W	[0]: 625 line candidate [1]: 625 line non-candidate

In making the above register settings, the following restrictions apply,

1. Setting both NDNTSC443(bit 4) and NDPAL60(bit 5) to [1] (High) is prohibited.
2. Setting both ND525L(bit 6) and ND625L(bit 7) to [1] (High) is prohibited.
3. To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.

[9.1.5.] Sub Address 0x04 “Output Format Register (R/W)”

Output data format setting register.

Sub Address: 0x04 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBIDEC1	VBIDEC0	SLLVL	TRSVSEL	LIMIT601	VBIL2	VBIL1	VBIL0
Default Value							
0	0	0	0	0	0	0	0

Output Format Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 2	VBIL0 ~ VBIL2	Vertical Blanking Length	R/W	Vertical blanking interval length setting, entered as difference from the default settings The default settings are: 525LINE: Line1 ~ Line19 / Line263.5 ~ Line282.5 625LINE: Line623.5 ~ Line23.5 / Line311 ~ Line335 Examples of lengthening and shortening: If lengthened 1 line, the interval becomes 525LINE: Line1 ~ Line20 / Line263.5 ~ Line283.5 625LINE: Line623.5 ~ Line24.5 / Line311 ~ Line336 If shortened 1 line, the interval becomes 525LINE: Line1 ~ Line18 / Line263.5 ~ Line281.5 625LINE: Line623.5 ~ Line22.5 / Line311 ~ Line334 [VBIL2 : VBIL0] [001]: VBI lengthened 1 line [010]: VBI lengthened 2 lines [011]: VBI lengthened 3 lines [000]: Default [101]: VBI shortened 3 lines [110]: VBI shortened 2 lines [111]: VBI shortened 1 line [100]: Reserved
bit 3	LIMIT601	601 Output Limit	R/W	Output data code limit (Min-Max) setting [0]: 1-254 (Y/Cb/Cr) [1]: 16-235 (Y) / 16-240 (Cb/Cr)
bit 4	TRSVSEL	Time Reference Signal V Select	R/W	Setting of lines for “Time reference signal” V-bit value change in ITU-R BT.656 format 525-LINE input If setting [0]: V=1 (Line1 ~ Line9 / Line264 ~ Line272) V=0 (Line10 ~ Line263 / Line273 ~ Line525) If setting [1]: V=1 (Line1 ~ Line19 / Line264 ~ Line282) V=0 (Line20 ~ Line263 / Line283 ~ Line525)

				625-LINE input Always (regardless of setting on this register): V=1 (Line1 ~ Line22 / Line311 ~ Line335 / Line624 ~ Line625) V=0 (Line23 ~ Line310 / Line336 ~ Line623)
bit 5	SLLVL	Slice Level	R/W	Slice level setting [0]: Slice level approx. 25 IRE [1]: Slice level approx. 50 IRE
bit 6 ~ bit 7	VBIDEC0 ~ VBIDEC1	VBI Decode	R/W	Setting for type of data output during interval set in Vertical Blanking Interval register [VBIDEC1 : VBIDEC0] [00]: Black level data output [01]: Monochrome data output [10]: Slice result data output [11]: Reserved

[9.1.6.] Sub Address 0x05 "Output Pin Control Register (R/W)"

Output pins status setting register.

Sub Address: 0x05 Default Value: 0x0F

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VARSEL1	VARSEL0	VD_FSEL	OEN	HL	VARL	VD_FL	DL
Default Value							
0	0	0	0	1	1	1	1

Output Pin Control Register Definition

Bit	Register Name		R/W	Definition
bit 0	DL	D Output Low	R/W	[0]: Normal output [1]: [D17: D0] pin output fixed at Low
bit 1	VD_FL	VD/FIELD Low	R/W	[0]: Normal output [1]: VD_F pin output fixed at Low
bit 2	VARL	VAR Low	R/W	[0]: Normal output [1]: VAR pin output fixed at Low
bit 3	HL	HD Low	R/W	[0]: Normal output [1]: HD pin output fixed at Low
bit 4	OEN	Output Enable	R/W	[0]: Normal output for each digital output pins* [1]: Hi-Z output for each digital output pins.
bit 5	VD_FSEL	VD/FIELD Select	R/W	VD_F pin output signal selection. [0]: VD signal output [1]: FIELD signal output
bit 6 ~ bit 7	VARSEL0 ~ VARSEL1	DVALID/FIELD NSIG/LINE Select	R/W	VAR pin output signal selection [VARSEL1 : VARSEL0] [00]: DVALID signal output from VAR-pin NSIG signal output from VARSUB-pin [01]: FIELD signal output from VAR-pin LINE signal output from VARSUB-pin [10]: NSIG signal output from VAR-pin FIELD signal output from VARSUB-pin [11]: LINE signal output from VAR-pin DVALID signal output from VARSUB-pin

*Collective term for DTCLK, DATA[7:0], HD, VD_F, VAR and VARSUB pins.

However, the PDN pin states will have priority regardless of these register setting. When PDN pin is Low output, the output from the DTCLK, DATA[7:0], VD_F, VAR, VARSUB and HD pins is Low output.

[9.1.7.] Sub Address 0x06 “Output Pin Polarity Set Register (R/W)”

Output pins polarity setting register.

Sub Address: 0x06 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VARP	VD_FP	HDP	CLKINV	Reserved	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

Output Pin Polarity Set Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 3	Reserved	Reserved	R/W	Reserved
bit 4	CLKINV	CLK Invert Set	R/W	DTCLK signal output polarity setting. [0]: Normal output (write in data at rising edge) [1]: Data and clock reversed (write in data at falling edge)
bit 5	HDP	HD Pin Polarity Set	R/W	HD signal polarity setting [0]: Active Low [1]: Active High
bit 6	VD_FP	VD_F Pin Polarity Set	R/W	VD_F pin output signal polarity setting (If VD signal is output) [0]: Active Low [1]: Active High (If Field signal is output) [0]: Odd-Field Low, Even-Field High [1]: Even-Field Low, Odd-Field High
bit 7	VARP	VAR Pin Polarity Set	R/W	VAR and VARSUB pin output signal polarity setting (If DVALID signal is output) [0]: Active Low [1]: Active High (If Field signal is output) [0]: Odd-Field Low , Even-Field High [1]: Even-Field Low , Odd-Field High (If NSIG signal is output) [0]: When the input signal is absent the output is High. [1]: When the input signal is absent the output is Low. (If LINE signal is output) [0]: 525L-Low, 625L-High [1]: 625L-Low, 525L-High

[9.1.8.] Sub Address 0x07 “Control 0 Register (R/W)”

Sub Address: 0x07 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VERTS	ACTSTA2	ACTSTA1	ACTSTA0	NSIGMD1	NSIGMD0	DPAL1	DPAL0
Default Value							
0	0	0	0	0	0	0	0

Control 0 Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	DPAL0 ~ DPAL1	Deluxe PAL	R/W	Setting for color averaging* (PAL phase correction block) Also applicable to NTSC. [DPAL1 : DPAL0] [00]: Adaptive phase correction ON [01]: Phase correction ON [10]: Phase correction OFF [11]: Reserved
bit 2 ~ bit 3	NSIGMD0 ~ NSIGMD1	No Signal Output Mode	R/W	Setting for output on no-signal detection [NSIGMD1 : NSIGMD0] [00]: Black-level output [01]: Blue-level (Blueback) output [10]: Input status (sandstorm) output [11]: Reserved
bit 4 ~ bit 6	ACTSTA0 ~ ACTSTA2	Active Video Start	R/W	Fine-tuning video data decode start position delay or advance 1 sample unit is 13.5MHz (about 74ns) [ACTSTA2 : ACTSTA0] [001]: 1Sample delay [010]: 2Sample delay [011]: 3Sample delay [000]: Normal start position [101]: 3Sample advance [110]: 2Sample advance [111]: 1Sample advance [100]: Reserved
bit 7	VERTS	Vertical Sync Way	R/W	Vertical sync mechanism setting [0]: VLOCK mechanism [1]: Direct lock mechanism

[9.1.9.] Sub Address 0x08 "Control 1 Register (R/W)"

Sub Address: 0x08 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMODE1	CLKMODE0	INTPOL1	INTPOL0	Reserved	EAVSAVN	YCSEP1	YCSEP0
Default Value							
0	0	0	0	0	0	0	0

Control 1 Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 1	YCSEP0 ~ YCSEP1	YC Separation Control	R/W	Y/C separation setting [YCSEP1 : YCSEP0] [00]: Adaptive Y/C separation [01]: 1-dimensional Y/C separation [10]: 2-dimensional Y/C separation [11]: Reserved
bit2	EAVSAVN	EAV SAV Disable	R/W	EAV/SAV code output (ON/OFF) setting. [0]: EAV/SAV code is superimposed to output data. [1]: EAV/SAV code is not output.
bit 3	Reserved	Reserved	R/W	Reserved
bit 4 ~ bit 5	INTPOL0 ~ INTPOL1	Interpolator Mode Select	R/W	Pixel interpolator setting [INTPOL1 : INTPOL0] [00]: Auto [01]: ON [10]: OFF [11]: Reserved
bit 6 ~ bit 7	CLKMODE0 ~ CLKMODE1	Clock Mode Select	R/W	Clock mode setting [CLKMODE1 : CLKMODE0] [00]: Automatic transition mode [01]: Line-locked clock mode [10]: Frame-locked clock mode [11]: Fixed-clock mode

[9.1.10.] Sub Address 0x09 "Reserved Register (R/W)"

Reserved register.

Sub Address: 0x09 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

[9.1.11.] Sub Address 0x0A "PGA1 Control Register (R/W)"

PGA1 gain control setting register.
PGA1 is used for CVBS and Y signals gain processing.

Sub Address: 0x0A Default Value: 0x3C

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PGA1_7	PGA1_6	PGA1_5	PGA1_4	PGA1_3	PGA1_2	PGA1_1	PGA1_0
Default Value							
0	0	1	1	1	1	0	0

PGA1 Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	PGA1_0 ~ PGA1_7	PGA1 Gain Set	R/W	PGA1 gain setting. PGA gain is set by follows equation.

[9.1.12.] Sub Address 0x0B "PGA2 Control Register (R/W)"

PGA2 gain control setting register.
PGA2 is used for C signal gain processing.

Sub Address: 0x0B Default Value: 0x3C

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PGA2_7	PGA2_6	PGA2_5	PGA2_4	PGA2_3	PGA2_2	PGA2_1	PGA2_0
Default Value							
0	0	1	1	1	1	0	0

PGA2 Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	PGA2_0 ~ PGA2_7	PGA2 Gain Set	R/W	PGA2 gain setting. PGA gain is set by follows equation.

PGA gain equation:

$$\text{Gain(dB)} = 20LOG\left(\frac{(2.5\times PGA)+251.5}{401.5}\right)$$

**PGA*:* PGA1 or PGA2 register value$_{(Dec.)}$

Default gain setting is 0x3C$_{(HEX)}$=0.00dB.

[9.1.13.] Sub Address 0x0C "AGC and Color Control Register (R/W)"

AGC and Color setting register.

Sub Address: 0x0C Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CKILLDIS	CONTSEL	ACC	SHARP	AGCC1	AGCC0	Reserved	AGC
Default Value							
0	0	0	0	0	0	0	0

AGC and Color Control Register Definition

Bit	Register Name		R/W	Definition
bit 0	AGC	AGC Setting	R/W	AGC (ON/OFF) setting. [0]: AGC OFF [1]: AGC ON
bit 1	Reserved	Reserved	R/W	Reserved
bit 2 ~ bit 3	AGCC0 ~ AGCC1	AGC Coring Control	R/W	AGC non-sensing bandwidth (LSB) setting [AGCC1 : AGCC0] [00]: ±2LSB [01]: ±3LSB [10]: ±4LSB [11]: No non-sensing band
bit 4	SHARP	SHARP	R/W	Sharpness adjustment setting [0]: No filtering [1]: Filter
bit 5	ACC	ACC Setting	R/W	ACC (ON/OFF) setting [0]: ACC OFF [1]: ACC ON
bit 6	CONTSEL	Contrast Select	R/W	Contrast inclination selector [0]: 50% [1]: 0%
bit 7	CKILLDISS	Color killer Disable Set	R/W	Color killer Enable/Disable setting [0]: Enable [1]: Disable

[9.1.14.] Sub Address 0x0D "Contrast Control Register (R/W)"

Contrast adjustment setting register.

Sub Address: 0x0D Default Value: 0x40

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
0	1	0	0	0	0	0	0

Contrast Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 6	CONT0 ~ CONT6	Contrast Control	R/W	Contrast adjustment setting [If CONTSEL-bit =[0]] YOUT = (CONT / 64) x (YIN - 128) +128 [If CONTSEL-bit =[1]] YOUT = (CONT / 64) X YIN YOUT: Contrast obtained by the calculation YIN: Contrast before the calculation CONT: Contrast gain factor (register setting value) Register for contrast adjustment in steps of 1/64 in range {0~ (127 / 64)}. Default value is 0x40.
bit 7	Reserved	Reserved	R/W	Reserved

[9.1.15.] Sub Address 0x0E "Brightness Control Register (R/W)"

Brightness adjustment setting register.

Sub Address: 0x0E Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

Brightness Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 6	BR0 ~ BR6	Brightness Control	R/W	Brightness adjustment setting YOUT = YIN + (BR x 2) YOUT: Brightness obtained by the calculation YIN: Brightness before the calculation BR: Brightness gain factor (register setting value) Register for brightness adjustment in steps of 2 in range of {-128 ~ 126}. Brightness setting is in 2's complement.
bit 7	Reserved	Reserved	R/W	Reserved

[9.1.16.] Sub Address 0x0F "Saturation Control Register (R/W)"

Color saturation adjustment setting register.

Sub Address: 0x0F Default Value: 0x40

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	SAT6	SAT 5	SAT 4	SAT 3	SAT 2	SAT 1	SAT 0
Default Value							
0	1	0	0	0	0	0	0

Saturation Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 6	SAT0 ~ SAT6	Saturation Control	R/W	Color saturation adjustment setting. COUT = (SAT / 64) X CIN COUT: Saturation obtained by the calculation CIN: Saturation before the calculation SAT: Saturation gain factor (register setting value) Register for saturation adjustment in steps of 1/64 in range {0~ (127 / 64)}. Default value is 0x40.
bit 7	Reserved	Reserved	R/W	Reserved

[9.1.17.] Sub Address 0x10 "HUE Control Register (R/W)"

HUE adjustment setting register.

Sub Address: 0x10 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	HUE6	HUE 5	HUE 4	HUE 3	HUE 2	HUE 1	HUE 0
Default Value							
0	0	0	0	0	0	0	0

HUE Control Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 6	HUE0 ~ HUE 6	HUE Control	R/W	HUE adjustment setting Register for hue adjustment in steps of 1/256 in range ±45° in 2's complement
bit 7	Reserved	Reserved	R/W	Reserved

[9.1.18.] Sub Address 0x11 "High Slice Data Set Register (R/W)"

Register for setting sliced data from VBI slicer to High value. Default code is 235.

Sub Address: 0x11 Default Value: 0xEB

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
H7	H6	H5	H4	H3	H2	H1	H0
Default Value							
1	1	1	0	1	0	1	1

High Slice Data Set Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	H0 ~ H7	High Data Set	R/W	Register for setting sliced data from VBI slicer to High value (Default code is 235). Important: Corresponds to 601 special code if set to 0x00 or 0xFF

[9.1.19.] Sub Address 0x12 "Low Slice Data Set Register (R/W)"

Register for setting sliced data from VBI slicer to Low value. Default code is 16.

Sub Address: 0x12 Default Value: 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
L7	L6	L5	L4	L3	L2	L1	L0
Default Value							
0	0	0	1	0	0	0	0

Low Slice Data Set Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 7	L0 ~ L7	Low Data Set	R/W	Register for setting sliced data from VBI slicer to Low value (Default code is 16). Important: Corresponds to 601 special code if set to 0x00 or 0xFF

[9.1.20.] Sub Address 0x13 "Request VBI Information Register (R/W)"

Requested decode data during VBI interval setting register.

Sub Address: 0x13 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	WSSRQ	VBIDRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Request VBI Information Register Definition

Bit	Register Name		R/W	Definition
bit 0	CCRQ	Closed Caption Decode Request	R/W	Setting (ON/OFF) for closed caption decode request [0]: No request (OFF) [1]: Request (ON)
bit 1	EXTRQ	Extended Data Decode Request	R/W	Setting (ON/OFF) for Extended Data decode request [0]: No request (OFF) [1]: Request (ON)
bit 2	VBIDRQ	VBID Decode Request	R/W	Setting (ON/OFF) for VBID decode request [0]: No request (OFF) [1]: Request (ON)
bit 3	WSSRQ	WSS Decode Request	R/W	Setting (ON/OFF) for WSS decode request [0]: No request (OFF) [1]: Request (ON)
bit 4 ~ bit 7	Reserved	Reserved	R/W	Reserved

[9.1.21.] Sub Address 0x14 "Reserved Register (R/W)"

Reserved register.

Sub Address: 0x14 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

[9.1.22.] Sub Address 0x15 "Status 1 Register (R Only)"

Internal status register.

Sub Address: 0x15

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OVCOL	PKWHITE	SCLKMD1	SCLKMD0	COLKILON	FRMSTD	VLOCK	NOSIG

Status 1 Register Definition

Bit	Register Name		R/W	Definition
bit 0	NOSIG	No Signal	R	Input signal indicator [0]: Input signal present [1]: Input signal absent
bit 1	VLOCK	Video Locked	R	Input signal VLOCK synchronization status indicator [0]: Input signal synchronized [1]: Input signal non-synchronized
bit 2	FRMSTD	Frame Standard	R	Input signal interlace status indicator [0]: Input signal 525/625 interlaced [1]: Input signal not 525/625 interlaced
bit 3	COLKILON	Color Killer	R	Color killer status indicator [0]: Color killer not operation [1]: Color killer operation
bit 4 ~ bit 5	SCLKMD0 ~ SCLKMD1	Clock Mode	R	Clock mode indicator [SCLKMD1 : SCLKMD0] [00]: Fixed-clock mode [01]: Line-locked clock mode [10]: Frame-locked clock mode [11]: Reserved
bit 6	PKWHITE	Peak White Detection	R	Luminance decode result flow status indicator, after passage through AGC block [0]: Normal [1]: Overflow
bit 7	OVCOL	Over Color Level	R	Color decode result flow status indicator, after passage through ACC block [0]: Normal [1]: Overflow

[9.1.23.] Sub Address 0x16 "Status 2 Register (R Only)"

Internal status register.

Sub Address: 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	AGCSTS	Reserved	WSSDET	VBIDDET	EXTDET	CCDET

Status 2 Register Definition

Bit	Register Name		R/W	Definition
bit 0	CCDET	Closed Caption Detect	R	Indicator for presence of decoded data in Closed Caption 1, 2 Register [0]: No closed caption data present [1]: Closed caption Data present
bit 1	EXTDET	Extended Data Detect	R	Indicator for presence of decoded data in Extended Data 1, 2 Register [0]: No extended data present [1]: Extended data present
bit 2	VBIDDET	VBID Data Detect	R	Indicator for presence of decoded data in VBID 1/2 Register [0]: No VBID data present [1]: VBID data present
bit 3	WSSDET	WSS Data Detect	R	Indicator for presence of decoded data in WSS 1/2 Register [0]: No WSS data present [1]: WSS data present
bit 4	Reserved	Reserved	R	Reserved
bit 5	AGCSTS	AGC Status	R	[0]: Sync AGC active [1]: Peak AGC active
bit 6 ~ bit 7	Reserved	Reserved	R	Reserved

[9.1.24.] Sub Address 0x17 "Macrovision Status Register (R Only)"

Macrovision signal status register.

Sub Address: 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	CSTYPE	CSDET	AGCDET

Macrovision Status Register Definition

Bit	Register Name		R/W	Definition
bit 0	AGCDET	AGC Process Detect	R	Indicator for presence of Macrovision AGC in input signal [0]: No Macrovision AGC present [1]: Macrovision AGC present
bit 1	CSDET	Color Stripe Detect	R	Indicator for presence of Macrovision Color Stripe in input signal [0]: No Color Stripe present [1]: Color Stripe present
bit 2	CSTYPE	Color Stripe Type	R	Indicator for type of Color Stripe included in input signal [0]: Color Stripe Type2 [1]: Color Stripe Type3
bit 3 ~ bit 7	Reserved	Reserved	R	Reserved

[9.1.25.] Sub Address 0x18 "Input Video Status Register (R Only)"

Input video status register for auto detection mode.

Sub Address: 0x18

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIXED	UNDEF	ST_B/W	ST_VLF	ST_VCEN1	ST_VCEN0	ST_VSCF1	ST_VSCF0

Input Video Status Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	ST_VSCF0 ~ ST_VSCF1	Status of Video Sub-Carrier Frequency	R	Input video signal subcarrier frequency indicator [ST_VSCF1 : ST_VSCF0] (MHz) [00]: 3.57954545 (NTSC-M,J) [01]: 3.57561149 (PAL-M) [10]: 3.58205625 (PAL-Nc) [11]: 4.43361875 (PAL-B,D,G,H,I,N,60,NTSC-4.43,SECAM*)
bit 2 ~ bit 3	ST_VCEN0 ~ ST_VCEN1	Status of Video Color Encode	R	Input signal color encode format indicator [ST_VCEN1 : ST_VCEN0] [00]: NTSC [01]: PAL [10]: SECAM [11]: Reserved
bit 4	ST_VLF	Status of Video Line Frequency	R	Input signal line frequency setting [0]: 525-Line (NTSC-M,J, NTSC-4.43, PAL-M,60) [1]: 625-Line (PAL-B,D,G,H,I,N, PAL-Nc, SECAM)
bit 5	ST_BW	Status of B/W Signal	R	Monochrome mode (ON/OFF) setting [0]: Monochrome mode OFF [1]: Monochrome mode ON
bit 6	UNDEF	Un_define	R	Setup process setting [0]: Process as input signal with no setup [1]: Process as input signal with setup
bit 7	FIXED	Input Video Standard fixed	R	Input signal auto detection setting [0]: OFF (auto detection disabled; set manually) [1]: ON (auto detection enabled)

*For SECAM input signal, change VSCF[1:0] setting to [11].

[9.1.26.] Sub Address 0x19 "Closed Caption 1 Register (R Only)"

Closed Caption data storage register Sub Address: 0x19

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

[9.1.27.] Sub Address 0x1A "Closed Caption 2 Register (R Only)"

Closed Caption data storage register Sub Address: 0x1A

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	Bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

[9.1.28.] Sub Address 0x1B "WSS 1 Register (R Only)"

WSS data storage register Sub Address: 0x1B

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WSS2-7	WSS2-6	WSS2-5	WSS2-4	WSS1-3	WSS1-2	WSS1-1	WSS1-0

[9.1.29.] Sub Address 0x1C "WSS 2 Register (R Only)"

WSS data storage register Sub Address: 0x1C

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	WSS4-13	WSS4-12	WSS4-11	WSS3-10	WSS3-9	WSS3-8

[9.1.30.] Sub Address 0x1D "Extended Data 1 Register (R Only)"

Closed Caption Extended data storage register Sub Address: 0x1D

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

[9.1.31.] Sub Address 0x1E "Extended Data 2 Register (R Only)"

Closed Caption Extended data storage register Sub Address: 0x1E

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

[9.1.32.] Sub Address 0x1F "VBID 1 Register (R Only)"

VBID data storage register Sub Address: 0x1F

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

[9.1.33.] Sub Address 0x20 "VBID 2 Register (R Only)"

VBID data storage register Sub Address: 0x20

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

[9.1.34.] Sub Address 0x21 "Device and Revision ID Register (R Only)"

Device ID and Revision information indicator.

Device ID: 0x3B
Revision ID: Initially 0x00; revision number changes only when control software should be modified.

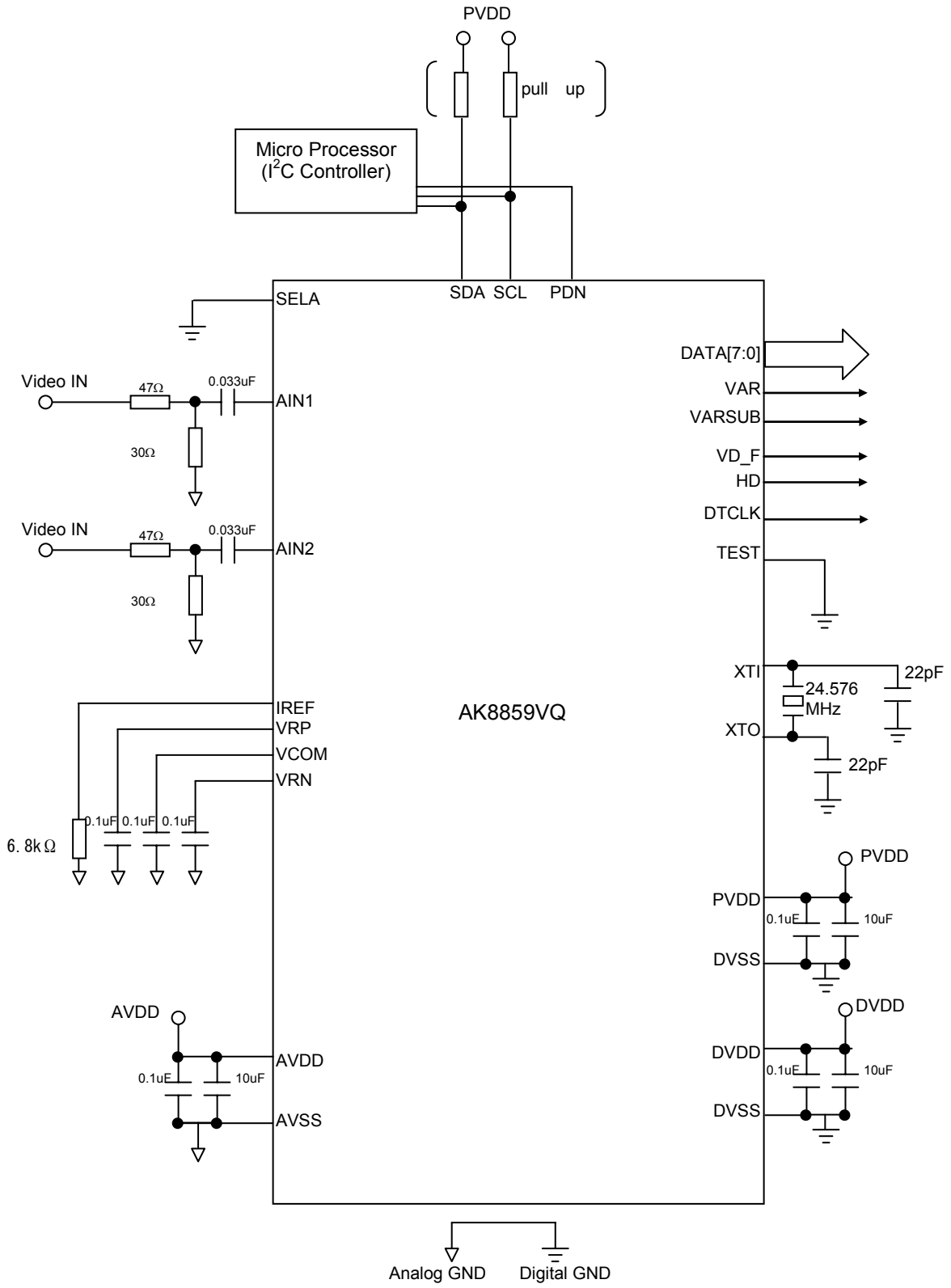
Sub Address: 0x21

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV1	REV0	DID5	DID4	DID3	DID2	DID1	DID0
Default Value							
0	0	1	1	1	0	1	1

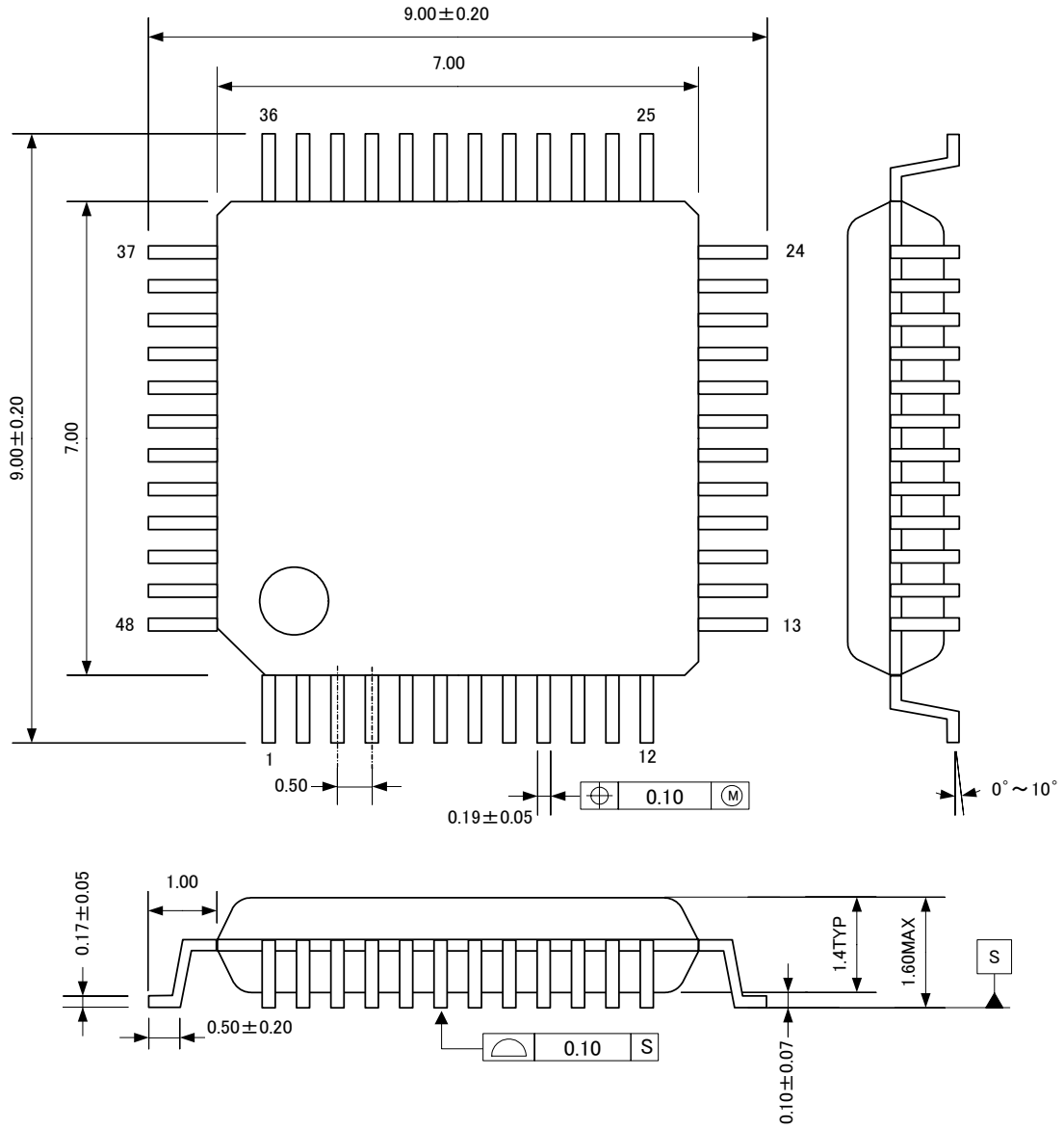
Device and Revision ID Register Definition

Bit	Register Name		R/W	Definition
bit 0 ~ bit 5	DID0 ~ DID5	Device ID	R	Device ID indicator (0x3B)
bit 6 ~ bit 7	REV0 ~ REV1	Revision ID	R	Revision ID indicator (initially 0x00)

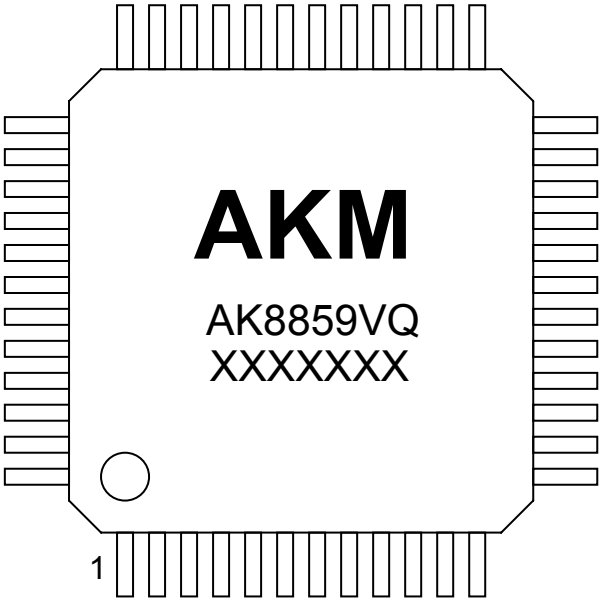
[10.] System connection example



[11.] Package


9.00±0.20
7.00
36
25
37
24
48
13
1
12
9.00±0.20
7.00
0.50
0.19±0.05
0.10
M
0°～10°
0.17±0.05
1.00
0.50±0.20
0.10
S
1.4TYP
1.60MAX
S
0.10±0.07

[12.] Marking



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