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Team Nexperia

IP3337CX18

7-channel integrated LC-filter network with ESD input protection to IEC 61000-4-2 level 4

Rev. 02 — 10 March 2009 Product data sheet

1. Product profile

1.1 General description

The IP3337CX18 is a 7-channel[1] LC low-pass filter network designed to filter undesired RF signals in the 800 MHz to 3000 MHz frequency band. In addition, the IP3337CX18 incorporates diodes which protect downstream components from ElectroStatic Discharge (ESD) voltages as high as 15 kV.

The IP3337CX18 is fabricated using monolithic silicon technology and integrates 7 inductors, 14 back-to-back diodes in a single Wafer-Level Chip-Scale Package (WLCSP) measuring 2.06 mm by 1.66 mm (typical). These features make the IP3337CX18 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features

- Pb-free, RoHS compliant and halogen free package; Dark Green compliant
- Integrated 7-channel π-type LC-filter network with 60 nH channel inductance
- 125 Ω series resistance, 25 pF (typical) capacitance per line
- Integrated ESD protection withstanding ±15 kV contact discharge, far exceeding IEC 61000-4-2, level 4
- WLCSP with 0.4 mm pitch

1.3 Applications

- Cellular and PCS mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems and PDAs

1. Available as a 10-channel device (IP3338CX24).

founded by Philips

2. Pinning information

2.1 Pinning

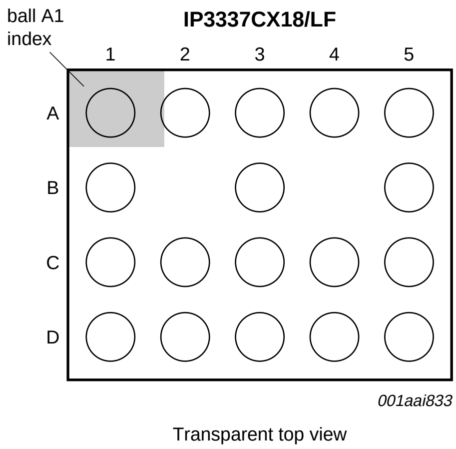


Fig 1. Pin configuration IP3337CX18

Table 1. Pinning

Pin	Description
A2 and A5	filter channel 1
A1 and A4	filter channel 2
B1 and B5	filter channel 3
C2 and C5	filter channel 4
C1 and C4	filter channel 5
D2 and D5	filter channel 6
D1 and D4	filter channel 7
A3, B3, C3, D3	ground
B2 and B4	no balls

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP3337CX18/LF	WLCSP18	wafer level chip-size package; 18 bumps; 2.06 × 1.66 × 0.61 mm	IP3337CX18/LF

4. Functional diagram

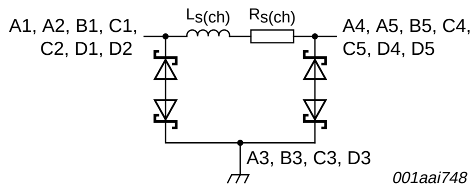


Fig 2. Schematic diagram IP3337CX18

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		–4.0	+4.0	V
V_{ESD}	electrostatic discharge voltage	all pins to ground			
		contact discharge [1]	–15	+15	kV
		air discharge [1]	–15	+15	kV
		IEC 61000-4-2, level 4; all pins to ground			
		contact discharge	–8	+8	kV
		air discharge	–15	+15	kV
I_{ch}	channel current (DC)	T_{amb} = 70 °C	-	10	mA
$I_{ch(M)}$	peak channel current	T_{amb} = 70 °C; 60 s	-	50	mA
P_{ch}	channel power dissipation	continuous power; T_{amb} = 70 °C	-	10	mW
P_{tot}	total power dissipation	T_{amb} = 70 °C	-	70	mW
T_{stg}	storage temperature		–55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum	-	260	°C
T_{amb}	ambient temperature		–35	+85	°C

[1] Device tested with 1000 pulses of ±15 kV contact discharges, according to the IEC 61000-4-2 model, which far exceeds IEC 61000-4-2, level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	f = 0 Hz (DC)	100	125	150	Ω
C_{ch}	channel capacitance	$V_{bias(DC)}$ = 0 V; f = 1 MHz	-	25	30[1]	pF
$L_{s(ch)}$	channel series inductance	[1]	-	60	-	nH
V_{BR}	breakdown voltage	I_{test} = 1 mA	6	-	10	V
		I_{test} = –1 mA	–10	-	–6	V
I_{LR}	reverse leakage current	per channel; V_I = 3.0 V	-	-	100	nA

[1] Guaranteed by design.

Table 5. Frequency characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	R_{gen} = 50 Ω; R_L = 50 Ω				
		800 MHz < f < 1 GHz	38	40	-	dB
		1 GHz < f < 3 GHz	35	40	-	dB
		at 0 Hz; R_{gen} = 50 Ω; R_L = 50 Ω; $V_{bias(DC)}$ = 0 V	6	7	10	dB
f_{-3dB}	cut-off frequency	measured relative to insertion loss at DC; R_{gen} = 50 Ω; R_L = 50 Ω	150	180	-	MHz
α_{ct}	crosstalk attenuation	800 MHz < f < 3 GHz; R_{gen} = 50 Ω; R_L = 50 Ω	35	40	-	dB

7. Application information

7.1 Insertion loss

The setup for measuring insertion loss in a 50 Ω system is shown in Figure 3.

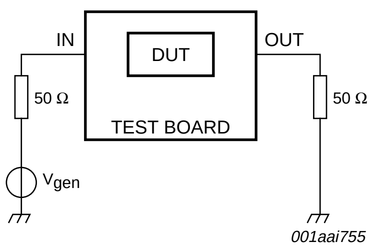
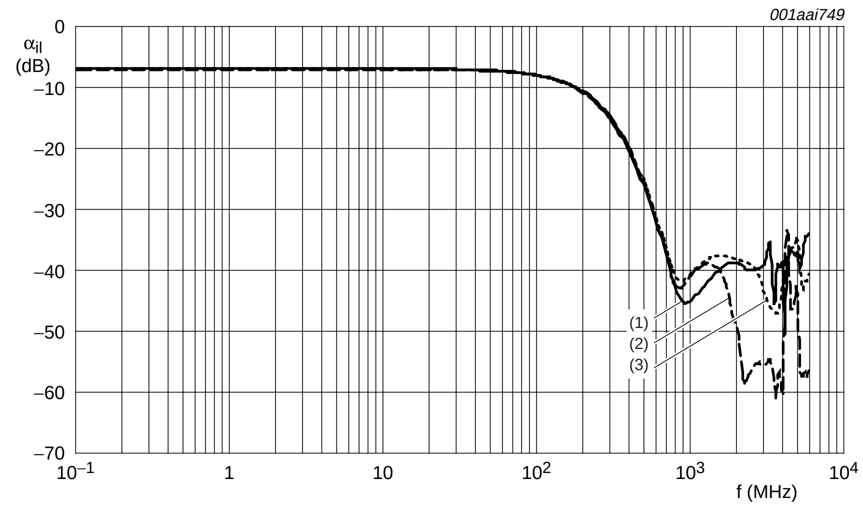


Fig 3. Frequency response measurement configuration

The measured frequency response curves for all channels are shown in Figure 4.



(1) Channel 2 (pins A1 and A4).

(2) Channel 5 (pins C1 and C4).

(3) Channel 7 (pins D1 and D4).

Fig 4. Measured frequency response curves

7.2 Crosstalk

The setup for measuring crosstalk in a 50 Ω system is shown in Figure 5.

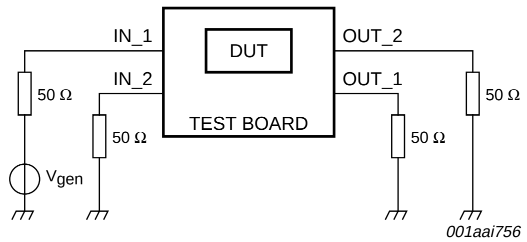
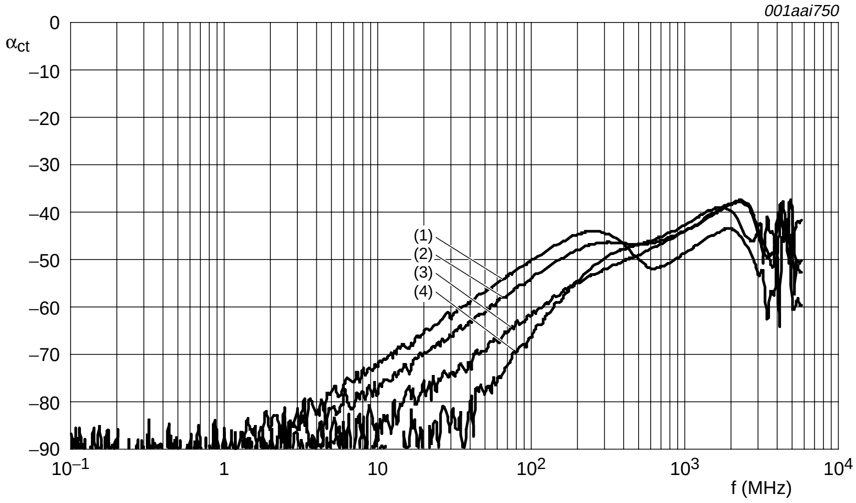


Fig 5. Crosstalk measurement configuration

The crosstalk between adjacent channels within the IP3337CX18 for different channel pairs measured in a 50 Ω NetWork Analyzer (NWA) system, is shown in Figure 6. In all cases, all unused connections are terminated with 50 Ω to ground.



(1) Channels 2 and 5 (pins A1 and C4).

(2) Channels 3 and 4 (pins B1 and C5).

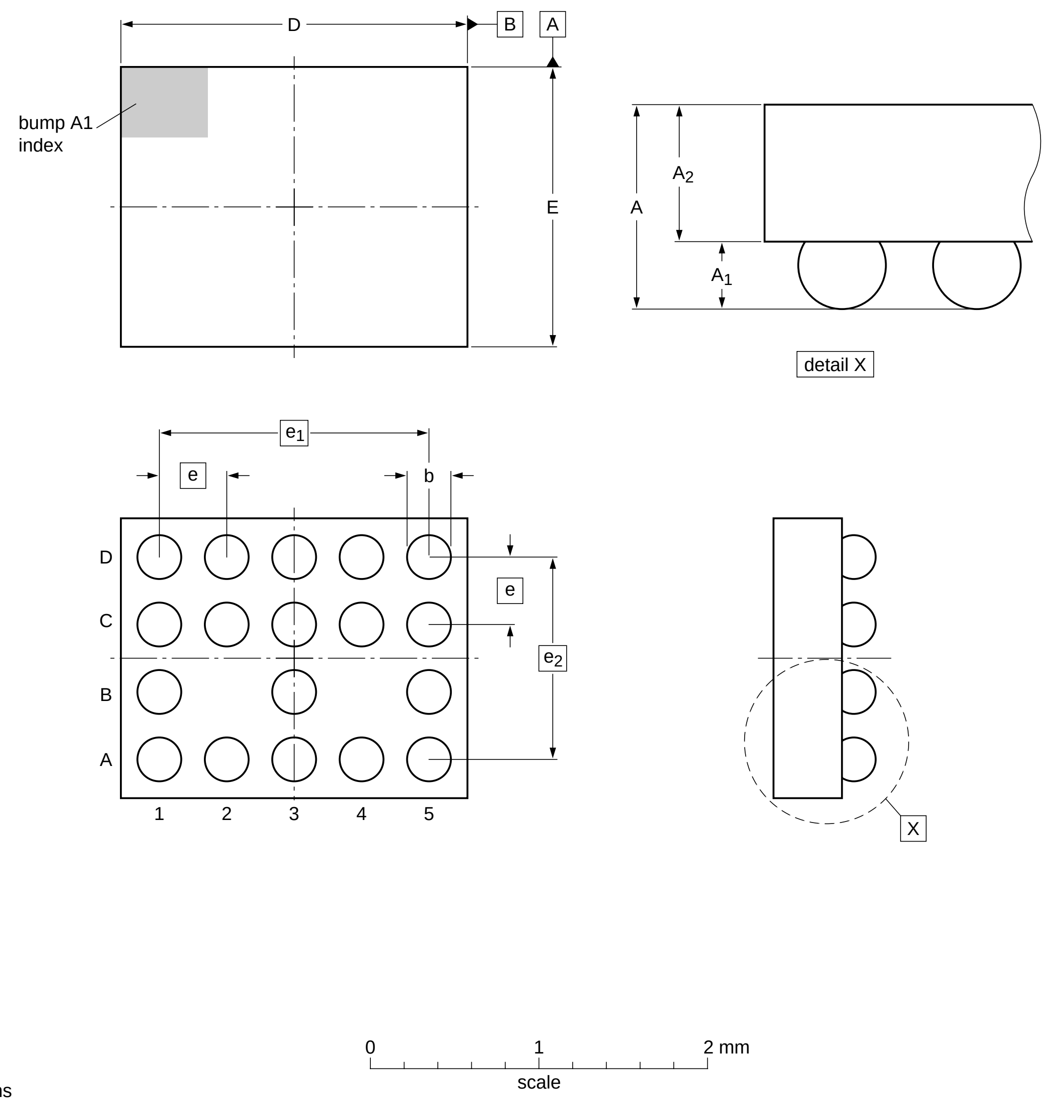
(3) Channels 3 and 6 (pins B1 and D5).

(4) Channels 2 and 1 (pins A1 and A5).

Fig 6. Measured crosstalk between adjacent channels

8. Package outline

WLCSP18: wafer level chip-size package; 18 bumps; 2.06 x 1.66 x 0.61 mm **IP3337CX18/LF**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2
	max	0.66	0.22		0.31	2.11	1.71			
mm	nom	0.61	0.20	0.41	0.26	2.06	1.66	0.4	1.6	1.2
	min	0.56	0.18		0.21	2.01	1.61			

ip3337cx18_lf_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
IP3337CX18/LF						~~08-08-08~~ 08-09-09

Fig 7. Package outline IP3337CX18/LF (WLCSP18)

9. Soldering of WLCSP packages

9.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 “Wafer Level Chip Scale Package”* and in application note *AN10365 “Surface mount reflow soldering description”*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

9.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

9.3 Reflow soldering

Key characteristics in reflow soldering are:

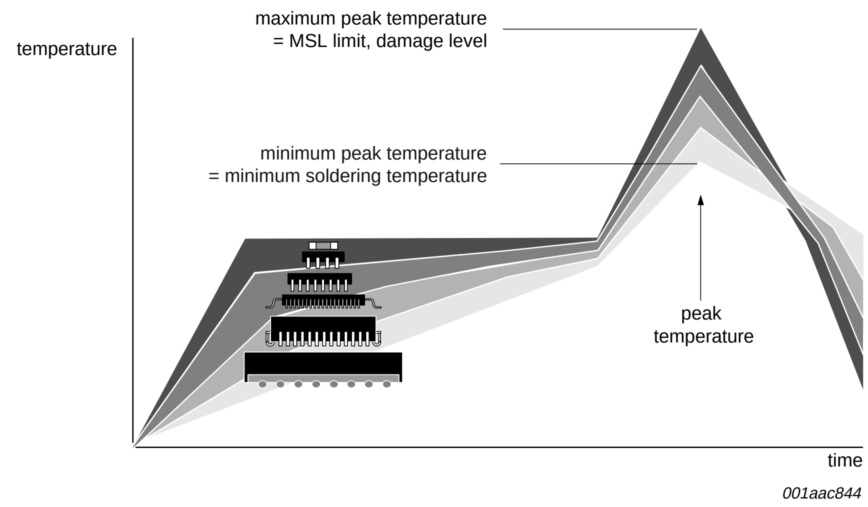
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 6.

Table 6. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

9.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

9.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

9.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

9.3.4 Cleaning

Cleaning can be done after reflow soldering.

10. Abbreviations

Table 7. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
NSMD	Non-Solder Mask Design
OSP	Organic Solderability Preservative
PCB	Printed-Circuit Board
PCS	Personal Communication System
PSU	Power Supply Unit
RoHS	Restriction of Hazardous Substances
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3337CX18_2	20090310	Product data sheet	-	IP3337CX18_1
Modifications:	• Figure 7 “Package outline IP3337CX18/LF (WLCSP18)” updated • Section 9 “Soldering of WLCSP packages” added • “Packing information” section removed • “Design and assembly recommendations” section removed			
IP3337CX18_1	20081112	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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