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Kind regards,

Team Nexperia

IP3348CX5; IP3348CX10; IP3348CX15; IP3348CX20

Integrated multi channel LC-filter network for high-speed data interfaces with ESD protection to IEC 61000-4-2 level 4

Rev. 1.1 — 4 April 2011 Product data sheet

1. Product profile

1.1 General description

IP3348CX5, IP3348CX10, IP3348CX15 and IP3348CX20 is a 2, 4, 6 and 8-channel LC low-pass filter network for high-speed data interfaces. It is designed to provide filtering of undesired RF signals in the 800 MHz to 3 GHz frequency band while supporting data rates up to 400 Mbit/s. In addition, IP3348CX5, IP3348CX10, IP3348CX15 and IP3348CX20 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±20 kV contact discharge according the IEC 61000-4-2 model, far exceeding standard level 4.

The devices are fabricated using monolithic silicon technology and integrate up to 8 inductors and up to 8 pairs of back-to-back diodes in a 0.4 mm pitch Wafer-Level Chip-Scale Package (WLCSP). These features make the IP3348CX5; IP3348CX10; IP3348CX15; IP3348CX20 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and other portable electronic devices.

1.2 Features and benefits

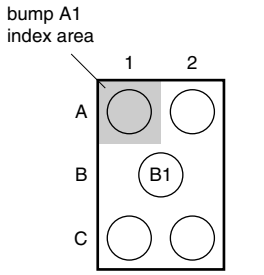
- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Supports data rates up to 400 Mbit/s
- Integrated ESD protection withstanding ±20 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- WLCSP with 0.4 mm pitch

1.3 Applications

- ElectroMagnetic Interference (EMI) filtering and ESD protection for high-speed data interfaces like Mobile Industry Processor Interface (MIPI) and Mobile Display Digital Interface (MDDI)
- Camera imager interface
- High resolution color Liquid Crystal Display (LCD) interfaces

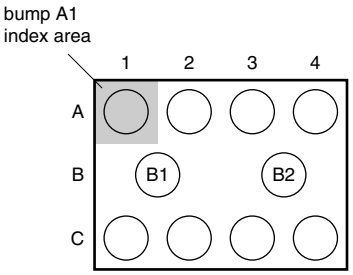
2. Pinning information

2.1 Pinning



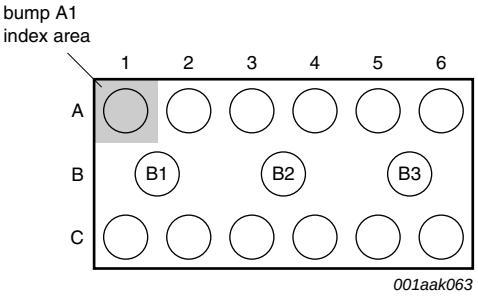
transparent top view,
solder balls facing down

Fig 1. Pin configuration IP3348CX5



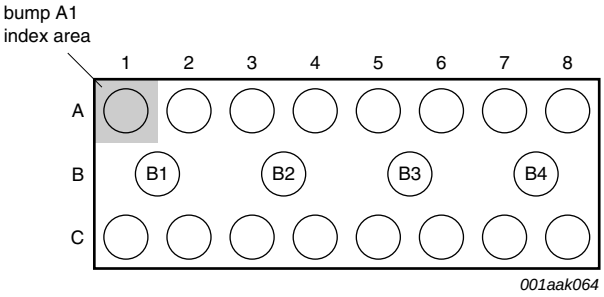
transparent top view,
solder balls facing down

Fig 2. Pin configuration IP3348CX10



transparent top view,
solder balls facing down

Fig 3. Pin configuration IP3348CX15



transparent top view,
solder balls facing down

Fig 4. Pin configuration IP3348CX20

2.2 Pin description

Table 1. Pinning

Pin				Description
IP3348CX5	IP3348CX10	IP3348CX15	IP3348CX20	
A1 and C1	A1 and C1	A1 and C1	A1 and C1	filter channel 1
A2 and C2	A2 and C2	A2 and C2	A2 and C2	filter channel 2
-	A3 and C3	A3 and C3	A3 and C3	filter channel 3
-	A4 and C4	A4 and C4	A4 and C4	filter channel 4
-	-	A5 and C5	A5 and C5	filter channel 5
-	-	A6 and C6	A6 and C6	filter channel 6
-	-	-	A7 and C7	filter channel 7
-	-	-	A8 and C8	filter channel 8
B1	B1 and B2	B1, B2 and B3	B1, B2, B3 and B4	ground

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP3348CX5	WLCSP5	wafer level chip-size package; 5 bumps (2-1-2)	IP3348CX5
IP3348CX10	WLCSP10	wafer level chip-size package; 10 bumps (4-2-4)	IP3348CX10
IP3348CX15	WLCSP15	wafer level chip-size package; 15 bumps (6-3-6)	IP3348CX15
IP3348CX20	WLCSP20	wafer level chip-size package; 20 bumps (8-4-8)	IP3348CX20

4. Functional diagram

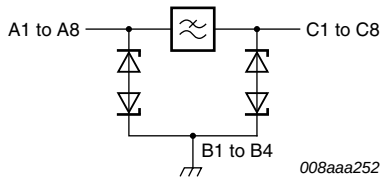


Fig 5. Schematic diagram of IP3348CX5; IP3348CX10; IP3348CX15; IP3348CX20

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			–4	+4	V
I_{ch}	channel current (DC)	T_{amb} = 85 °C		-	20	mA
V_{ESD}	electrostatic discharge voltage	all pins to ground				
		contact discharge; 10 pulses	[1]	–20	+20	kV
		air discharge		–20	+20	kV
		IEC 61000-4-2 level 4; all pins to ground				
		contact discharge		–8	+8	kV
		air discharge		–15	+15	kV
P_{ch}	channel power dissipation	continuous; T_{amb} = 85 °C		-	10	mW
T_{stg}	storage temperature			–55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum		-	260	°C
T_{amb}	ambient temperature			–40	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance			-	10	-	Ω
$L_{s(ch)}$	channel series inductance		[1]	-	15	-	nH
C_{ch}	channel capacitance	f = 100 kHz	[1]				
		$V_{bias(DC)}$ = 0 V		-	30	-	pF
		$V_{bias(DC)}$ = 2.5 V		-	25	-	pF
V_{BR}	breakdown voltage	I_{test} = 1 mA		5	-	10	V
		I_{test} = −1 mA		−10	-	−5	V
I_{LR}	reverse leakage current	per channel; V_I = 3 V		-	10	100	nA
		per channel; V_I = −3 V		−100	−10	-	nA

[1] Guaranteed by design.

Table 5. Frequency characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{il}	insertion loss	R_{gen} = 50 Ω; R_L = 50 Ω					
		800 MHz < f_i < 1 GHz		25	-	-	dB
		1 GHz < f_i < 3 GHz		30	40	-	dB
		f_i = 0 Hz; $V_{bias(DC)}$ = 0 V		-	-	1	dB
f_{-3dB}	cut-off frequency	R_{gen} = 50 Ω; R_L = 50 Ω	[1]	-	350	-	MHz
α_{ct}	crosstalk attenuation	R_{gen} = 50 Ω; R_L = 50 Ω; 800 MHz < f_i < 3 GHz		35	-	-	dB

[1] Measured relative to insertion loss at DC.

7. Application information

7.1 Insertion loss

The setup for measuring insertion loss in a 50 Ω system is shown in Figure 6.

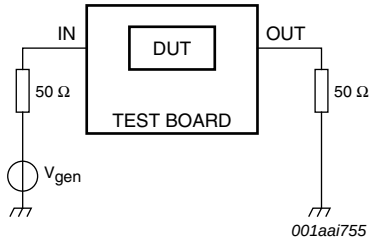
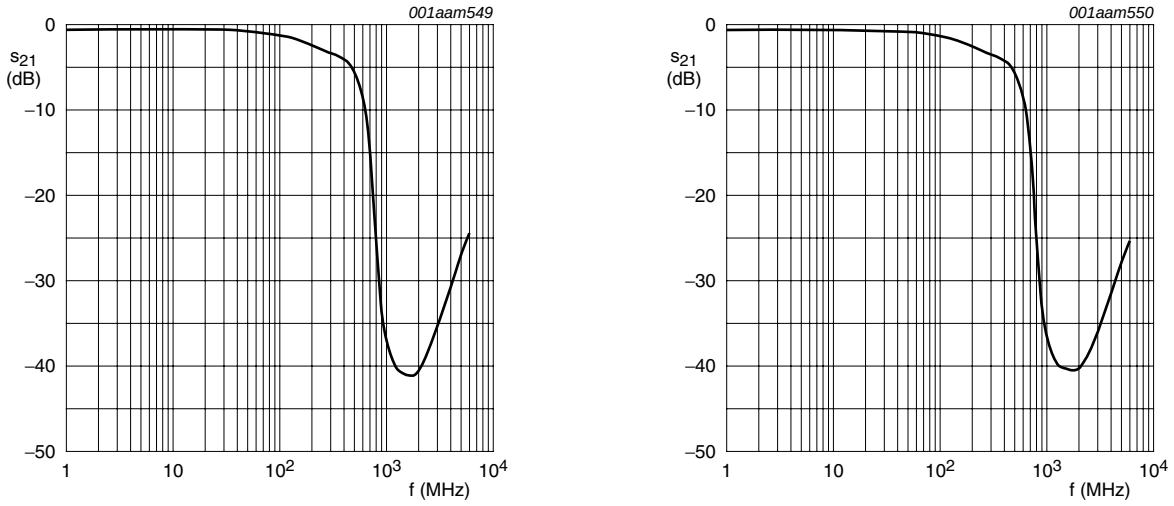


Fig 6. Frequency response measurement configuration

As an example, the insertion loss in a 50 Ω system for two channels of the IP3348CX15 are shown in Figure 7. The insertion loss is measured directly on the wafer with coplanar probes. Unused pins are connected to ground with 50 Ω.



a. Channel 2 (pin A2 to C2).

b. Channel 6 (pin A6 to C6).

Fig 7. Measured insertion loss magnitudes

7.2 Crosstalk

The crosstalk measurement configuration of a typical 50 Ω NetWork Analyzer (NWA) system for evaluation of the IP3348CX5, IP3348CX10, IP3348CX15 and IP3348CX20 is shown in Figure 8.

Four typical examples of crosstalk measurement results of IP3348CX15 are depicted. Unused channels are terminated with 50 Ω to ground.

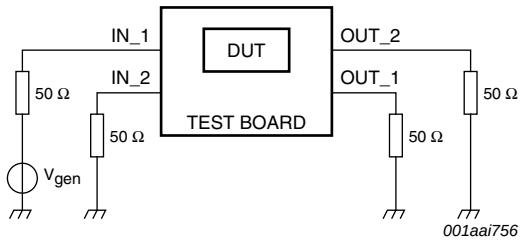
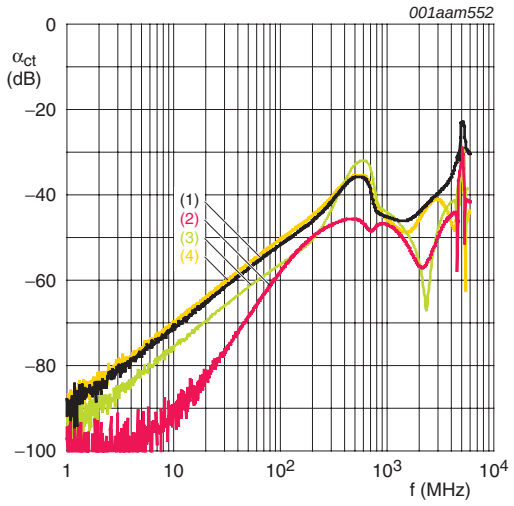


Fig 8. Crosstalk measurement configuration



(1) Channel 1 to 2 (pin A1 to C2).

(2) Channel 1 to 5 (pin A1 to C5).

(3) Channel 3 to 2 (pin A3 to C2).

(4) Channel 3 to 5 (pin A3 to C5).

Fig 9. Measured crosstalk between different channels using the example of IP3348CX15

7.3 Eye diagram

The transient behavior of the IP3348CX5, IP3348CX10, IP3348CX15 and IP3348CX20 at a data rate of 400 Mbit/s is shown in Figure 10 based on eye diagram measurements.

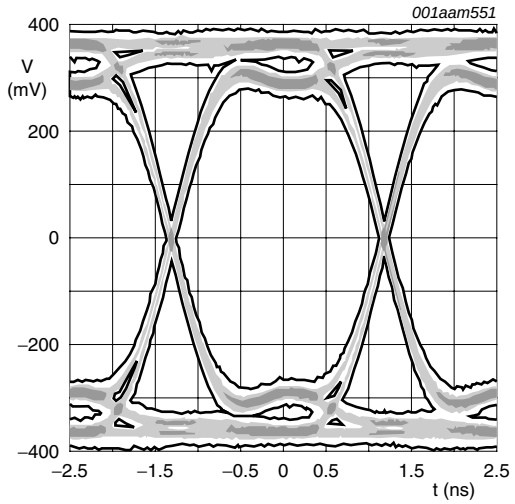


Fig 10. Eye diagram of the IP3348CXxy at a data rate of 400 Mbit/s

While Figure 10 shows the eye diagram of the IP3348CXxy for a data rate of 400 Mbit/s the time characteristics for different data rates can be found in Table 6.

Furthermore the percentage of time where the signal amplitude is above the MIPI receiver High-Speed (HS) mode threshold voltage of ±70 mV is shown, too. This is a good indicator for the achievable data rate in an MIPI HS mode application.

E.g. the IP3348CXxy can be used up to a data rate of 600 Mbit/s if the receiver is able to detect bits whose amplitudes are 75 % of time above the threshold.

Table 6. Eye diagram time characteristics

T_{amb} = 25 °C; unless otherwise specified.

Data rate [Mbit/s]	Period time [ns]	Δt @ ±70 mV [ns]	Time above MIPI HS mode threshold of ±70 mV [%]
300	3.33	3.04	91.3
350	2.85	2.56	89.3
400	2.50	2.20	88.0
450	2.22	1.89	85.1
500	2.00	1.63	81.5
550	1.81	1.42	78.4
600	1.66	1.26	75.9

8. Package outline

WLCSP5: wafer level chip-size package; 5 bumps (2-1-2)

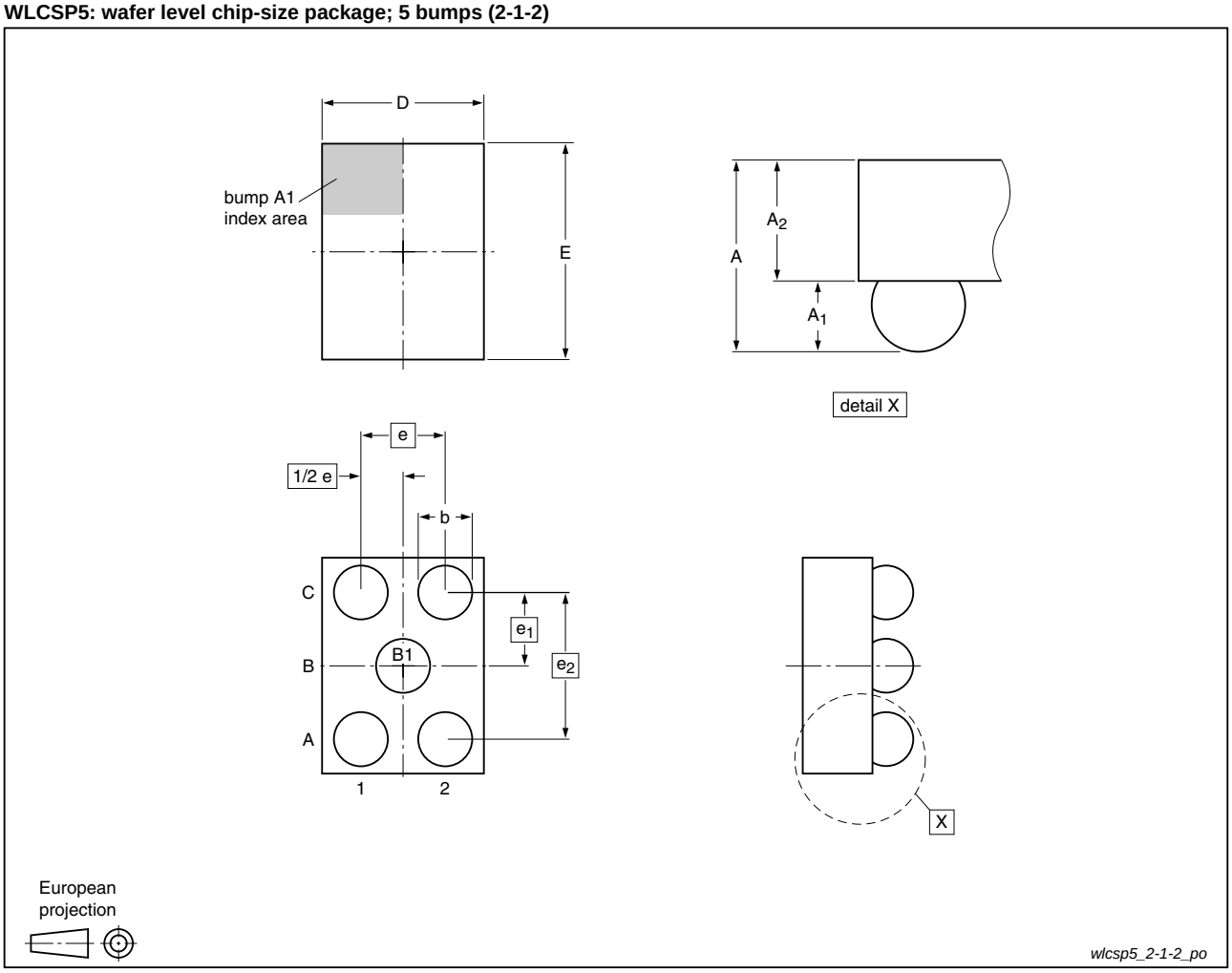


Fig 11. Package outline IP3348CX5 (WLCSP5)

Table 7. Dimensions for Figure 11

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	0.71	0.76	0.81	mm
E	1.01	1.06	1.11	mm
e	-	0.4	-	mm
e_1	-	0.346	-	mm
e_2	-	0.692	-	mm

WLCSP10: wafer level chip-size package; 10 bumps (4-2-4)

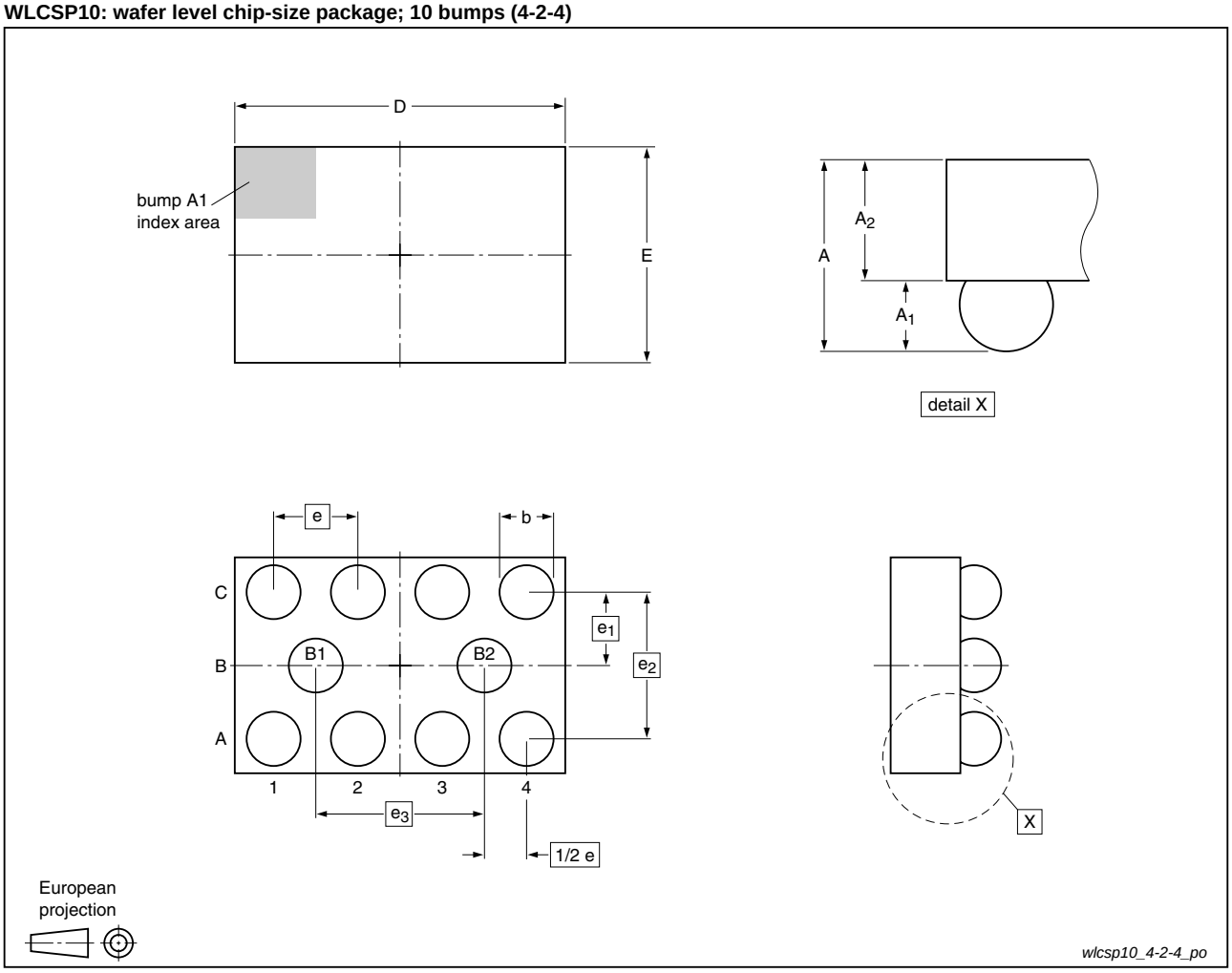


Fig 12. Package outline IP3348CX10 (WLCSP10)

Table 8. Dimensions for Figure 12

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	1.51	1.56	1.61	mm
E	1.01	1.06	1.11	mm
e	-	0.4	-	mm
e_1	-	0.346	-	mm
e_2	-	0.692	-	mm
e_3	-	0.8	-	mm

WLCSP15: wafer level chip-size package; 15 bumps (6-3-6)

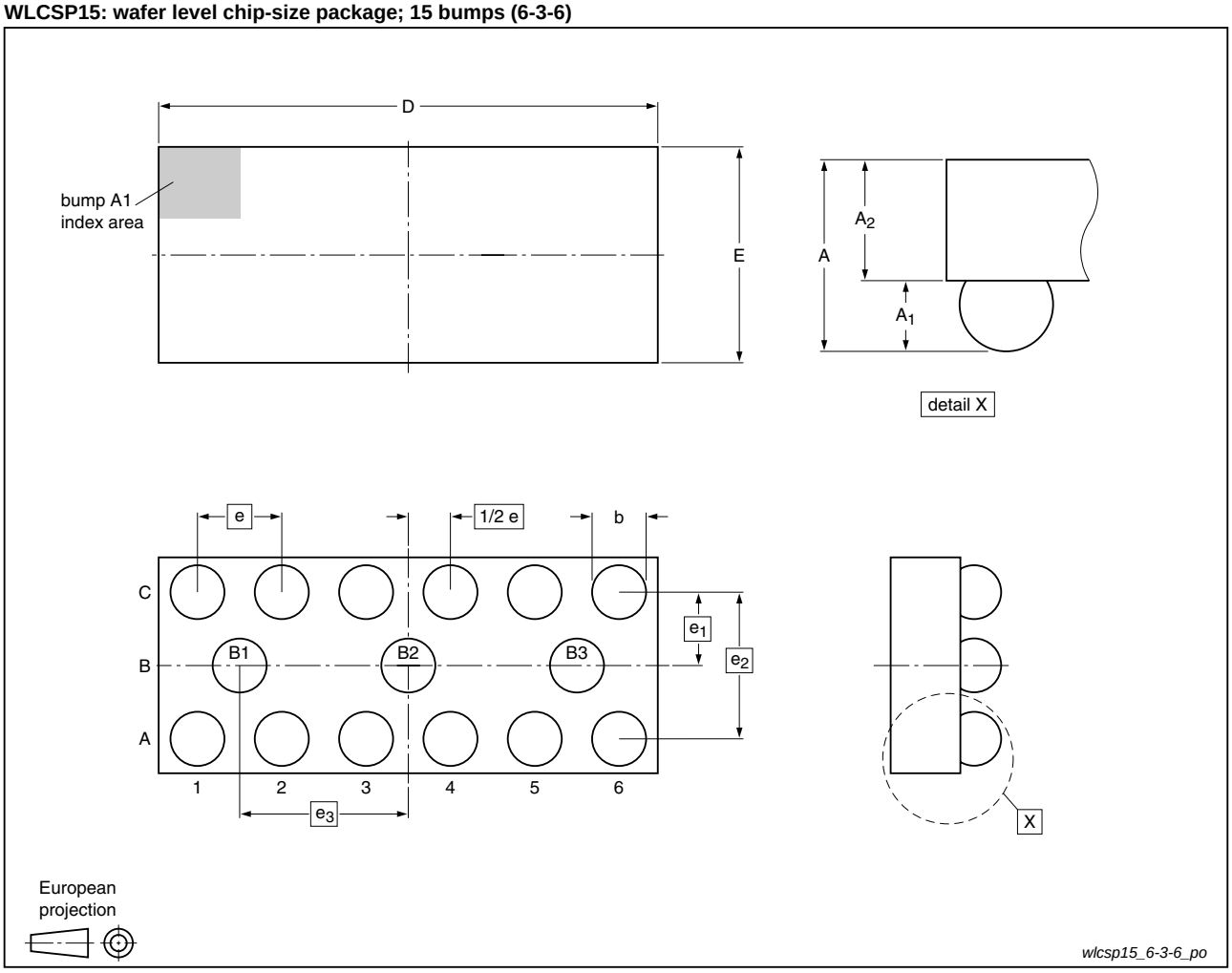


Fig 13. Package outline IP3348CX15 (WLCSP15)

Table 9. Dimensions for Figure 13

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	2.31	2.36	2.41	mm
E	1.01	1.06	1.11	mm
e	-	0.4	-	mm
e_1	-	0.346	-	mm
e_2	-	0.692	-	mm
e_3	-	0.8	-	mm

WLCSP20: wafer level chip-size package; 20 bumps (8-4-8)

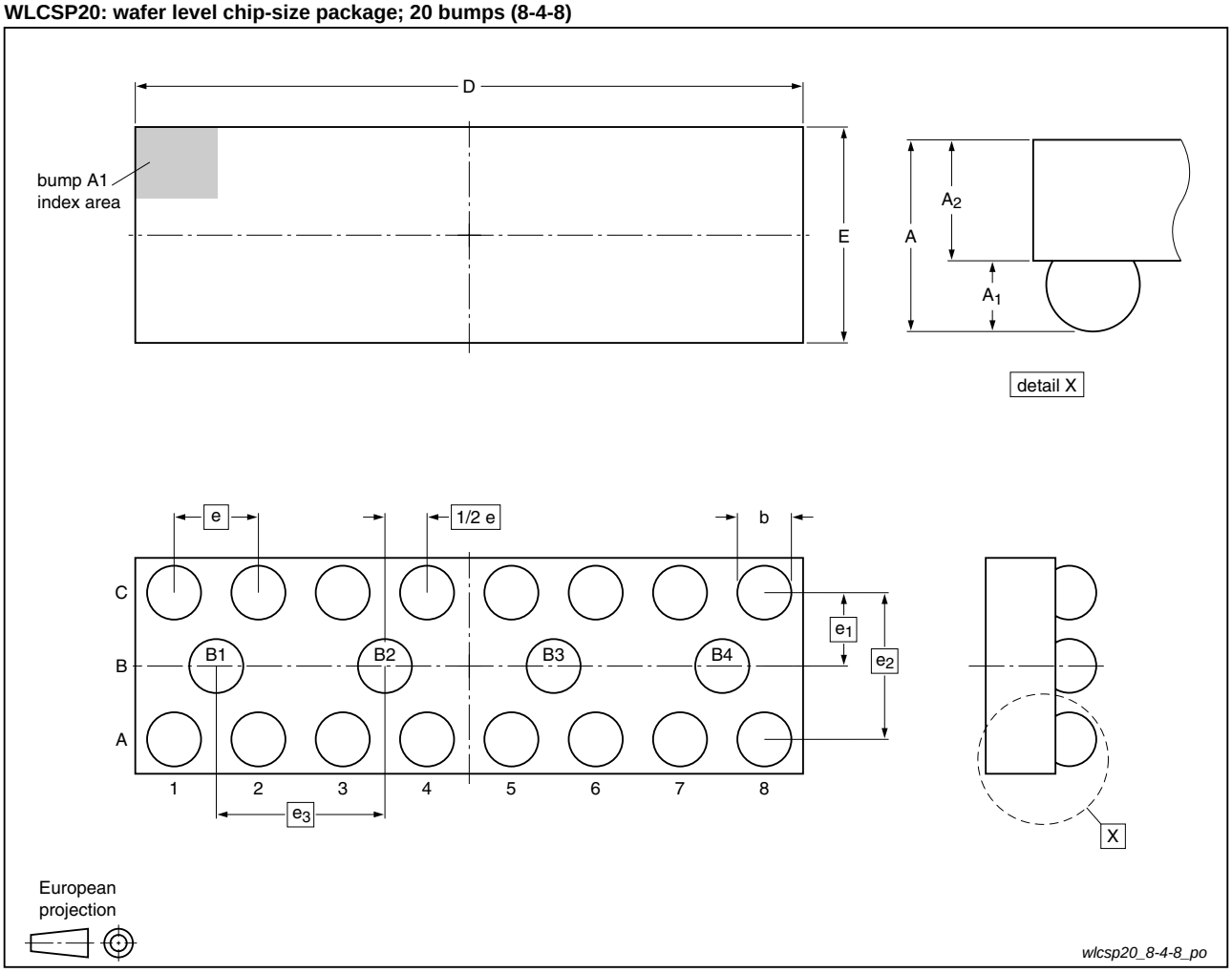


Fig 14. Package outline IP3348CX20 (WLCSP20)

Table 10. Dimensions for Figure 14

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	3.11	3.16	3.21	mm
E	1.01	1.06	1.11	mm
e	-	0.4	-	mm
e_1	-	0.346	-	mm
e_2	-	0.692	-	mm
e_3	-	0.8	-	mm

9. Design and assembly recommendations

9.1 PCB design guidelines

It is recommended, for optimum performance, to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 11 for the recommended PCB design parameters.

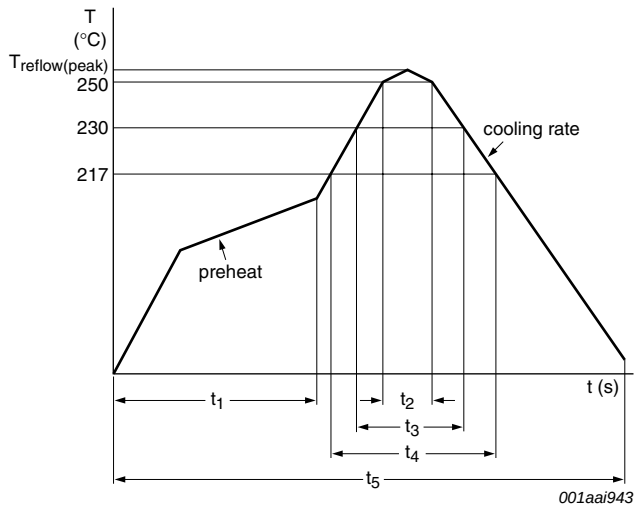
Table 11. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

9.2 PCB assembly guidelines for Pb-free soldering

Table 12. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	325 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 15



The device is capable of withstanding at least three reflows of this profile.

Fig 15. Pb-free solder reflow profile

Table 13. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

10. Abbreviations

Table 14. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
HS	High-Speed
LCD	Liquid Crystal Display
MDDI	Mobile Display Digital Interface
MIPI	Mobile Industry Processor Interface
NSMD	Non-Solder Mask Defined
NWA	NetWork Analyzer
PCB	Printed-Circuit Board
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3348CX5_CX10_CX15_CX20 v.1.1	20110404	Product data sheet	-	IP3348CX5_CX10_CX15_CX20 v.1
Modifications:	• Section 1.3: Changed MIDI to MIPI			
IP3348CX5_CX10_CX15_CX20 v.1	20101102	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contact information

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14. Contents

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