FEATURES

- World's most cost-effective 32-bit DSP featuring Dolby® Volume and Audistry® by Dolby
  - Supports native processing at input Fs up to 48kHz
  - Single download image enables support for 32 KHz, 44.1 kHz, and 48 kHz audio input
- CS48DV2B supports up to 2.0 channels of audio input and up to 2.1 channels of output
- Enables concurrent processing features beyond Dolby Volume including Tone Control, Multiband Parametric EQ, Bass Management, Delays.
- Configurable Serial Audio Inputs/Outputs
  - Configurable for all input/output digital audio types (I^2S/LJ/RJ)
  - 32-bit data path delivers uncompromised dynamic range
  - 192 kHz capable integrated S/PDIF transmitter
  - DAO can operate in master or slave mode (SCLK & LRCLK)
- Integrated Clock Manager/PLL
  - Capable of operating from a wide variety of external crystals or external oscillators
- Slave Host Boot Capability via Serial Interface
  - SPI™ interface capable of running up to 25 MHz during run time
- 1.8V Core and 3.3V I/O that is tolerant to 5V input
- Low-power Mode enabled
  - Energy Star® Design Compliance Capability via low-power mode, 268 µW in Standby mode

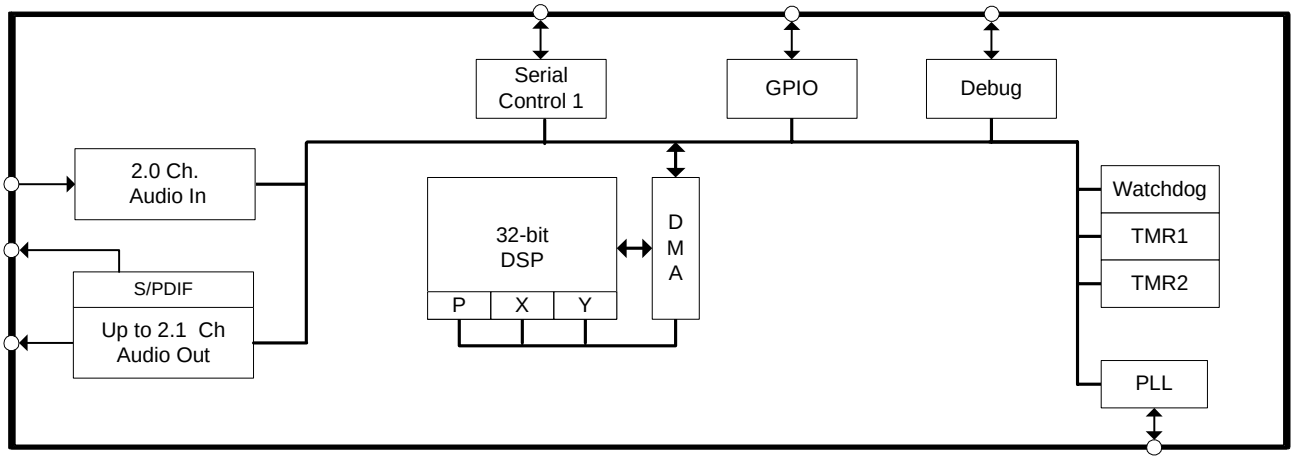
The new CS48DV2B supports a host of signal processing applications concurrently, including the mass production-ready Dolby Volume solution. See Section 3. for details about firmware concurrency on the CS48DV2B. The target applications for the CS48DV2B DSP are:

- Digital Televisions
- Soundbars / DTVs with Integrated Soundbars
- PMD/iPod® Docking Stations
- Automotive Head Units
- Automotive Outboard Amplifiers
- Blu-ray Disc® & DVD Receivers / HTiBs
- PC Speakers

All of these applications and many more that use volume control and are subject to playback from sources that do not have consistent volume levels will benefit from the CS48DV2B Dolby Volume solution.

Ordering Information:

See page 21 for ordering information.



Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**.

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1. Documentation Strategy

The *CS48DV2B Data Sheet* describes CS48DV2B multichannel audio processors. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS48DV2B processors.

Table 1. CS48DV2B DSP Related Documentation

Document Name	Description
CS48DV2B Data Sheet	This document
CS485xx Family Hardware User's Manual	Includes detailed system design information including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, etc.
AN298 - *CS485xx Family Firmware User's Manual*	Includes detailed firmware design information including signal processing flow diagrams and control API information
DSP Composer User's Manual	Includes detailed configuration and usage information for the GUI development tool.
AN298VPMA,*Audistry® by Dolby®"*	Describes API used to control the Audistry firmware module.
AN298PPMN, *Dolby® Volume Firmware User's Manual for the CS48DV2x Family*	Describes API used to control the Dolby Volume firmware module.

The scope of the *CS48DV2B Data Sheet* is primarily the hardware specifications of the CS48DV2B devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the *CS48DV2B Data Sheet* is the system PCB designer, MCU programmer, and the quality control engineer.

2. Overview

The CS48DV2B DSP is designed to provide high-performance post-processing and mixing of digital audio. The dual clock domain provided on the PCM inputs allows for the mixing of audio streams with different sampling frequencies. The low-power standby preserves battery life for applications which are always on, but not necessarily processing audio, such as automotive audio systems.

The CS48DV2B supports dual input clock domains and dual audio processing paths. The CS48DV2B is available in a 48-pin QFP package. Please refer to Table 2 on page 7 for the input, output, firmware features of each device.

2.1 Licensing

Licenses are required for all of the 3rd party audio processing algorithms listed in Section 3. Please contact your local Cirrus Logic Sales representative for more information.

3. Code Overlays

The suite of software available for the CS48DV2B DSP consists of an operating system (OS) and a library of overlays. The overlays have been divided into three main groups called Matrix-processors, Virtualizer-processors, and Post-processors. All software components are defined below:

1. **OS/Kernel** - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, error concealment, etc.
2. **Matrix-processor**- Any Module that performs a matrix decode on PCM data to produce more output channels than input channels (2⇨n channels). Examples are Dolby® Pro Logic® IIx and DTS Neo:6™. Generally speaking, these modules increase the number of valid channels in the audio I/O buffer.
3. **Virtualizer-processor** - Any module that encodes PCM data into fewer output channels than input channels (n⇨2 channels) with the effect of providing “phantom” speakers to represent the physical audio channels that were eliminated. Examples are Dolby Headphone® and Dolby® Virtual Speaker®. Generally speaking, these modules reduce the number of valid channels in the audio I/O buffer.
4. **Post-processors** - Any module that processes audio I/O buffer PCM data in-place after the matrix- or virtualizer-processors. Examples are the Dolby Volume and Audistry by Dolby firmware, bass management, audio manager, tone control, EQ, delay, and customer-specific effects

The bulk of each overlay is stored in ROM within the CS48DV2B, but a small image is required to configure the overlays and boot the DSP. This small image can either be stored in an external serial FLASH/EEPROM, or downloaded via a host controller through the SPI™/I^{2}C® serial port.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a new matrix-processor is selected, the OS, virtualizer-, and post-processors do not need to be reloaded — only the new matrix-processor. This fact is also true for the other overlays.

Table 2 lists the firmware available based on device selection. Please refer to AN298, *CS485xx Firmware User’s Manual* for the latest listing of application codes and Cirrus Framework™ modules available.

Table 2. Device and Firmware Selection Guide

Devices	Availability	Suggested Applications	Specific Features
CS48DV2B-CQZ CS48DV2B-DQZ	**In Production Now**	• Digital TV Portable Audio Docking Station • Portable DVD Players • Multimedia PC Speakers • Soundbars • Automotive Entertainment Systems	• 2.1 channels of audio input and 2.1 channels of PCM audio output. • 512 FFT Window, 20-Bands/Channel • Dolby Volume Native Processing of the following Fs: — 32 kHz — 44.1 kHz — 48 kHz

4. Hardware Functional Description

4.1 DSP Core

The CS48DV2B DSPs are single-core DSP with separate X and Y data and P code memory spaces. The DSP core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two multiply-and-accumulate (MAC) operations per clock cycle. The DSP core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

The DSP core is coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the serial control port (SCP), digital audio input (DAI) and digital audio output (DAO), or any DSP core memory, all without the intervention of the DSP. The DMA engine off loads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS48DV2B functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS48DV2B from a host controller or external serial FLASH/EEPROM.

Users can develop their applications using DSP Composer to create the processing chain and then compile the image into a series of commands that are sent to the CS48DV2B through the SCP. The processing application can either load modules (matrix-processors, virtualizers, post-processors) from the DSPs on-board ROM, or custom firmware can be downloaded through the SCP.

The CS48DV2B is suitable for a variety of audio post-processing applications such as automotive head-ends, automotive amplifiers, and boom boxes.

4.1.1 DSP Memory

The DSP core has its own on-chip data and program RAM and ROM and does not require external memory for post-processing applications.

The Y-RAM and P-RAM share a single block of memory that can be configured to make Y and P equal in size, or more memory can be allocated for Y-RAM in 2kword blocks.

4.1.2 DMA Controller

The powerful 8-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAMs/ROMs and the peripheral bus. Modulo and linear addressing

modes are supported, with flexible start address and increment controls. The service intervals for each DMA channel, as well as up to 6 interrupt events, are programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The DAI port supports a wide variety of data input formats at sample rates (Fs) as high as 192 kHz. The port is capable of accepting PCM or DSD formats. Up to 32-bit word lengths are supported. DSD is supported and internally converted to PCM before processing. The DAI also supports a time division multiplexed (TDM) one-line data mode that packs multiple channels of PCM audio input on a single data line. The total number of channels that are possible depends on the ratio of SCLK to LRCLK.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, off-loading the task of monitoring the S/PDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

DAO port supports PCM resolutions of up to 32-bits. The port supports sample rates (Fs) as high as 192 kHz. The port can be configured as an independent clock domain mastered by the DSP, or as a clock slave if an external MCLK or SCLK/LRCLK source is available. One of the serial audio pins can be re-configured as a S/PDIF transmitter that drives a bi-phase encoded S/PDIF signal (data with embedded clock on a single line).

The DAO also supports a time division multiplexed (TDM) one-line data mode, that packs multiple channels of PCM audio on a single data line.

4.2.3 Serial Control Port ($I^2C^{®}$ or SPI™)

The on-chip serial control port is capable of operating as master or slave in either SPI™ or $I^2C^{®}$ modes. Master/Slave operation is chosen by mode select pins when the CS48DV2B comes out of Reset. The serial clock pin can support frequencies as high as 25 MHz in SPI mode (SPI clock speed must always be ≤ (F_{dclk}/2)). The CS48DV2B serial control port also includes a pin for flow control of the communications interface ($\overline{\text{SCP\_BSY}}$) and a pin to indicate when the DSP has a message for the host ($\overline{\text{SCP\_IRQ}}$).

4.2.4 GPIO

Many of the CS48DV2B peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.5 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS48DV2B defaults to running from the external reference frequency and is switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.2.6 Hardware Watchdog Timer

The CS48DV2B has an integrated watchdog timer that acts as a “health” monitor for the DSP. The watchdog timer must be reset by the DSP before the counter expires, or the entire chip is reset. This peripheral ensures that the CS48DV2B will reset itself in the event of a temporary system failure. In stand-alone mode (that is, no host MCU), the DSP will reboot from external FLASH. In slave mode (that is, host MCU present) a GPIO will be used to signal the host that the watchdog has expired and the DSP should be rebooted and re-configured.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS48DV2B pins are multi-functional. For details on pin functionality please refer to the *CS485xx Hardware User’s Manual*.

4.3.2 Termination Requirements

Open-drain pins on the CS48DV2B must be pulled high for proper operation. Please refer to the *CS485xx Hardware User’s Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins in the CS48DV2B are used to select the boot mode upon the rising edge from reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS485xx Hardware User’s Manual*.

4.3.3 Pads

The CS48DV2B I/Os operate from the 3.3 V supply and are 5 V tolerant.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device. Please contact your local Cirrus representative for details.

5. Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, C_L = 20 pF, VDD = VDDA = 1.8 V, VDDIO = 3.3 V, GNDD = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0V)

Parameter	Symbol	Min	Max	Unit
DC power supplies: Core supply	VDD	-0.3	2.0	V
PLL supply	VDDA	-0.3	3.6	V
I/O supply	VDDIO	-0.3	3.6	V
|VDDA – VDDIO|		-	0.3	V
Input pin current, any pin except supplies	I_{in}	-	+/-10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on I/O pins	V_{inio}	-0.3	5.0	V
Storage temperature	T_{stg}	-65	150	°C

Caution: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies: Core supply	VDD	1.71	1.8	1.89	V
PLL supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
|VDDA – VDDIO|			0		V
Ambient operating temperature	T_A		-		°C
CS48DV2B-CQZ		0		+70	
CS48DV2B-DQZ		-40		+85	

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage, except XTI	V_{IL}	-	-	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	-	-	0.6	V
Input Hysteresis	V_{hys}		0.4		V
High-level output voltage (I_O = -2mA), except XTI	V_{OH}	VDDIO * 0.9	-	-	V
Low-level output voltage (I_O = 2mA), except XTI	V_{OL}	-	-	VDDIO * 0.1	V
Input leakage XTI	I_{LXTI}	-	-	5	µA
Input leakage current (all digital pins with internal pull-up resistors enabled)	I_{LEAK}	-	-	70	µA

5.4 Power Supply Characteristics

(Measurements performed under operating conditions)

Parameter	Min	Typ	Max	Unit
Operational Power Supply Current:				
VDD: Core and I/O operating[1]	-	203	-	mA
VDDA: PLL operating	-	8	-	mA
VDDIO: With most ports operating	-	27	-	mA
Total Operational Power Dissipation:		480		mW
Standby Power Supply Current:				
VDD: Core and I/O not clocked	-	100	-	µA
VDDA: PLL halted	-	1	-	µA
VDDIO: All connected I/O pins 3-stated by other ICs in system	-	50	-	µA
Total Standby Power Dissipation:	-	348	-	µW

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (48-Pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Junction Temperature	T_j	-	-	125	°C
Thermal Resistance (Junction to Ambient)					
Two-layer Board[1]	θ_{ja}	-	63.5	-	°C / Watt
Four-layer Board[2]		-	54	-	
Thermal Resistance (Junction to Top of Package)					
Two-layer Board[3]	ψ_{jt}	-	0.70	-	°C / Watt
Four-layer Board[4]		-	0.64	-	

1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20 % of the top & bottom layers.
2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20 % of the top & bottom layers and 0.5-oz. copper covering 90 % of the internal power plane & ground plane layers.
3. To calculate the die temperature for a given power dissipation

T_j = Ambient Temperature + [(Power Dissipation in Watts) * θ_{ja}]

4. To calculate the case temperature for a given power dissipation

$T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}]

5.6 Switching Characteristics— RESET

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low	T_{rstl}	1	-	ms
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	-	100	ns
Configuration pins setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	-	ns
Configuration pins hold after $\overline{\text{RESET}}$ high	T_{rsthld}	20	-	ns

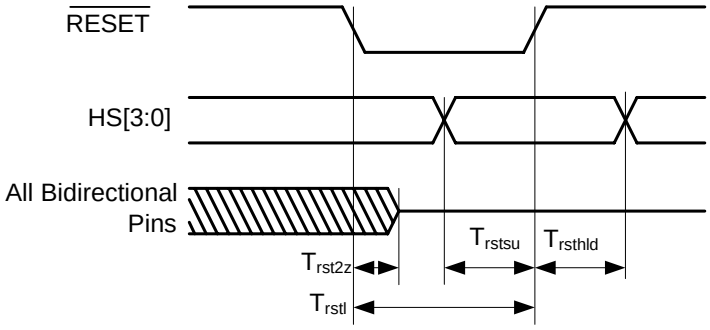


Figure 1. RESET Timing

5.7 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	11.2896	27	MHz
XTI period	T_{clki}	33.3	100	ns
XTI high time	T_{clkih}	13.3	-	ns
XTI low time	T_{clkil}	13.3	-	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR		50	Ω

1. Part characterized with the following crystal frequency values: 11.2896, 12.288, 18.432, 24.576, & 27 MH.z
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals that require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

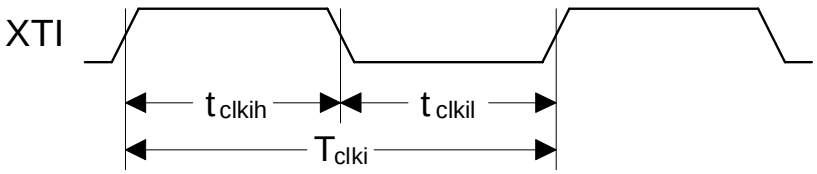


Figure 2. XTI Timing

5.8 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1]	F_{dclk}	-		MHz
CS48DV2B-CQZ		F_{xtal}	150	
CS48DV2B-DQZ		F_{xtal}	150	
Internal DCLK period[1]	DCLKP	-		ns
CS48DV2B-CQZ		6.7	$1/F_{xtal}$	
CS48DV2B-DQZ		6.7	$1/F_{xtal}$	

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kickstart commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode.

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		25	MHz
$\overline{\text{SCP\_CS}}$ falling to SCP_CLK rising	t_{spicss}	24		-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MOSI input	t_{spidsu}	5		-	ns
Hold time SCP_MOSI input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	-		11	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{spiirqh}$	-		20	ns
$\overline{\text{SCP\_CS}}$ rising to $\overline{\text{SCP\_IRQ}}$ falling	$t_{spiirql}$	0			ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising	t_{spicsh}	24		-	ns
$\overline{\text{SCP\_CS}}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	-	20		ns
SCP_CLK rising to $\overline{\text{SCP\_BSY}}$ falling	$t_{spicbsyl}$	-	3∗DCLKP+20		ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{xtal}/3$.

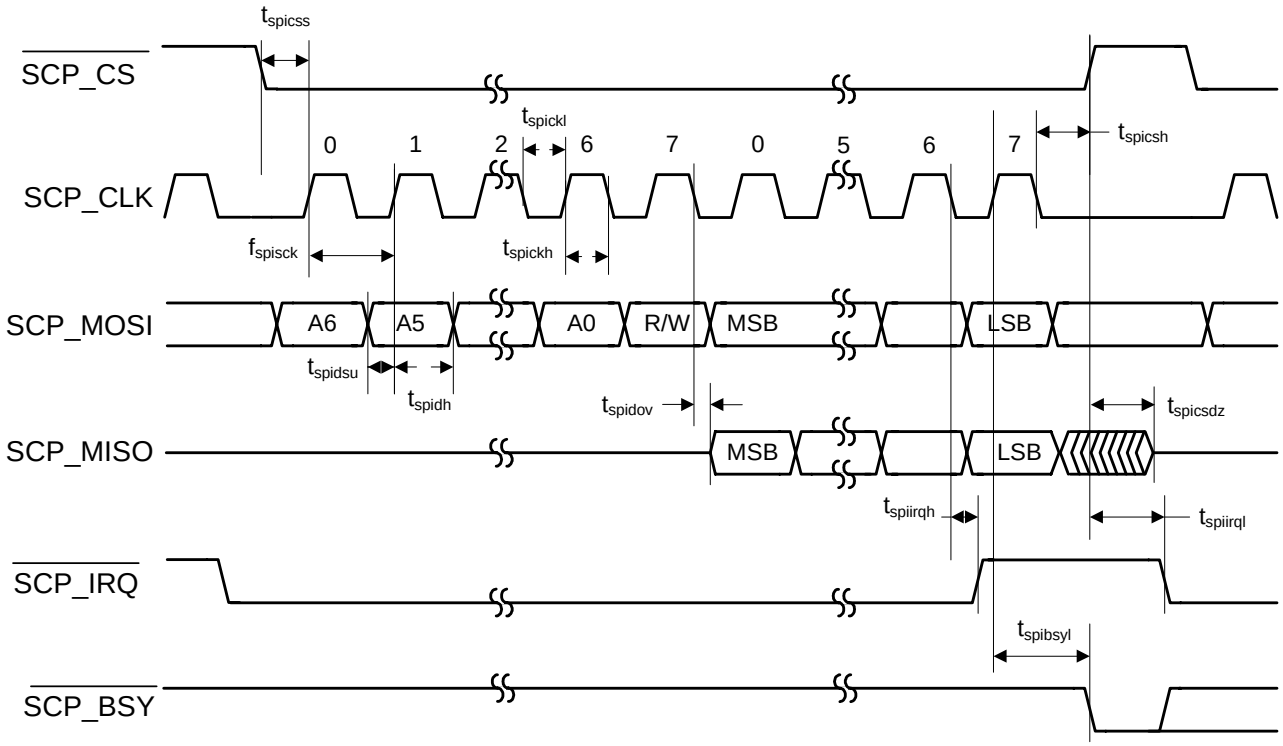


Figure 3. Serial Control Port - SPI Slave Mode Timing

5.10 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		$F_{xtal}/2^2$	MHz
$\overline{\text{SCP\_CS}}$ falling to SCP_CLK rising [3]	t_{spicss}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MISO input	t_{spidsu}	9		-	ns
Hold time SCP_MISO input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	-		8	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ falling	t_{spicsl}	7		-	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising	t_{spicsh}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
Bus free time between active SCP_CS	t_{spicsx}		3*DCLKP	-	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	-		20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.7.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter

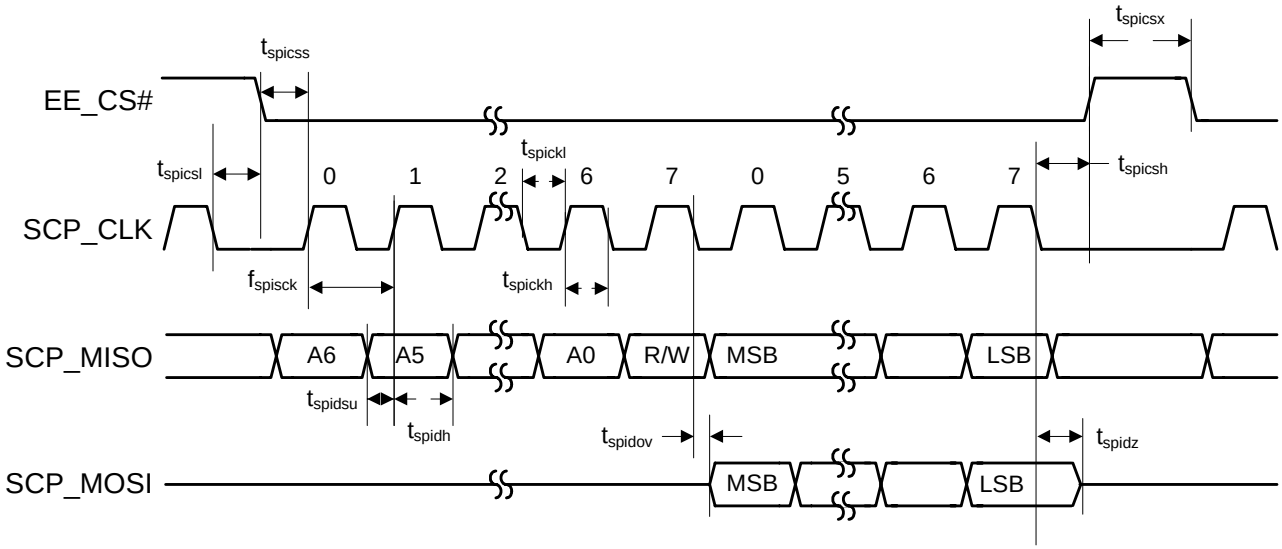


Figure 4. Serial Control Port - SPI Master Mode Timing

5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-		400	kHz
SCP_CLK low time	t_{iicckl}	1.25		-	µs
SCP_CLK high time	t_{iicckh}	1.25		-	µs
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25			µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25		-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5		-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3		-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100			ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20		-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-		18	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{iicirqh}$	-		3∗DCLKP + 40	ns
NAK condition to $\overline{\text{SCP\_IRQ}}$ low	$t_{iicirql}$		3∗DCLKP + 20		ns
SCP_CLK rising to $\overline{\text{SCB\_BSY}}$ low	$t_{iicbsyl}$	-	3∗DCLKP + 20		ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer.

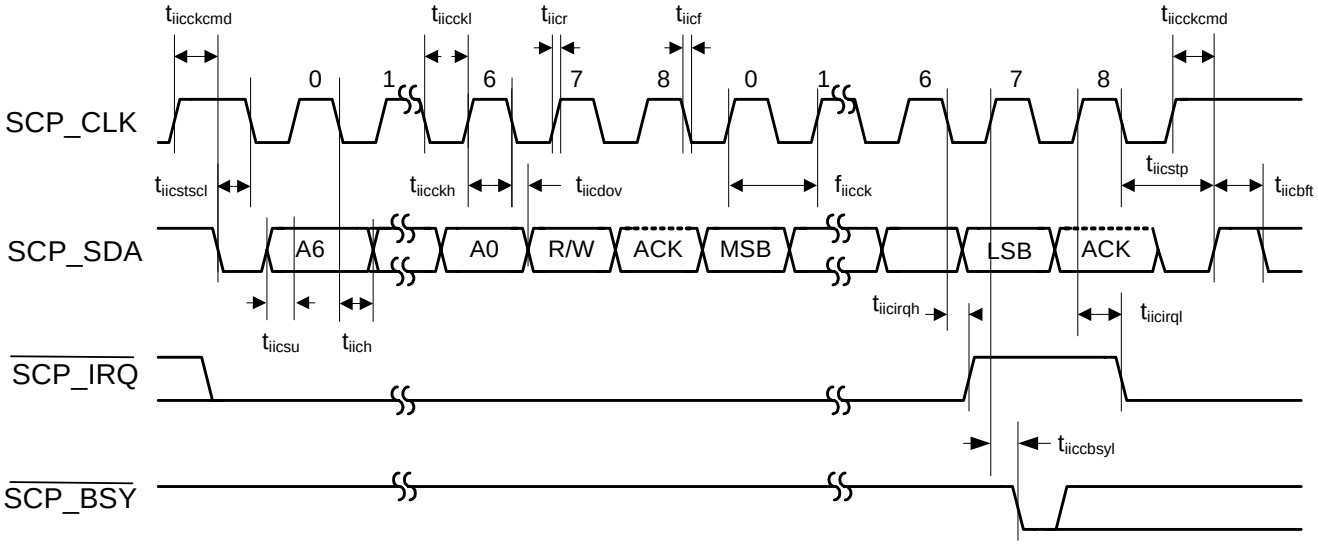


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	-	µs
SCP_CLK high time	t_{iicckh}	1.25	-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25		µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100		ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20	-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-	18	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.

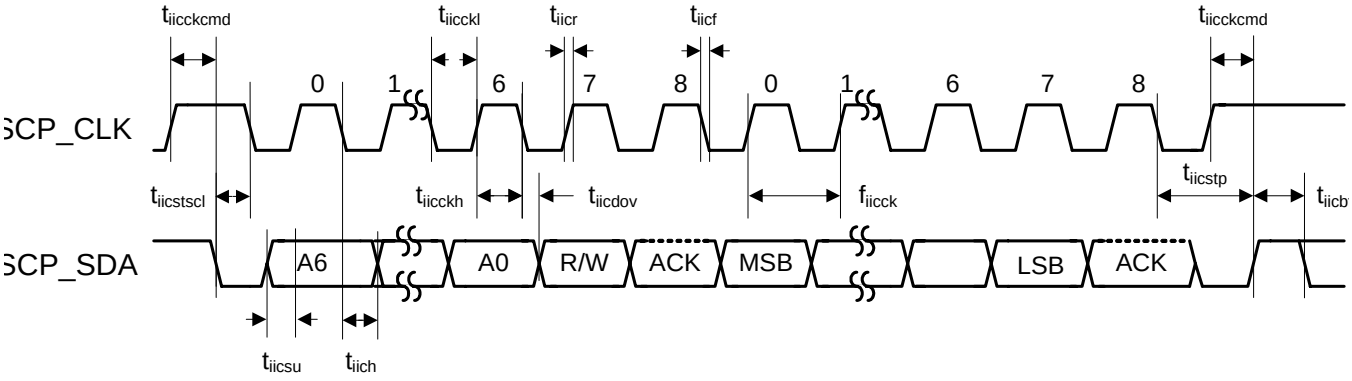


Figure 6. Serial Control Port - I²C Master Mode Timing

5.13 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	-	ns
DAI_SCLK duty cycle	-	45	55	%
Setup time DAI_DATAn	t_{daidsu}	10	-	ns
Hold time DAI_DATAn	t_{daidh}	5	-	ns

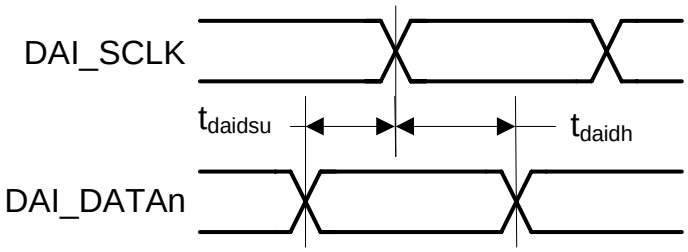


Figure 7. Digital Audio Input (DAI) Port Timing Diagram

5.14 Switching Characteristics — DSD Slave Input Port

Parameter	Symbol	Min	Typ	Max	Unit
DSD_SCLK Pulse Width Low	t_{sclkl}	78	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	78	-	-	ns
DSD_SCLK Frequency (64x Oversampled)	-	1.024	-	3.2	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns

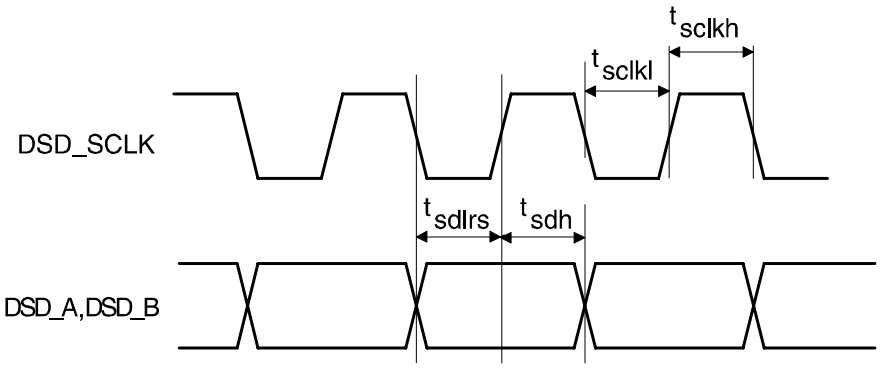
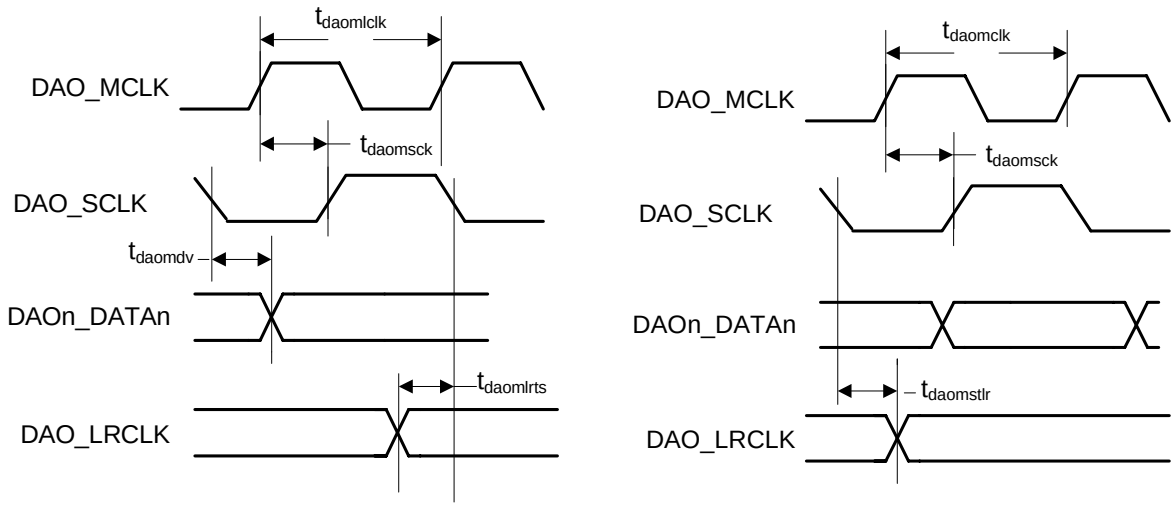


Figure 8. Direct Stream Digital - Serial Audio Input Timing

5.15 Switching Characteristics — Digital Audio Output Port

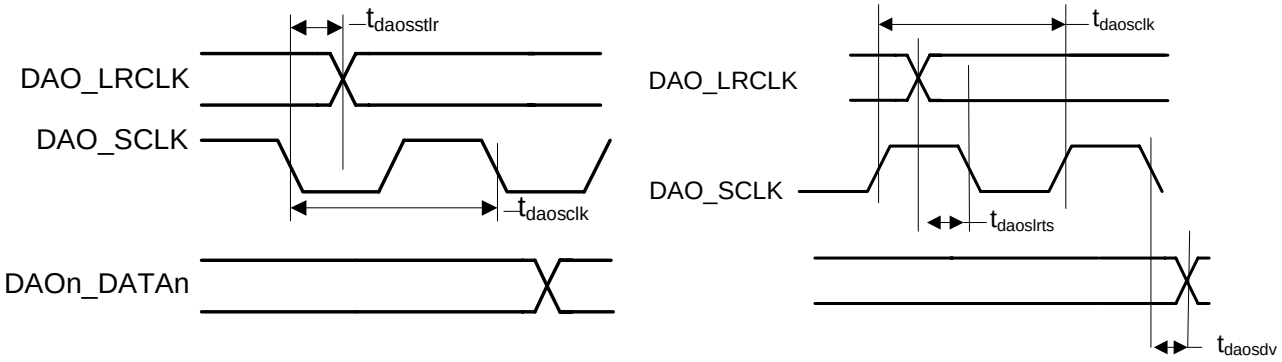
Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	-	ns
DAO_MCLK duty cycle	-	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	-	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	-	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	-	19	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[3]	$t_{daomstlr}$	-	8	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively[3]	$t_{daomlrts}$	-	8	ns
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daomdv}	-	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition[3]	t_{daosdv}	-	15	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[3]	$t_{daosstlr}$	-	30	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively[3]	$t_{daoslrts}$	-	15	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS48DVxx driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 9. Digital Audio Output Port Timing, Master Mode



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 10. Digital Audio Output Timing, Slave Mode (Relationship LRCLK to SCLK)

6. Ordering Information

The CS48DV2B part number is described as follows:

CS48DVNI-XYZR

where

N - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

R - Tape and Reel Packaging

Table 3. Ordering Information

Part No.	Grade	Temp. Range	Package
CS48DV2B-CQZ	Commercial	0 to +70 °C	48-pin LQFP
CS48DV2B-DQZ	Automotive	-40 to +85 °C	48-pin LQFP

NOTE: Please contact the factory for availability of the -D (automotive grade) package.

7. Environmental, Manufacturing, & Handling Information

Table 4. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS48DV2B-CQZ CS48DV2B-CQZR	260 °C	3	7 Days
CS48DV2B-DQZ CS48DV2B-DQZR			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. Device Pinout Diagrams

8.1 CS48DV2B, 48-pin LQFP Pinout Diagram

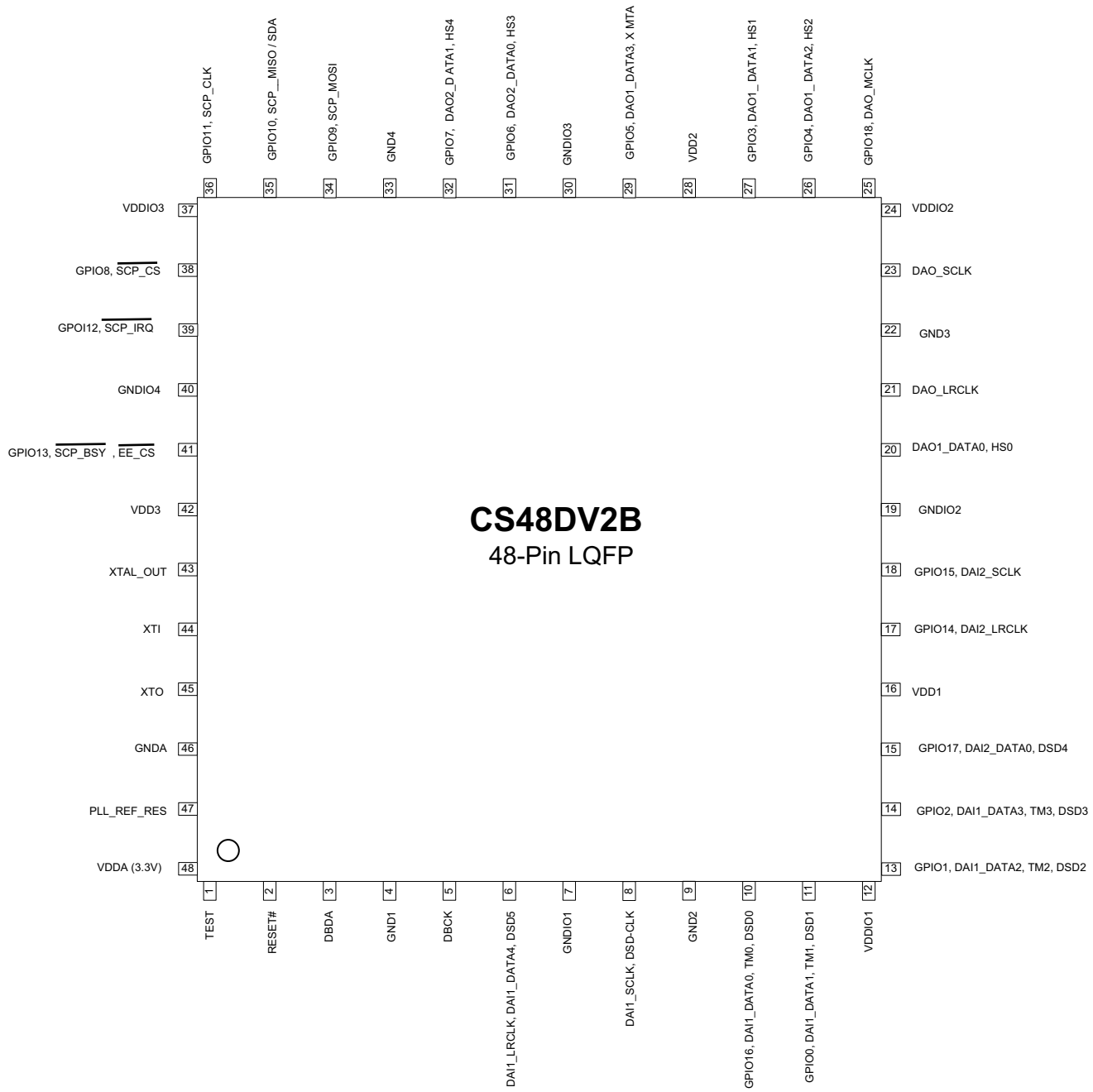
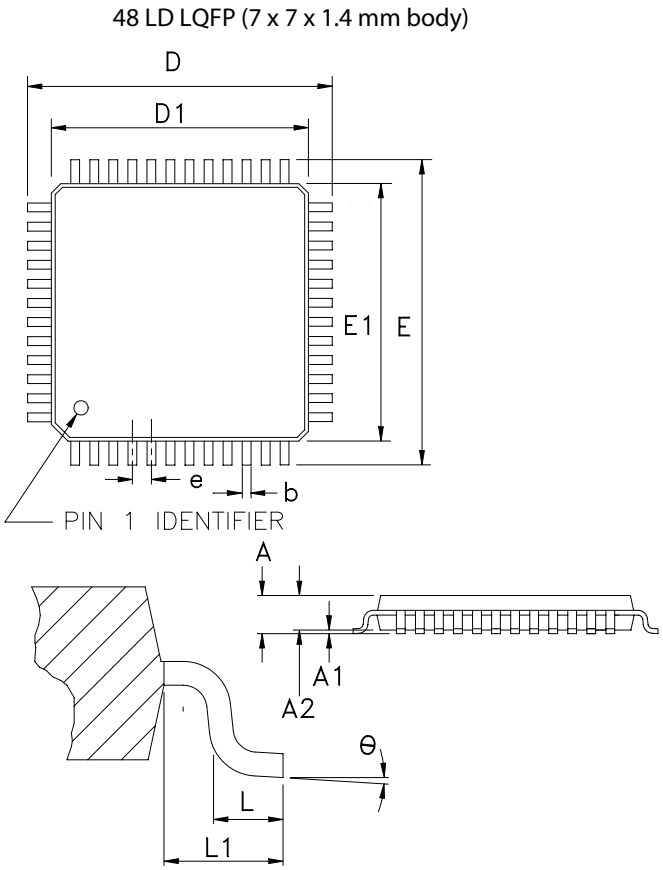


Figure 11. CS48DV2B 48-Pin LQFP Pinout Diagram

8.2 48-pin LQFP Package Drawing



	Number of Leads 48		
	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D		9.00 BSC	
D1		7.00 BSC	
e		0.50 BSC	
E		9.00 BSC	
E1		7.00 BSC	
theta	0		7
L	0.45	0.60	0.75
L1		1.00 REF	

NOTES:
1) Reference document: JEDEC MS-026
2) All dimensions are in millimeters and controlling dimension is in millimeters.
3) D1 and E1 do not include mold flash which is 0.25 mm max. per side.A1
4) Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.

Figure 12. 48-Pin LQFP Package Drawing

9. Revision History

Revision	Date	Changes
F1	December 3, 2008	Initial Release of *CS48DV2B Data Sheet*
F2	February 16, 2009	Updated Section 5.5, adding Junction Temperature specification.