

DSP320C10

CMOS Digital Signal Processor

The DSP320C10 is the first low power CMOS member of the Microchip Technology DSP320 family of digital signal processors, designed to support a wide range of high-speed or numeric-intensive applications. This device is a CMOS pin-for-pin compatible version of the industry standard DSP32010 digital signal processor.

The processor has been enhanced to make the Data RAM static with respect to the Reset. Also, the address hold time has been improved to a non-negative value.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SMD, QML, MIL-STD-883, /B and /R Flows

SMD/QML: Devices are processed per the applicable SMD flow and is fully compliant as such.

MIL-STD-883: Devices are tested 100% electrically at -55°C, +25°C and +125° per the applicable Manufacturer's part number datasheet or test program and processed per MIL-STD-883 and is fully compliant as such.

/B: Devices are processed to the Rochester Electronics military temperature process flow, which consists of 100% electrical testing to the Rochester Electronics datasheet at -55°C, +25°C and +125°C. Processing also includes 5004 screening and Groups A, B, C and D testing. All processing of MIL-STD-883 would be performed, but is non-compliant due to paragraph 1.2.1 for wafer fab documentation.

/R: Devices are processed to the Rochester Electronics military temperature process flow, which consists of 100% electrical testing to the Rochester Electronics datasheet at -55°C, +25°C and +125°C. Processing also includes 5004 screening and a Group A sample.



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DSP320C10

CMOS Digital Signal Processor

FEATURES

- 122ns instruction cycle
- 144 word on-chip data RAM
- ROM-less version — DSP320C10
- 1.5K word on-chip program ROM—DSP320CM10
- External memory expansion to a total of 4K words at full speed
- 16-bit instruction/data word
- 32-bit ALU/Accumulator
- 16 x 16-bit multiply in 122ns
- 0 to 15-bit barrel shifter
- Eight input and eight output channels
- 16-bit bidirectional data bus with a 65Mbps transfer rate
- Interrupt with a full context save
- Signed two's complement fixed-point arithmetic
- CMOS technology
- Single 5 volt supply
- Four versions available:
 - DSP320C10-14 14.4MHz Clock
 - DSP320C10 20.5MHz Clock
 - DSP320C10-25 25.6MHz Clock
 - DSP320C10-32 32.8MHz Clock

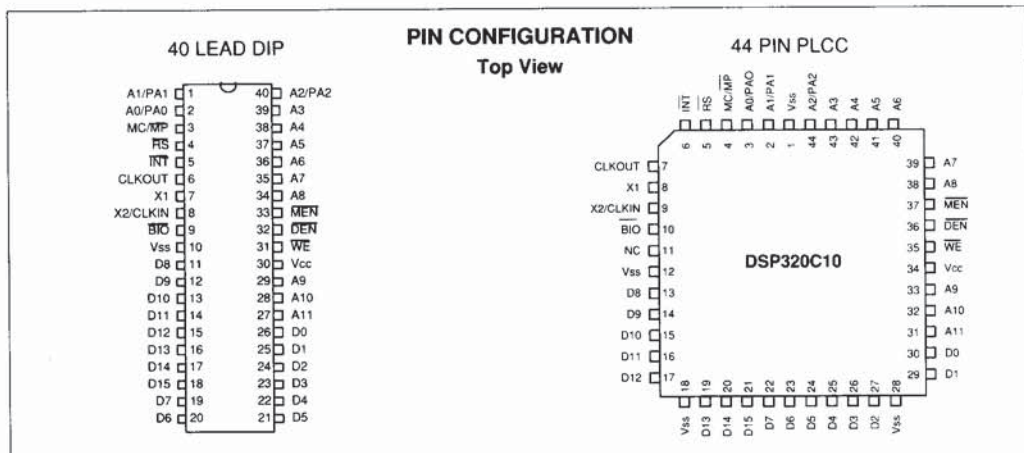
DESCRIPTION

The DSP320C10 is the first low power CMOS member of the Microchip Technology DSP320 family of digital signal processors, designed to support a wide range of high-speed or numeric-intensive applications. This device is a CMOS pin-for-pin compatible version of the industry standard DSP32010 digital signal processor.

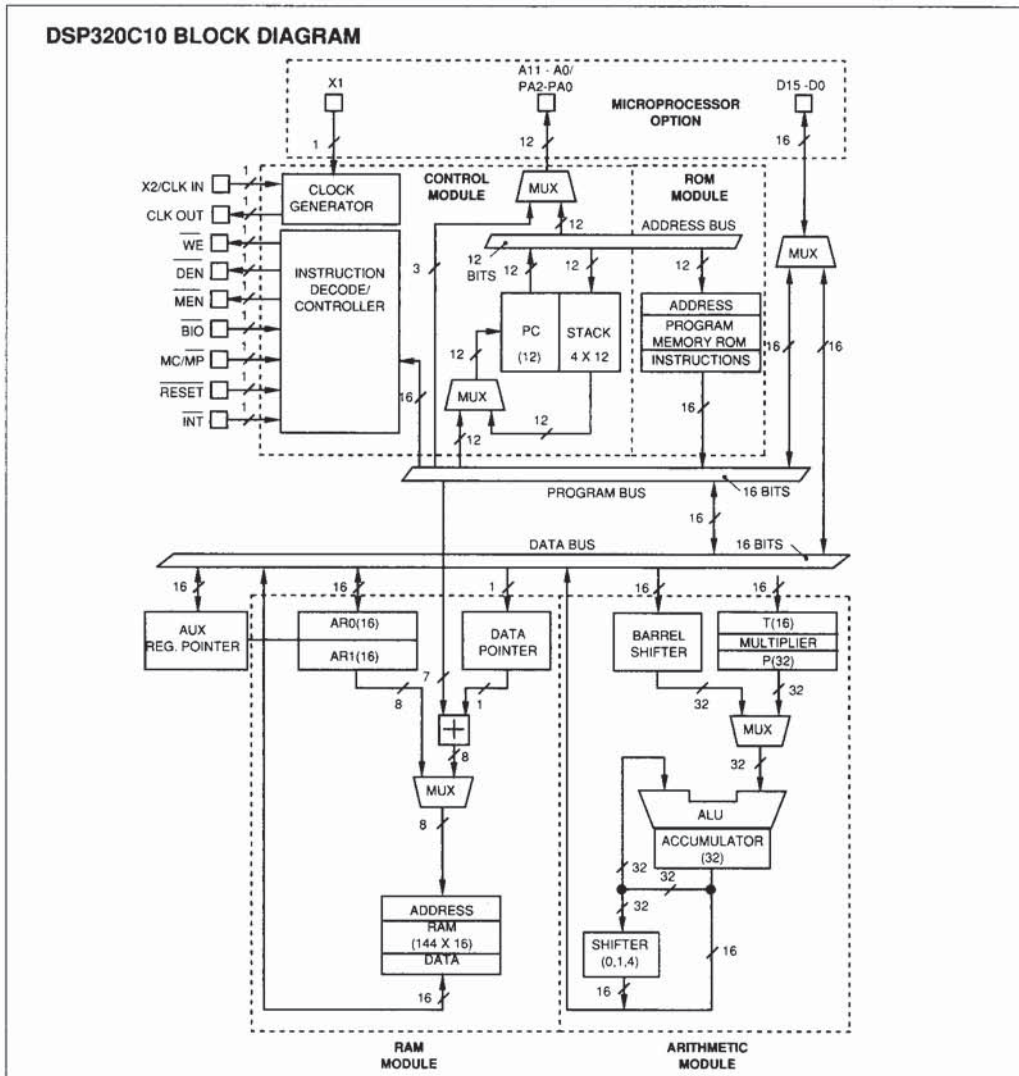
The processor has been enhanced to make the Data RAM static with respect to the Reset. Also, the address hold time has been improved to a non-negative value.

This 16/32 bit single-chip microcomputer combines the flexibility of a high-speed controller with the numerical capability of an array processor thereby offering an inexpensive alternative to multichip bit-slice processors. The DSP320 family contains MOS microcomputers capable of executing eight million instructions per second. This high throughput is the result of the comprehensive, efficient, and easily programmed instruction set and of the highly pipelined architecture. Special instructions have been incorporated to speed the execution of digital signal processing (DSP) algorithms.

The DSP320 family's unique versatility and power give the design engineer solutions to a variety of complicated applications. In addition, these microcomputers are capable of providing the multiple functions often required for a single application. For example, the DSP320 family can enable an industrial robot to synthesize and recognize speech, sense objects with radar or optical intelligence, and perform mechanical operations through digital servo loop computations.



DSP320C10



PIN DESCRIPTIONS

| Name | I/O | Definition | Name | I/O | Definition |
|--------------------|-----|---|----------|-----|--|
| A11-A0/ PA2-PA0 | OUT | External address bus. I/O port address multiplexed over PA2-PA0. | MC/MP | IN | Memory mode select: High selects microcomputer, low selects microprocessor mode. |
| BIO | IN | External polling input for bit test and jump operations. | MEN | OUT | Memory enable indicates that D15-D0 will accept external memory instruction. |
| CLKOUT | OUT | System clock output, 1/4 crystal CLKIN frequency. | RS | IN | Reset used to initialize device. |
| D15-D0 | I/O | 16-bit data bus. | VCC | IN | Power. |
| DEN | OUT | Data enable indicates the processor accepting input data on D15-D0. | VSS | IN | Ground. |
| INT | IN | Interrupt. | WE | OUT | Write enable indicates valid data on D15-D0. |
| | | | X1 | IN | Crystal input. |
| | | | X2/CLKIN | IN | Crystal input or external clock input. |

ARCHITECTURE

The DSP320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of the instruction fetch and execution. The DSP320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

The DSP320C10 utilizes hardware to implement functions that other processors typically perform in software. For example, this device contains a hardware multiplier to perform a multiplication in a single 122ns cycle. There is also a hardware barrel shifter for shifting data on its way into the ALU. Finally, extra hardware has been included so that auxiliary registers, which provide indirect data RAM addresses, can be configured in an auto increment/decrement mode for single-cycle manipulation of data tables. This hardware-intensive approach gives the design engineer the type of power previously unavailable on a single chip.

32-bit ALU/Accumulator

The DSP320C10 contains a 32-bit ALU and accumulator that support double-precision arithmetic. The ALU operates on 16-bit words taken from the data RAM or derived from immediate instructions. Besides the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.

Shifters

A barrel shifter is available for left-shifting data 0 to 15 places before it is loaded into, subtracted from, or added to the accumulator. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for two's complement arithmetic. A second shifter left-shifts the upper half of the accumulator 0, 1, or 4 places while it is being stored in the data RAM. Both shifters are very useful for scaling and bit extraction.

16 x 16-bit Parallel Multiplier

The DSP320C10's multiplier performs a 16 x 16-bit, two's complement multiplication in one 122ns instruction cycle. The 16-bit T Register temporarily stores the multiplicand; the P Register stores the 32-bit result. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the DSP320C10 to perform such fundamental operations as convolution, correlation, and filtering at a very high rate.

Program Memory Expansion

The DSP320C10 is equipped with a 1536-word ROM which can be mask-programmed at the factory with a customer's program. It can also execute from an additional 2560 words of off-chip program memory at full speed. This memory expansion capability is especially useful for those situations where a customer has a number of different applications that share the same subroutines. In this case, the common subroutines can be stored on-chip while the application specific code is stored off-chip.

The DSP 320C10 can operate in either of the following memory modes via the MC/MP pin:

Microcomputer Mode (MC)—Instruction addresses 0-1535 fetched from on-chip ROM. Those with addresses 1536-4095 fetched from off-chip memory at full speed.

Microprocessor Mode (MP)—Full speed execution from all 4096 off-chip instruction addresses.

The ability of the DSP320C10 to execute at full speed from off-chip memory provides important benefits:

- Easier prototyping and development work than is possible with a device that can address only on-chip ROM
- Purchase of a standard off-the-shelf product rather than a semi-custom mask-programmed device
- Ease of updating code
- Execution from external RAM
- Downloading of code from another microprocessor
- Use of off-chip RAM to expand data storage capability

Input/Output

The DSP320C10's 16-bit parallel data bus can be utilized to perform I/O functions at burst rates of 65 million bits per second. Available for interfacing to peripheral devices are 128 input and 128 output bits consisting of eight 16-bit multiplexed input ports and eight 16-bit multiplexed output ports. In addition, a polling input for bit test and jump operations (BIO) and an interrupt pin (INT) have been incorporated for multi-tasking.

Interrupts and Subroutines

The DSP320C10 contains a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the DSP320C10's complete context. The instructions, PUSH stack from accumulator, and POP stack to accumulator permit a level of nesting restricted only by the amount of available RAM. The interrupts used in the DSP320C10 are maskable.

DSP320C10

INSTRUCTION SET

The DSP320C10's comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general purpose operations, such as high-speed control. The instruction set, explained in Tables 1 and 2, consists primarily of single-cycle single-word instructions, permitting execution rates of up to eight million instructions per second. Only infrequently used branch and I/O instructions are multicycle.

The DSP320C10 also contains a number of instructions that shift data as part of an arithmetic operation. These all execute in a single cycle and are very useful for scaling data in parallel with other operations.

Three main addressing modes are available with the DSP320C10 instruction set: direct, indirect, and immediate addressing.

Direct Addressing

In direct addressing, seven bits of the instruction word concatenated with the data page pointer form the data memory address. This implements a paging scheme in which the first page contains 128 words and the second page contains 16 words. In a typical application, infrequently accessed variables, such as those used for servicing an interrupt, are stored on the second page. The instruction format for direct addressing is shown below.

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|---|---|---|-----|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OPCODE | | | | | | | | | DMA | | | | | | |

Bit 7 = 0 defines direct addressing mode. The opcode is contained in bits 15 through 8. Bits 6 through 0 contain data memory address.

The seven bits of the data memory address (DMA) field can directly address up to 128 words (1 page) of data memory. Use of the data memory page pointer is required to address the full 144 words of data memory.

Direct addressing can be used with all instructions requiring data operands except for the immediate operand instructions.

Indirect Addressing

Indirect addressing forms the data memory from the least significant eight bits of one of two auxiliary registers, AR0 and AR1. The auxiliary register pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. The instruction format for indirect addressing is as follows:

| | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| OPCODE | | | | | | | | 1 | 0 | I | D | N | A | 0 | 0 | A |
| | | | | | | | | | | N | E | A | R | | | R |
| | | | | | | | | | | C | C | R | | | | P |

Bit 7 = 1 defines indirect addressing mode. The opcode is contained in bits 15 through 8. Bits 7 through 0 contain indirect addressing control bits.

Bit 3 and bit 0 control the Auxiliary Register Pointer (ARP). If bit 3 = 0, then the content of bit 0 is loaded into the ARP. If bit 3 = 1, then content of ARP remain unchanged. ARP = 0 defines the contents of AR0 as memory address. ARP = 1 defines the contents of AR1 as memory address.

Bit 5 and bit 4 control the auxiliary registers. If bit 5 = 1, then the ARP defines which auxiliary register is to be incremented by 1. If bit 4 = 1, then the ARP defines which auxiliary register is to be decremented by 1. If bit 5 or bit 4 are zero, then neither auxiliary register is incremented or decremented. Bits 6, 2 and 1 are reserved and should always be programmed to zero.

Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

Immediate Addressing

The DSP320C10 instruction set contains special "immediate" instructions. These instructions derive data from part of the instruction word rather than from the data RAM. Some very useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

INSTRUCTION SET SUMMARY

| Symbol | Meaning |
|--------|---|
| ACC | Accumulator |
| D | Data memory address field |
| I | Addressing mode bit |
| K | Immediate operand field |
| PA | 3-bit port address field |
| R | 1-bit operand field specifying auxiliary register |
| S | 4-bit left-shift code |
| X | 3-bit accumulator left-shift field |

| Mnemonic | Description | Number of Cycles Words | | OpCode - Instruction Register | | | | | | | | | | | | | | | | | |
|----------|---|------------------------|---|-------------------------------|----|----|----|-------|-------|---|-------|-------|---------------|-------|---|---|---|---|---|---|--|
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| ABS | Absolute value of accumulator | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| ADD | Add to accumulator with shift | 1 | 1 | 0 | 0 | 0 | 0 | ← S → | | I | ← D → | | | | → | | | | | | |
| ADDH | Add to high-order accumulator bits | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | I | ← D → | | | | → | | | |
| ADDS | Add to accumulator with no sign extension | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | I | ← D → | | | | → | | | | |
| AND | AND with accumulator | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | I | ← D → | | | | → | | | | |
| LAC | Load accumulator with shift | 1 | 1 | 0 | 0 | 1 | 0 | ← S → | | I | ← D → | | | | → | | | | | | |
| LACK | Load accumulator immediate | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | ← K → | | | | → | | | | | |
| OR | OR with accumulator | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | I | ← D → | | | | → | | | | |
| SACH | Store high-order accumulator bits with shift | 1 | 1 | 0 | 1 | 0 | 1 | 1 | ← X → | | I | ← D → | | | | → | | | | | |
| SACL | Store low-order accumulator bits | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | I | ← D → | | | | → | | | | |
| SUB | Subtract from accumulator with shift | 1 | 1 | 0 | 0 | 0 | 1 | ← S → | | I | ← D → | | | | → | | | | | | |
| SUBC | Conditional subtract (for divide) | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | I | ← D → | | | | → | | | | |
| SUBH | Subtract from high-order | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | I | ← D → | | | | → | | | | |
| SUBS | Subtract from accumulator with no sign extension | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | I | ← D → | | | | → | | | | |
| XOR | Exclusive OR with accumulator | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | I | ← D → | | | | → | | | | |
| ZAC | Zero accumulator | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 0 0 1 0 0 1 | | | | → | | | | |
| ZALH | Zero accumulator and load high-order bits | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | I | ← D → | | | | → | | | | |
| ZALS | Zero accumulator and load low-order bits with no sign extension | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | I | ← D → | | | | → | | | | |

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INSTRUCTION SET SUMMARY (CONT.)

TABLE 2 (CONT.) - AUXILIARY REGISTER AND DATA PAGE POINTER INSTRUCTIONS

| Mne- monic | Description | Number of Cycles Words | | OpCode - Instruction Register | | | | | | | | | | | | | | | |
|---------------|---|---------------------------|---|-------------------------------|----|----|----|----|----|---|---|-----------------|-----------------|---|---|---|---|---|---|
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LAR | Load auxiliary register | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | R | I | ←----- D -----→ | | | | | | |
| LARK | Load auxiliary register immediate | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | R | ←----- K -----→ | | | | | | | |
| LARP | Load auxiliary register pointer immediate | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | K |
| LDP | Load data memory page pointer | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | I | ←----- D -----→ | | | | | | |
| LDPK | Load data memory page pointer immediate | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | K |
| MAR | Modify auxiliary register and pointer | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | I | ←----- D -----→ | | | | | | |
| SAR | Store auxiliary register | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | R | I | ←----- D -----→ | | | | | | |

TABLE 2 (CONT.) - BRANCH INSTRUCTIONS

| Mne- monic | Description | Number of Cycles Words | | OpCode - Instruction Register | | | | | | | | | | | | | | | |
|---------------|---|---------------------------|---|-------------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| B | Branch unconditionally | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BANZ | Branch on auxiliary register not zero | 2 | 2 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BGEZ | Branch if accumulator ≥ 0 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BGZ | Branch if accumulator > 0 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BIOZ | Branch on $\overline{\text{BIO}} = 0$ | 2 | 2 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BLEZ | Branch if accumulator ≤ 0 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BLZ | Branch if accumulator < 0 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BNZ | Branch if accumulator ≠ 0 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BV | Branch on overflow | 2 | 2 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| BZ | Branch if accumulator = 0 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| CALA | Call subroutine from accumulator | 2 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| CALL | Call subroutine immediately | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | ←----- BRANCH ADDRESS -----→ | | | | | | | | | | | | | | | |
| RET | Return from subroutine or interrupt routine | 2 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

INSTRUCTION SET SUMMARY (CONT.)

| TABLE 2 (CONT.) - T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS | | | | | | | | | | | | | | | | | | | | |
|---|---|------------------------|---|-------------------------------|----|----|-------|----|----|---|---|---|-------|---|---|---|---|---|---|---|
| Mnemonic | Description | Number of Cycles Words | | OpCode - Instruction Register | | | | | | | | | | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| APAC | Add P register to accumulator | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| LT | Load T register | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | ← D → | | | | | | | |
| LTA | LTA combines LT and APAC into one instruction | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | ← D → | | | | | | | |
| LTD | LTD combines LT, APAC, and DMOV into one instruction | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | ← D → | | | | | | | |
| MPY | Multiply with T register, store product in P register | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | ← D → | | | | | | | |
| MPYK | Multiply T register with immediate operand; store product in P register | 1 | 1 | 1 | 0 | 0 | ← K → | | | | | | | | | | | | | |
| PAC | Load accumulator from P register | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| SPAC | Subtract P register from accumulator | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| TABLE 2 (CONT.) - CONTROL INSTRUCTIONS | | | | | | | | | | | | | | | | | | | | |
|--|-----------------------------|------------------------|---|-------------------------------|----|----|----|----|----|---|---|---|-------|---|---|---|---|---|---|---|
| Mnemonic | Description | Number of Cycles Words | | OpCode - Instruction Register | | | | | | | | | | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| DINT | Disable interrupt | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| EINT | Enable interrupt | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| LST | Load status register | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | ← D → | | | | | | | |
| NOP | No operation | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| POP | POP stack to accumulator | 2 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| PUSH | PUSH stack from accumulator | 2 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| ROVM | Reset overflow mode | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| SOVM | Set overflow mode | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| SST | Store status register | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | ← D → | | | | | | | |

| TABLE 2 (CONT.) - I/O AND DATA MEMORY OPERATIONS | | | | | | | | | | | | | | | | | | | | |
|--|--|------------------------|---|-------------------------------|----|----|----|----|--------|---|-------|---|-------|---|---|---|---|---|---|--|
| Mnemonic | Description | Number of Cycles Words | | OpCode - Instruction Register | | | | | | | | | | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| DMOV | Copy contents of data memory | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | ← D → | | | | | | | |
| IN | Input data from port | 2 | 1 | 0 | 1 | 0 | 0 | 0 | ← PA → | | ← D → | | | | | | | | | |
| OUT | Output data to port | 2 | 1 | 0 | 1 | 0 | 0 | 1 | ← PA → | | ← D → | | | | | | | | | |
| TBLR | Table read from program memory to data RAM | 3 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | ← D → | | | | | | | |
| TBLW | Table write from data RAM to program (external only) | 3 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | ← D → | | | | | | | |

DSP320C10

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Over specified temperature range (unless otherwise noted)**

Supply voltage, V_{CC} -0.3V to 7V
 All input voltages -0.3V to 7V
 Output voltage -0.3V to 7V

Continuous power dissipation:

DSP320C10 (0° to +70°C) 0.3W
 DSP320C10I (-40° to +85°C) 0.36W
 DSP320C10-25 (0° to +70°C) 0.35W
 DSP320C10I-25 (-40° to +85°C) 0.4W

Air temperature range above operating device:

- Commercial 0° C to 70° C
 - Industrial -40° C to 85° C
 Storage Temperature Range -55° C to 150° C
 Junction Temperature (TJ) 165° C

**Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

| DC CHARACTERISTICS | | | | | | | | | | | | | * $V_{CC} = 5V$, $T_A = 25^\circ C$ | |
|--|--------------|------|----------|--------------|------|----------|--------------|------|----------|--------------|------|----------|--------------------------------------|---|
| Characteristics | DSP320C10 | | | DSP320C10-14 | | | DSP320C10-25 | | | DSP320C10-32 | | | Unit | Conditions |
| | Min | Nom* | Max | Min | Nom* | Max | Min | Nom* | Max | Min | Nom* | Max | | |
| Supply voltage, V_{CC} | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V | |
| Supply voltage, V_{SS} | — | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | V | |
| High-level input voltage, V_{IH} - All inputs except CLKIN - CLKIN | 2.0 | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | — | — | V | |
| | 65 V_{CC} | — | — | 65 V_{CC} | — | — | 65 V_{CC} | — | — | 65 V_{CC} | — | — | V | |
| Low-level input voltage, V_{IL} (all inputs) | — | — | 0.8 | — | — | 0.8 | — | — | 0.8 | — | — | 0.8 | V | |
| High-level output voltage V_{OH} | $V_{CC} - 4$ | — | — | $V_{CC} - 4$ | — | — | $V_{CC} - 4$ | — | — | $V_{CC} - 4$ | — | — | V | $I_{OH} = 20\mu A$ |
| | 2.4 | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | — | — | V | $I_{OH} = 300\mu A$ |
| Low-level output voltage, V_{OL} | — | — | 0.4 | — | — | 0.4 | — | — | 0.4 | — | — | 0.4 | V | $I_{OL} = 2mA$ |
| Off-state output current, I_{OZ} | — | — | 20 | — | — | 20 | — | — | 20 | — | — | 20 | μA | $V_{CC} = 5.5V$ $V_O = V_{CC} - .4V$ |
| | — | — | -20 | — | — | -20 | — | — | -20 | — | — | -20 | μA | |
| Input current, I_i | — | — | ± 50 | — | — | ± 50 | — | — | ± 50 | — | — | ± 50 | μA | |
| Supply current, I_{CC} (tested w/clocks running & part in reset) | — | — | 50 | — | — | 50 | — | — | 55 | — | — | 65 | mA | $V_{CC} = 5.5V$ |
| Input capacitance, C_i - Data bus - All others | — | 25 | — | — | 25 | — | — | 25 | — | — | 25 | — | pF | f = 1MHz, all other pins 0V |
| | — | 15 | — | — | 15 | — | — | 15 | — | — | 15 | — | pF | |
| Output capacitance, C_o - Data bus - All others | — | 25 | — | — | 25 | — | — | 25 | — | — | 25 | — | pF | |
| | — | 10 | — | — | 10 | — | — | 10 | — | — | 10 | — | pF | |

PARAMETER MEASUREMENT INFORMATION

FIGURE 2 - TEST LOAD CIRCUIT

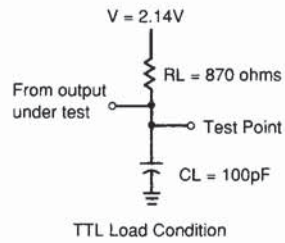


FIGURE 3 - AC TIMING VOLTAGE REFERENCE LEVELS



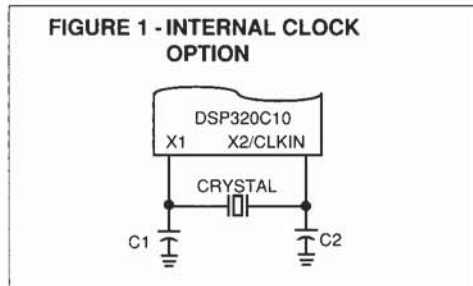
DSP320C10

CLOCK

The DSP320C10 can use either its internal oscillator or an external frequency source for a clock.

INTERNAL CLOCK OPTION

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (See Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency.



The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1mW, and be specified at a load capacitance of 20pF.

EXTERNAL CLOCK OPTION

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected.

The external frequency injected must conform to the specifications listed in the table below.

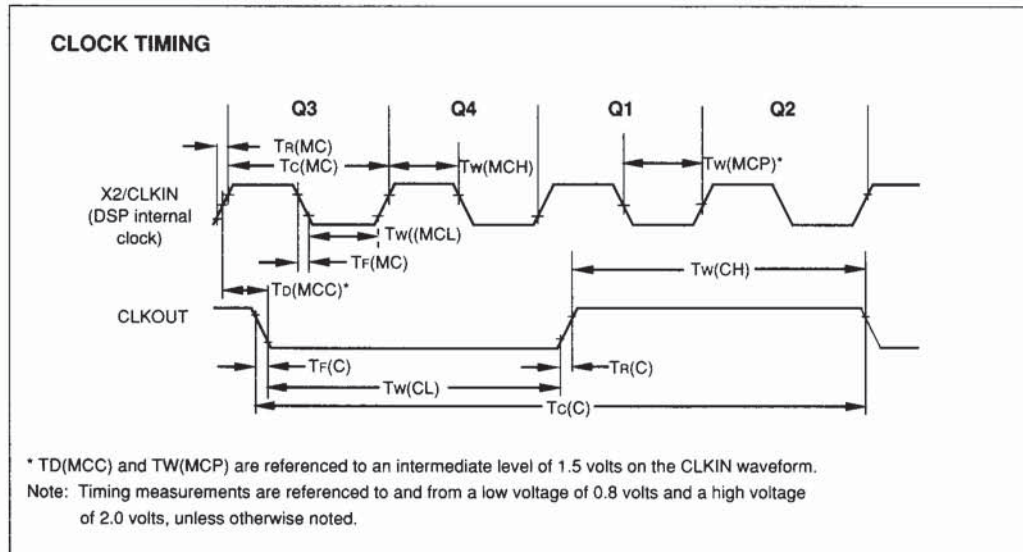
| CLOCK FREQUENCIES | | | | | | |
|--------------------------------|-----|-----|-----|------|------|------------------------------|
| Characteristics | Sym | Min | Nom | Max | Unit | Temperature Range Conditions |
| DSP320C10 Crystal frequency | fx | 6.7 | — | 20.5 | MHz | I, C |
| DSP320C10-14 Crystal frequency | fx | 6.7 | — | 14.4 | MHz | I, C |
| DSP320C10-25 Crystal frequency | fx | 6.7 | — | 25.6 | MHz | I, C |
| DSP320C10-32 Crystal frequency | fx | 6.7 | — | 32.8 | MHz | I, C |
| C1,C2 | — | — | 10 | — | pf | I, C |

DSP320C10

CLOCK (CONT.)

| CLOCK AC CHARACTERISTICS | | | | | | | | | | | | | TA (Commercial) = 0° to 70° C TA (Industrial) = -40° to 85° C VCC = 5V + 10%, VSS = 0V | | |
|---|---------|-----------|-----|-----------|--------------|-----|-----------|--------------|-----|------------|--------------|-----|--|------|------------|
| Timing requirements/Switching Characteristics over Recommended Operating Conditions | | | | | | | | | | | | | | | |
| Characteristics | Sym | DSP320C10 | | | DSP320C10-14 | | | DSP320C10-25 | | | DSP320C10-32 | | | Unit | Conditions |
| | | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | | |
| Master clk cycle time | Tc(MC) | 48.78 | — | 150 | 69.50 | — | 150 | 39 | — | 150 | 30.5 | — | 150 | ns | Note 1 |
| Rise time mast. clk in. | Tr(MC) | — | 5 | 10* | — | 5 | 10* | — | 4 | 8* | — | 3 | 6* | ns | |
| Fall time mast. clk in. | Tf(MC) | — | 5 | 10* | — | 5 | 10* | — | 4 | 8* | — | 3 | 6* | ns | |
| Pulse dur. mast. clk low, Tc(MC) = 70ns | Tw(MCL) | 14* | 20 | — | 14* | 20 | — | 12* | 16 | — | 8* | 12 | — | ns | |
| Pulse dur. mast. clk high, Tc(MC) = 70ns | Tw(MCH) | 14* | 20 | — | 14* | 20 | — | 12* | 16 | — | 8* | 12 | — | ns | |
| Pulse dur. mast. clk | Tw(MCP) | 0.4Tc(C)* | — | 0.6Tc(C)* | 0.4Tc(C)* | — | 0.6Tc(C)* | 0.45Tc(C)* | — | 0.55Tc(C)* | 0.45Tc(C)* | — | 0.55Tc(C)* | ns | |
| CLKOUT cycle time | Tc(C) | 195.12 | — | — | 277.80 | — | — | 156 | — | — | 122 | — | — | ns | See Fig 2 |
| CLKOUT rise time | Tr(C) | — | 10 | — | — | 10 | — | — | 10 | — | — | 4 | — | ns | |
| CLKOUT fall time | Tf(C) | — | 8 | — | — | 8 | — | — | 8 | — | — | 7 | — | ns | |
| Pls. dur., CLKOUT low | Tw(CL) | — | 92 | — | — | 131 | — | — | 74 | — | — | 57 | — | ns | |
| Pls. dur., CLKOUT high | Tw(CH) | — | 90 | — | — | 129 | — | — | 72 | — | — | 54 | — | ns | |
| Delay time to CLKIN↑ to CLKOUT↓ (Note 2) | Td(MCC) | 10 | — | 60 | 10 | — | 60 | 10 | — | 50 | 10 | — | 50 | ns | |

Note: (1) Tc(C) is the cycle time of CLKOUT. i.e., 4*Tc(MC) (4 times CLKIN cycle time if an external oscillator is used)
(2) * These values were derived from characterization data and are not tested or guaranteed.



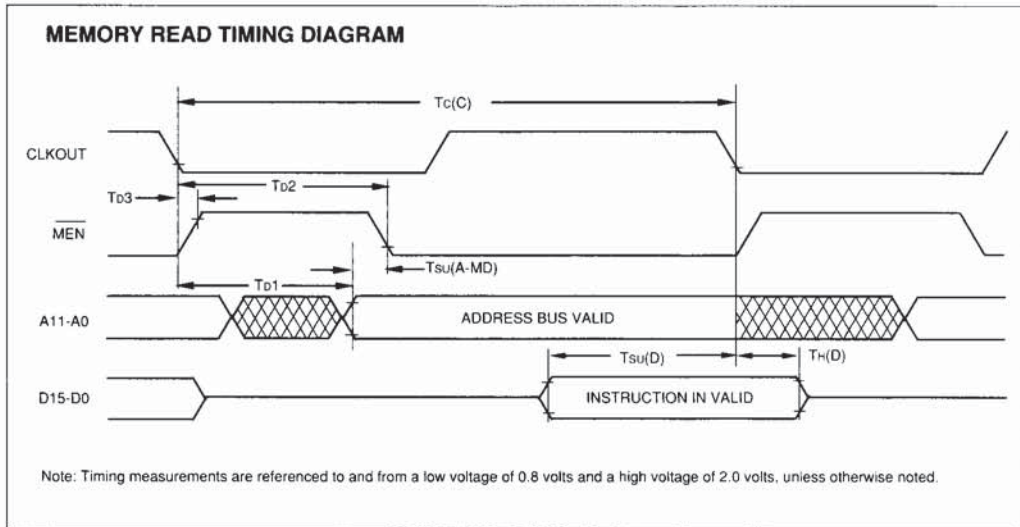
DSP320C10

MEMORY AND PERIPHERAL INTERFACE TIMING

| MEMORY AND PERIPHERAL INTERFACE - AC CHARACTERISTICS | | | | | | |
|---|-----------------------|----------------------------|-----|-----------------------------|------|--------------|
| Over recommended operating conditions | | | | | | |
| Characteristics | Sym | Min | Typ | Max | Unit | Conditions |
| Delay time CLKOUT↓ to address bus valid (see note) | T _{d1} | 10* | — | 38 | ns | See Figure 2 |
| Delay time CLKOUT↓ to $\overline{\text{MEN}}\downarrow$ | T _{d2} | 1/4T _c (C) - 5* | — | 1/4T _c (C) + 12 | ns | |
| Delay time CLKOUT↓ to $\overline{\text{MEN}}\uparrow$ | T _{d3} | -8* | — | 12 | ns | |
| Delay time CLKOUT↓ to $\overline{\text{DEN}}\downarrow$ | T _{d4} | 1/4T _c (C) - 5* | — | 1/4T _c (C) + 12 | ns | |
| Delay time CLKOUT↓ to $\overline{\text{DEN}}\uparrow$ | T _{d5} | -8* | — | 12 | ns | |
| Delay time CLKOUT↓ to $\overline{\text{WE}}\downarrow$ | T _{d6} | 1/2T _c (C) - 5* | — | 1/2T _c (C) + 12 | ns | |
| Delay time CLKOUT↓ to $\overline{\text{WE}}\uparrow$ | T _{d7} | -8* | — | 12 | ns | |
| Delay time CLKOUT↓ to data bus OUT valid | T _{d8} | — | — | 1/4T _c (C) + 40 | ns | |
| Time after CLKOUT↓ that data bus starts to be driven | T _{d9} | 1/4T _c (C) - 5* | — | — | ns | |
| Time after CLKOUT↓ that data bus stops being driven | T _{d10} | — | — | 1/4T _c (C) + 30* | ns | |
| Data bus OUT valid after CLKOUT↓ | T _v | 1/4T _c (C) - 10 | — | — | ns | |
| Delay time $\overline{\text{DEN}}\uparrow$, $\overline{\text{MEN}}\uparrow$ and $\overline{\text{WE}}\uparrow$ from $\overline{\text{RS}}\downarrow$ | T _{d11} | — | — | T _c (C) + 50* | ns | |
| Setup time data bus valid prior to CLKOUT↓ | T _{su(D)} | 38 | — | — | ns | |
| Hold time data bus held valid after CLKOUT↓ | T _{h(D)} | 0 | — | — | ns | |
| Address bus setup time prior to $\overline{\text{MEN}}\downarrow$ or $\overline{\text{DEN}}\downarrow$ | T _{su(A-MD)} | 1/4T _c (C) - 35 | — | — | ns | |
| Address bus hold after $\overline{\text{WE}}\uparrow$, $\overline{\text{MEN}}\uparrow$ or $\overline{\text{DEN}}\uparrow$ | T _{h(A-WMD)} | 5 | — | — | ns | |
| Address bus setup time prior to $\overline{\text{WE}}\downarrow$ | T _{su(A-WE)} | 1/2T _c (C) - 34 | — | — | ns | |
| Data bus setup time prior to $\overline{\text{WE}}\downarrow$ | T _{su(D-WE)} | 1/4T _c (C) - 32 | — | — | ns | |
| Data bus hold after $\overline{\text{WE}}\uparrow$ | T _{h(D-WE)} | 1/4T _c (C) - 18 | — | — | ns | |
| External memory access time | T _{acc} | — | — | T _c (C) - 69 | ns | |
| External memory output enable time | T _{oe} | — | — | 3/4 T _c (C) - 40 | ns | |

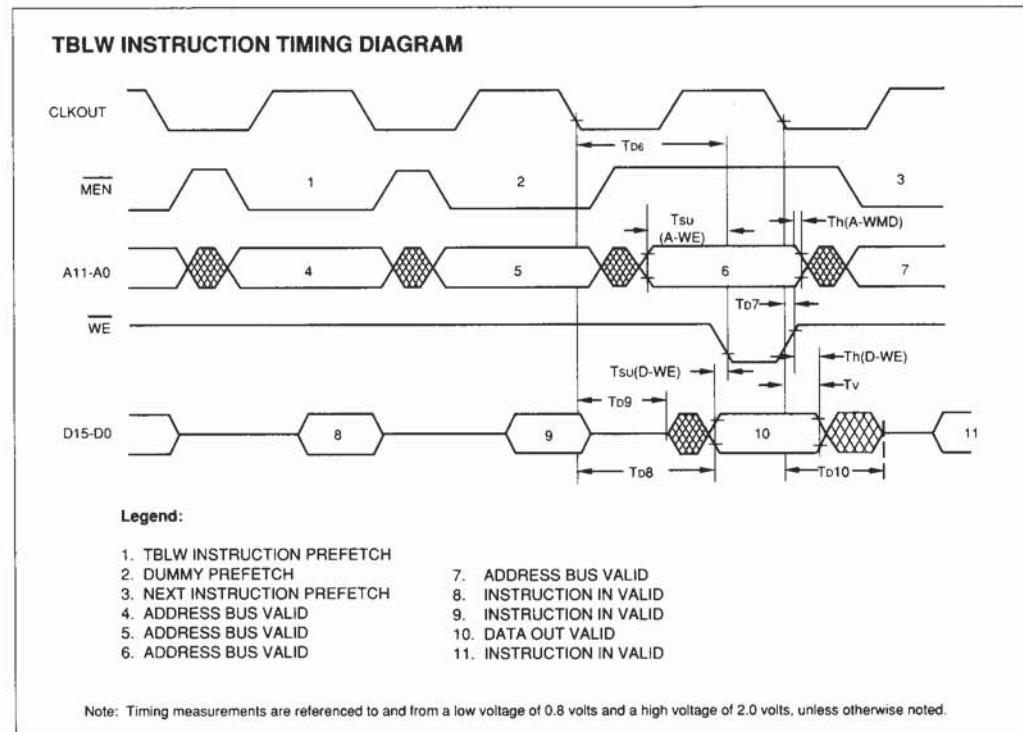
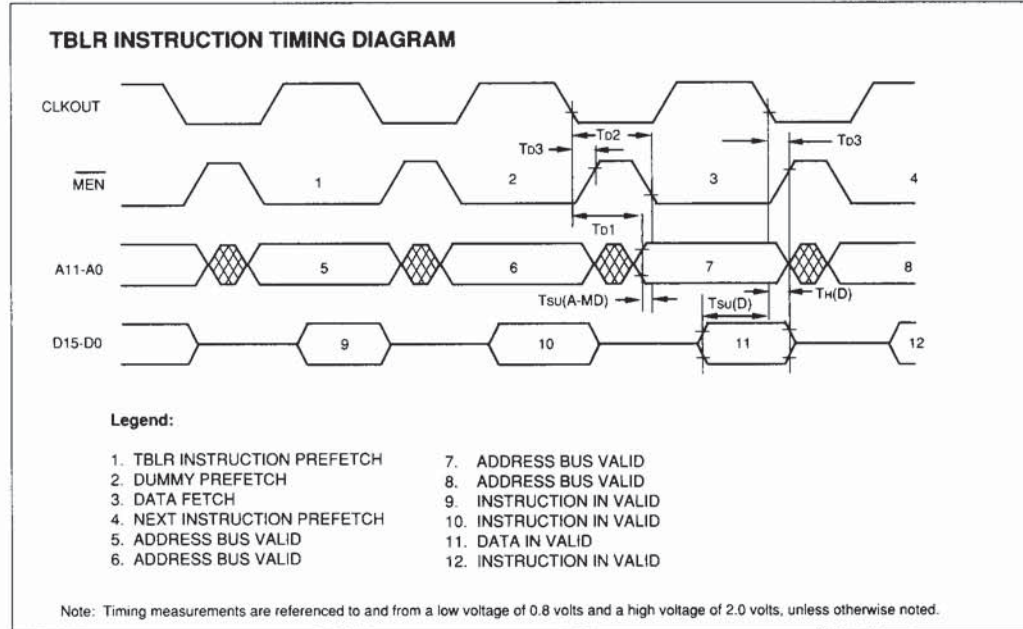
*These values were derived from characterization data and are not tested.
 Note: 1. Address bus will be valid upon $\overline{\text{WE}}\uparrow$, $\overline{\text{DEN}}\uparrow$, or $\overline{\text{MEN}}\uparrow$.
 2. Data may be removed from the data bus upon $\overline{\text{MEN}}\uparrow$ or $\overline{\text{DEN}}\uparrow$ preceding CLKOUT↓

MEMORY AND PERIPHERAL INTERFACE TIMING (CONT.)

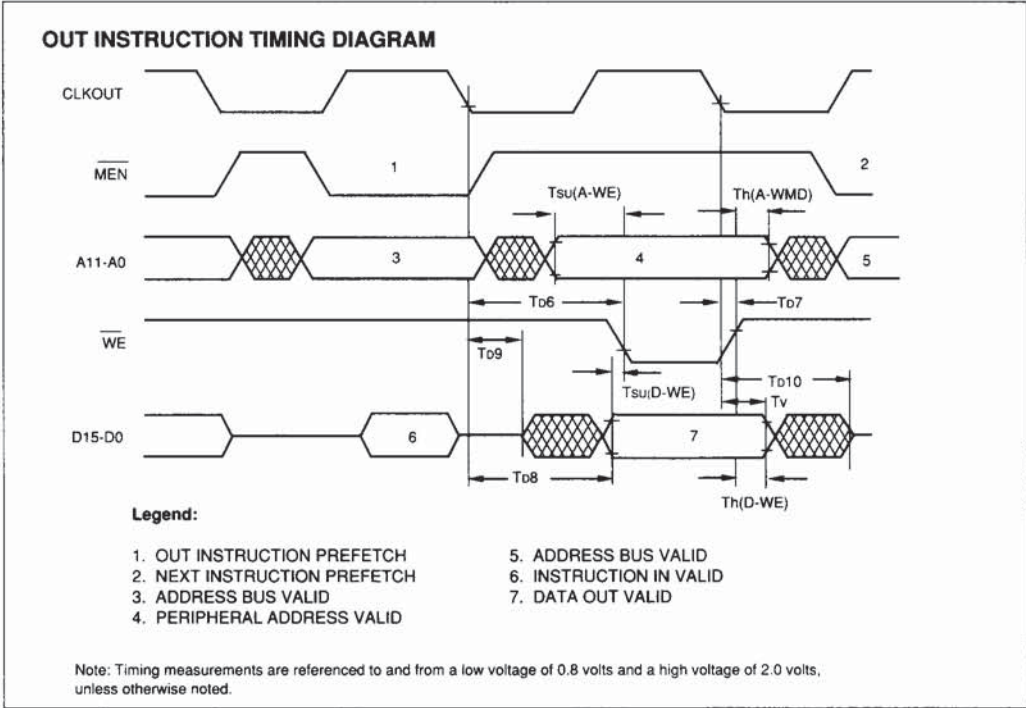
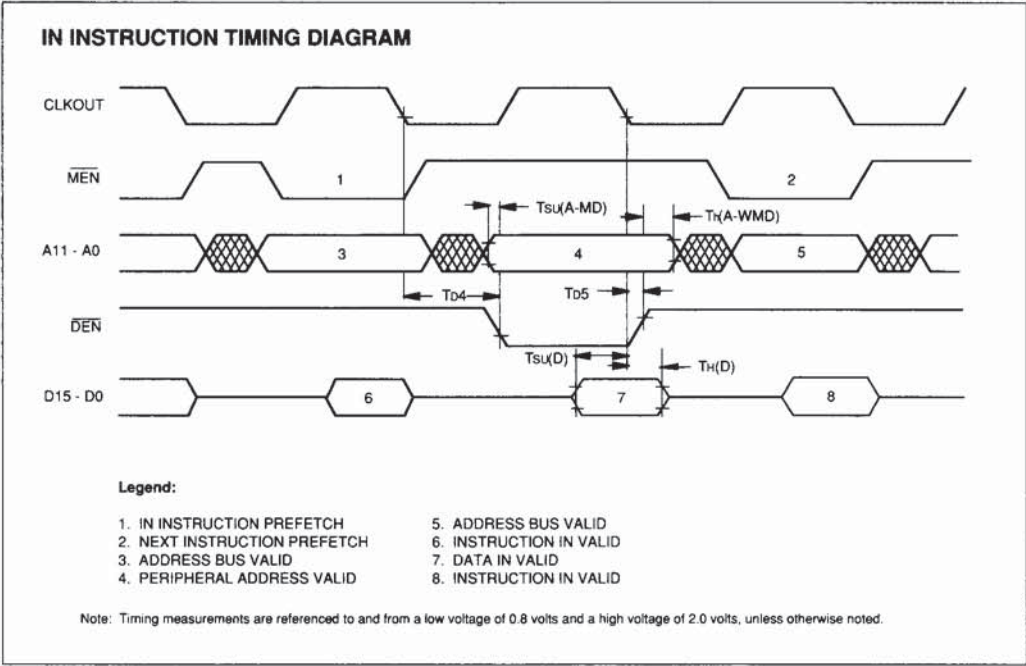


DSP320C10

INSTRUCTION TIMING DIAGRAMS (CONT.)



INSTRUCTION TIMING DIAGRAMS (CONT.)

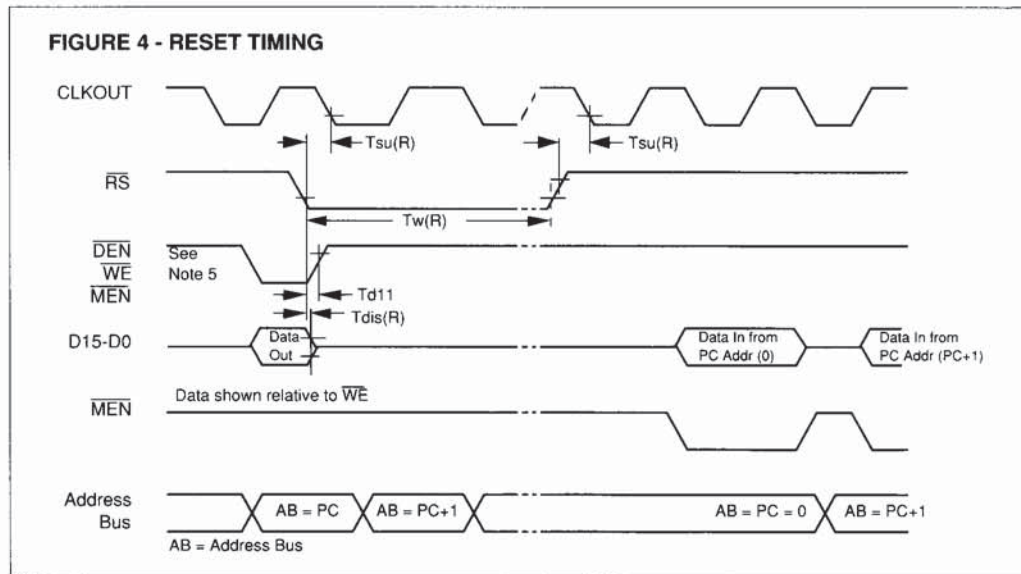


DSP320C10

RESET (RS) TIMING

| RESET TIMING AC CHARACTERISTICS | | | | | | |
|---|--------------|-----------|-----|---------------------|------|--------------|
| Timing requirements over recommended operating conditions | | | | | | |
| Characteristics | Sym | Min | Nom | Max | Unit | Conditions |
| Reset (\overline{RS}) setup time prior to CLKOUT. See notes 1-4. DSP320C10-32 | $T_{su}(R)$ | 38 | — | — | ns | See Figure 2 |
| \overline{RS} pulse duration | $T_w(R)$ | $5T_c(C)$ | — | — | ns | |
| Delay time $\overline{DEN}\uparrow$, $\overline{WE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}\downarrow$ | T_{d11} | — | — | $T_c(C) + 50^*$ | ns | |
| Data bus disable time after \overline{RS} | $T_{dis}(R)$ | — | — | $3/4T_c(C) + 120^*$ | ns | |

Note: RS can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.
 *These values were derived from characterization data and are not tested.

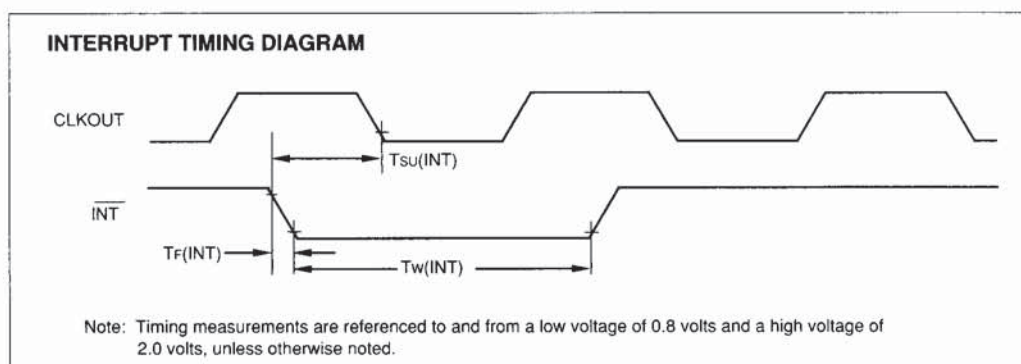


Notes:

- \overline{RS} forces \overline{DEN} , \overline{WE} , and \overline{MEN} high and tristates data bus DO through D15. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}\downarrow$.
- \overline{RS} must be maintained for a minimum of five clock cycles.
- Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}\uparrow$.
- Due to the synchronizing action on \overline{RS} , time to execute the function can vary dependent upon when $\overline{RS}\uparrow$ or $\overline{RS}\downarrow$ occur in the CLK cycle.
- Diagram shown is for definition purpose only. \overline{DEN} , \overline{WE} , and \overline{MEN} are mutually exclusive.
- Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
- During a write cycle, \overline{RS} may produce an invalid write address.

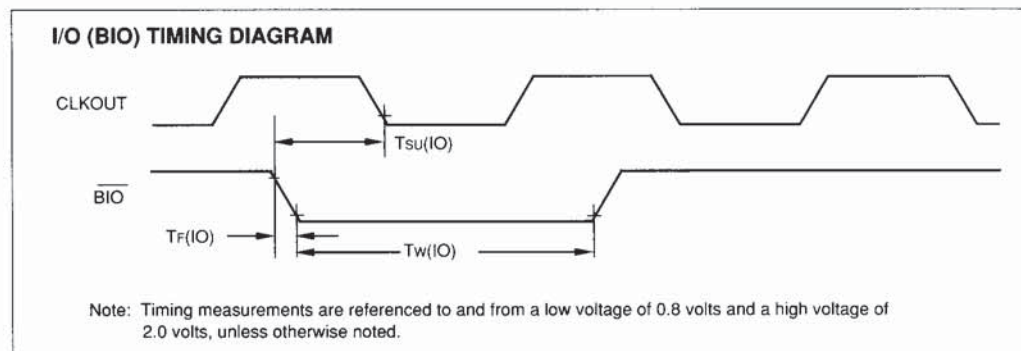
INTERRUPT (INT) TIMING

| INTERRUPT TIMING AC CHARACTERISTICS | | | | | | |
|---|----------------------|-----------------|-----|-----|-------------------------------|------------|
| Timing requirements over recommended operating conditions | | | | | * These values are not tested | |
| Characteristics | Sym | Min | Nom | Max | Unit | Conditions |
| Fall time $\overline{\text{INT}}$ | $T_f(\text{INT})$ | — | — | 15* | ns | |
| Pulse duration $\overline{\text{INT}}$ | $T_w(\text{INT})$ | $T_c(\text{C})$ | — | — | ns | |
| Setup time $\overline{\text{INT}}\downarrow$ before $\text{CLKOUT}\downarrow$ | $T_{su}(\text{INT})$ | 38 | — | — | ns | |



I/O (BIO) TIMING

| I/O (BIO) AC CHARACTERISTICS | | | | | | |
|---|---------------------|-----------------|-----|-----|-------------------------------|------------|
| Timing requirements over recommended operating conditions | | | | | * These values are not tested | |
| Characteristics | Sym | Min | Nom | Max | Unit | Conditions |
| Fall time $\overline{\text{BIO}}$ | $T_f(\text{IO})$ | — | — | 15* | ns | |
| Pulse duration $\overline{\text{BIO}}$ | $T_w(\text{IO})$ | $T_c(\text{C})$ | — | — | ns | |
| Setup time $\overline{\text{BIO}}\downarrow$ before $\text{CLKOUT}\downarrow$ | $T_{su}(\text{IO})$ | 38 | — | — | ns | |



DSP320C10

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

DSP320C10 - 32 I / P

Package:

P Plastic DIP
L PLCC

Temperature Range:

Blank 0 to 70° C
I -40 to 85° C

Frequency:

14 14.4 MHz
— 20.5 MHz
25 25.6 MHz
32 32.8 MHz

Device

DSP320C10 Digital Signal Processor