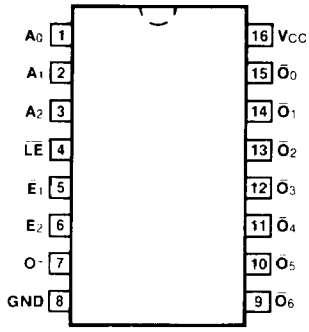
54S/74S137

1-OF-8 DECODER/DEMULTIPLEXER
(With Input Latches)

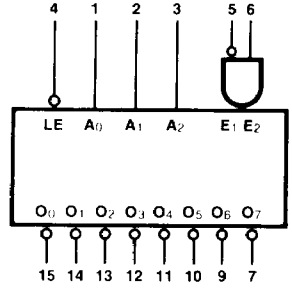
DESCRIPTION — The 'S137 is a very high speed 1-of-8 decoder/demultiplexer with latches on the three address inputs. This device essentially combines the function and speed of the 'S138 1-of-8 decoder with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the 'S137 acts as a 1-of-8 active LOW decoder. When the Latch Enable ($\overline{LE}$) goes from LOW to HIGH, the last data present at the inputs before this transition is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH. The output enable gate ($\overline{E}_1 \bullet E_2$) controls the state of the outputs independent of the Address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and E_2 is HIGH. The 'S137 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems. The 'S137 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **COMBINES 1-OF-8 DECODER WITH 3-BIT LATCH**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION OR INDEPENDENT CONTROLS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S137PC		9B
Ceramic DIP (D)	A	74S137DC	54S137DM	6B
Flatpak (F)	A	74S137FC	54S137FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

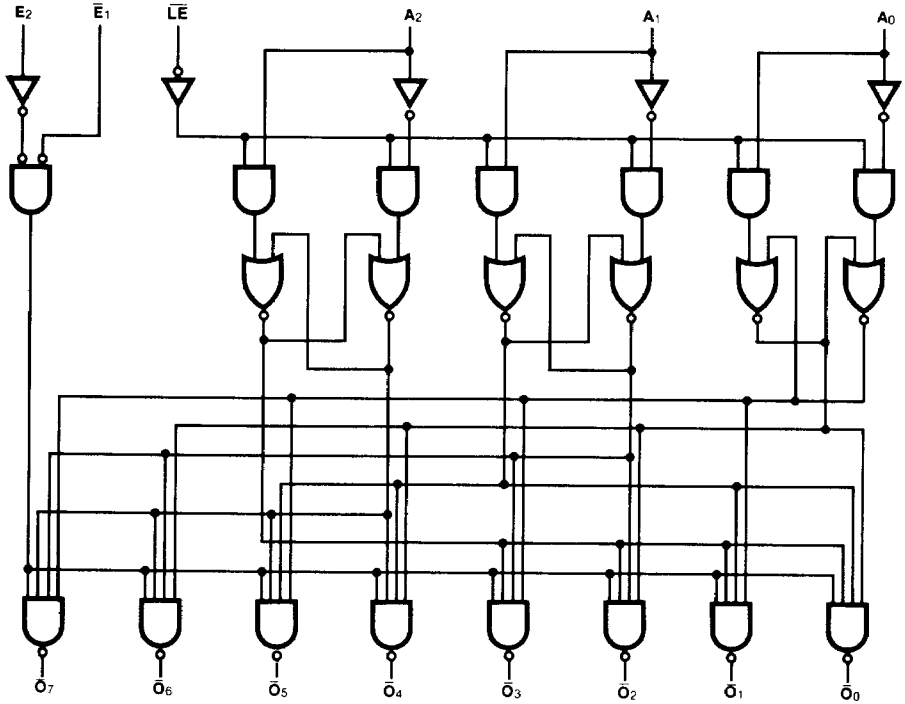
PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	1.25/1.25
$\overline{LE}$	Latch Enable Input (Active LOW)	1.25/1.25
$\overline{E}_1$	Enable Input (Active LOW)	1.25/1.25
E_2	Enable Input (Active HIGH)	1.25/1.25
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)	25/12.5

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	L	H	X	X	X	STABLE							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 'S137 is a very high speed 1-of-8 decoder/demultiplexer fabricated with the Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$ — $\overline{O}_7$). The 'S137 also features a 3-bit latch on the Address inputs. The device functions as a 1-of-8 decoder (same as 'S138) when the Latch Enable ($\overline{LE}$) is LOW. When $\overline{LE}$ is HIGH, the address present one setup time prior to the LOW-to-HIGH transition of $\overline{LE}$ will be stored in the address latches and the outputs will not be affected by further address changes. The output enable control is an AND gate comprised of one active LOW input ($\overline{E}_1$) and one active HIGH input (E_2). All outputs are HIGH unless the enable inputs ($\overline{E}_1 \bullet E_2$) are in their true (active) state.

A non-overlapping decoder with edge-triggered address inputs can be easily implemented by tying the Latch Enable input $\overline{LE}$ to the active HIGH Enable input (E_2). When this input ($\overline{LE} \bullet E_2$) is LOW, all outputs are forced HIGH and a new address enters the latches. When the $\overline{LE} \bullet E_2$ input goes HIGH, the address is stored in the latches and the corresponding output gate is enabled (goes LOW). In this configuration, the address must be stable only one setup time prior to the LOW-to-HIGH transition of the $\overline{LE} \bullet E_2$ input. The addressed output remains active LOW as long as the ($\overline{LE} \bullet E_2$) input remains HIGH, even if the address changes. Data or control information can thus be strobed into the 'S137 from very noisy or bus oriented systems using a LOW pulse width equal to the minimum latch enable pulse width $t_w(L)$.

The multiple enable inputs along with the address latches allows easy expansion to a 1-of-64 decoder with nonoverlapping outputs (see *Figure a*).

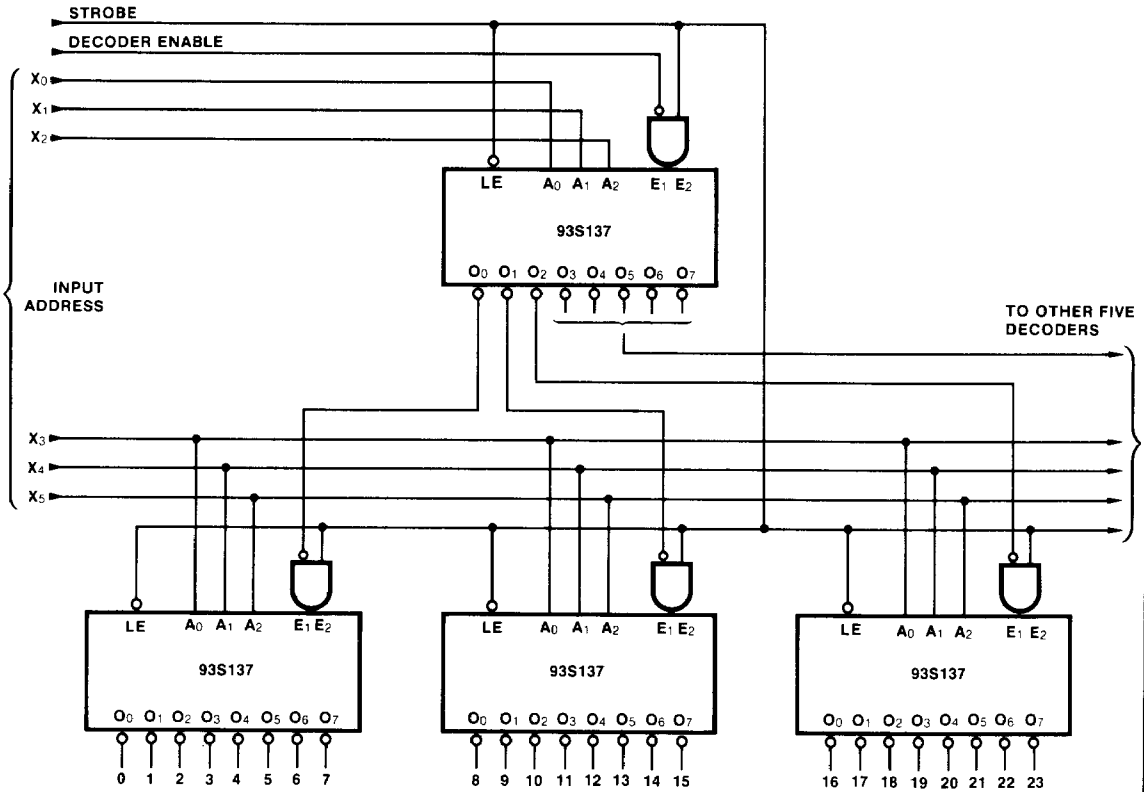


Fig. a High Speed 1-of-64 Decoder with Input Data Storage

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		95	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		12 20	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$		10 12	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_2$ to $\overline{O}_n$		12 12	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to $\overline{O}_n$		12 20	ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74S		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH A_n to $\overline{LE}$	4.5		ns	Fig. 3-13
t_h (H)	Hold Time HIGH A_n to $\overline{LE}$	0		ns	
t_s (L)	Setup Time LOW A_n to $\overline{LE}$	6.5		ns	Fig. 3-13
t_h (L)	Hold Time LOW A_n to $\overline{LE}$	0		ns	
t_w (L)	$\overline{LE}$ Pulse Width LOW	7.0		ns	Fig. 3-21

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