CMOS

REGISTERS

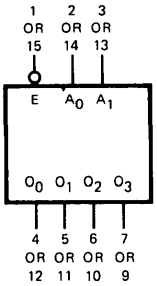
Item	Function	DEVICE NO.	No. of Bits	Serial Entry	Parallel Entry No. of Bits	Clock Edge	Max Clock Frequency MHz (Typ) V_{DD} = 10V	Clock To Output Delay - ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
1	Parallel-In/Parallel-Out	**4035B**	4	$J\bar{K}$	4	L→H	17	90	C39	4L,6B,9B
2	Parallel-In/Parallel-Out Bidirectional	**40194B**	4	D	4	L→H	14	45	C40	4L,6B,9B
3	Parallel-In/Parallel-Out	**40195B**	4	$J\bar{K}$	4	L→H	14	45	C41	4L,6B,9B
4	Serial-In/Parallel-Out	**4015B**	8	D	—	L→H	14	85	C42	4L,6B,9B
5	Parallel-In/Serial-Out	**4014B**	8	D	8	L→H	14 7	68	C43	4L,6B,9B
6	Parallel-In/Serial-Out	**4021B**	8	D	8	L→H	18 1	74	C44	4L,6B,9B
7	Serial-In/Serial-Out	**4006B**	18	D	—	H→L	30	37	C45	3I,6A,9A
8	Serial-In/Serial-Out	**4731B**	256	D	—	H→L	8 0	95	C46	3I,6A,9A
9	Serial-In/Serial-Out	**4031B**	64	D	—	L→H	8 0	60	C78	4L,6B,9B
10	Serial-In/Serial-Out Variable	**4557B**	1 to 64	D	—	2- H→L or L→H	10	150	C80	4L,6B,9B
11	Parallel/Serial-Input/Output	**4034B**	8	D	8	L→H	8 0	155	C79	4M,6N,9N

DECODERS/DEMULTIPLEXERS

Item	Function	DEVICE NO.	Address Inputs	Active LOW Enable	Output Configuration	Select Delay ns (Typ) V_{DD} = 10V	Enable Delay ns (Typ) V_{DD} = 10V	Logic/Connection Diagram	Package(s)
12	Dual 1-of-4 Decoder	**4555B**	2x2	2	H	60	60	C34	4L,6B,9B
13	Dual 1-of-4 Decoder	**4556B**	2x2	2	L	68	58	C35	4L,6B,9B
14	1-of-10 Decoder	**4028B**	4	—	H	66	—	C36	4L,6B,9B
15	1-of-16 Decoder	**4514B**	4	1	H	95	95	C37	4M,6N,9N,9U
16	1-of-16 Decoder	**4515B**	4	1	L	95	95	C38	4M,6N,9N,9U
17	Dual 4-Channel Demultiplexer	**4052B**	2	1	H	125	105	C64	4L,6B,9B

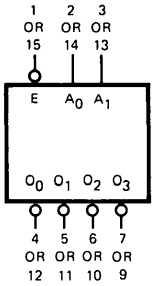
DIGITAL-CMOS

C34
4555B



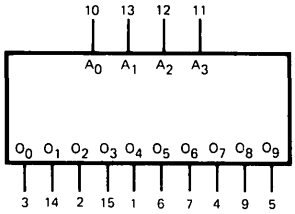
V_{DD} = Pin 16
V_{SS} = Pin 8

C35
4556B



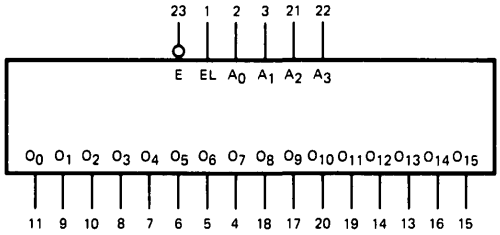
V_{DD} = Pin 16
V_{SS} = Pin 8

C36
4028B



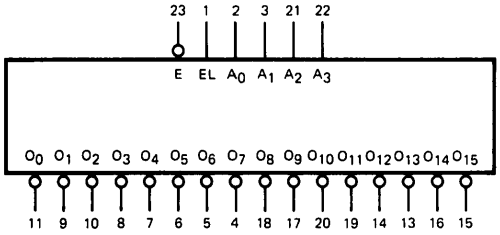
V_{DD} = Pin 16
V_{SS} = Pin 8

C37
4514B



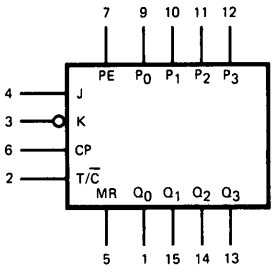
V_{DD} = Pin 24
V_{SS} = Pin 12

C38
4515B



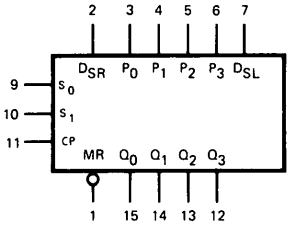
V_{DD} = Pin 24
V_{SS} = Pin 12

C39
4035B



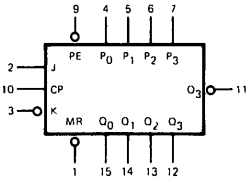
V_{DD} = Pin 16
V_{SS} = Pin 8

C40
40194B



V_{DD} = Pin 16
V_{SS} = Pin 8

C41
40195B



V_{DD} = Pin 16
V_{SS} = Pin 8

NOTE The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-Line Packages

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