

Complete data sheet available via web, Harris' home page: <http://www.semi.harris.com> or via Harris AnswerFAX, see Section 17

August 1997

Numeric/Alphanumeric Triplexed LCD Display Drivers

Features

- ICM7231 Drives 8 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Parallel Format
- ICM7232 Drives 10 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Serial Format
- All Signals Required to Drive Rows and Columns of Triplexed LCD Display are Provided
- Display Voltage Independent of Power Supply
- On-Chip Oscillator Provides All Display Timing
- Total Power Consumption Typically 200 μ W, Maximum 500 μ W at 5V
- Low-Power Shutdown Mode Retains Data With 5 μ W Typical Power Consumption at 5V, 1 μ W at 2V
- Direct Interface to High-Speed Microprocessors

Description

The ICM7231 and ICM7232 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high-performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	NUMBER OF DIGITS	INPUT FORMAT	PKG. NO.
ICM7231BFIJL	-25 to 85	40 Ld CERDIP	8 Digit	Parallel	F40.6
ICM7231BFIPL	-25 to 85	40 Ld PDIP	8 Digit	Parallel	E40.6
ICM7232BFIPL	-25 to 85	40 Ld PDIP	10 Digit	Serial	E40.6
ICM7232CRIPL	-25 to 85	40 Ld PDIP	10 Digit	Serial	E40.6

NOTE:

All versions intended for triplexed LCD displays.

ICM7231, ICM7232

Pinouts

**ICM7231BF
(PDIP, CERDIP)
TOP VIEW**

CS	1	40	V _{DD}
V _{DISP}	2	39	A2
BP1	3	38	A1
BP2	4	37	A0
BP3	5	36	V _{SS}
b1, c1, an11	6	35	BD3
a1, g1, d1	7	34	BD2
f1, e1, an21	8	33	BD1
b2, c2, an12	9	32	BD0
a2, g2, d2	10	31	AN2
f2, e2, an22	11	30	AN1
b3, c3, an13	12	29	f8, a8, an28
a3, g3, d3	13	28	a8, g8, d8
f3, e3, an23	14	27	b8, c8, an18
b4, c4, an14	15	26	f7, e7, an27
a4, g4, d4	16	25	a7, g7, d7
f4, e4, an24	17	24	b7, c7, an17
b5, c5, an15	18	23	f6, e6, an26
a5, g5, d5	19	22	a6, g6, d6
f5, e5, an25	20	21	b6, c6, an16

**ICM7232AF, BF
(PDIP, CERDIP)
TOP VIEW**

DATA CLOCK INPUT	1	40	V _{DD}
V _{DISP}	2	39	WRITE INPUT
BP1	3	38	DATA INPUT
BP2	4	37	DATA ACCEPTED OUTPUT
BP3	5	36	V _{SS}
b1, c1, an11	6	35	b1, c1, an11
a1, g1, d1	7	34	a1, g1, d1
f1, e1, an21	8	33	f1, e1, an21
b2, c2, an12	9	32	b2, c2, an12
a2, g2, d2	10	31	a2, g2, d2
f2, e2, an22	11	30	f2, e2, an22
b3, c3, an13	12	29	b3, c3, an13
a3, g3, d3	13	28	a3, g3, d3
f3, e3, an23	14	27	f3, e3, an23
b4, c4, an14	15	26	b4, c4, an14
a4, g4, d4	16	25	a4, g4, d4
f4, e4, an24	17	24	f4, e4, an24
b5, c5, an15	18	23	b5, c5, an15
a5, g5, d5	19	22	a5, g5, d5
f5, e5, an25	20	21	f5, e5, an25

**ICM7232CR
(PDIP)
TOP VIEW**

DATA CLOCK INPUT	1	40	V _{DD}
V _{DISP}	2	39	WRITE INPUT
BP1	3	38	DATA INPUT
BP2	4	37	DATA ACCEPTED OUTPUT
BP3	5	36	V _{SS}
b1, c1, an11	6	35	b6, c6, an16
a1, g1, d1	7	34	a6, g6, d6
f1, e1, an21	8	33	f6, e6, an26
b2, c2, an12	9	32	b7, c7, an17
a2, g2, d2	10	31	a7, g7, d7
f2, e2, an22	11	30	f7, e7, an27
b3, c3, an13	12	29	b8, c8, an18
a3, g3, d3	13	28	a8, g8, d8
f3, e3, an23	14	27	f8, a8, an28
b4, c4, an14	15	26	b9, c9, an19
a4, g4, d4	16	25	a9, g9, d9
f4, e4, an24	17	24	f9, e9, an29
b5, c5, an15	18	23	b10, c10, an110
a5, g5, d5	19	22	a10, g10, d10
f5, e5, an25	20	21	f10, e10, an210