LC75841PE

Static Drive, 1/2-Duty Drive General-Purpose LCD Driver

ON Semiconductor®

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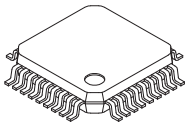


LQFP36 7x7 / QFP36

Overview

The LC75841PE is static drive or 1/2-duty drive, microcontroller-controlled general-purpose LCD driver that can be used in applications such as frequency display in products with electronic tuning. In addition to being capable to drive up to 54 segments directly, it can control up to 4 general-purpose output ports.

Features

- Serial data control of switching between static drive mode and 1/2 duty drive mode.
  When 1/1-duty: Capable of driving up to 27 segments
  When 1/2-duty: Capable of driving up to 54 segments
- Serial data input supports CCB* format communication with the system controller.
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port functions
  (up to 4 general-purpose output ports).
- Serial data control of the frame frequency of the common and segment output waveforms.
- Either RC oscillator operating or external clock operating mode can be selected with the serial control data.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- Allows compatible operation with the LC75842 (842 mode transfer function).

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

June 2017 - Rev. 1
Publication Order Number :
LC75841PE/D

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +7.0	V
	$V_{IN}2$	OSC	−0.3 to V_{DD}+0.3	
Output voltage	V_{OUT}	S1 to S27, COM1, COM2, P1 to P4, OSC	−0.3 to V_{DD}+0.3	V
Output current	$I_{OUT}1$	S1 to S27	300	μA
	$I_{OUT}2$	COM1, COM2	3	mA
	$I_{OUT}3$	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 105°C	50	mW
Operating temperature	Topr		−40 to +105	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = −40 to +105°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.0		6.0	V
Input high-level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.45V_{DD}		6.0	V
	$V_{IH}2$	OSC External clock operating mode	0.45V_{DD}		V_{DD}	
Input low-level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSC External clock operating mode	0		0.2V_{DD}	
Recommended external resistor for RC oscillation	Rosc	OSC RC oscillator operating mode		39		kΩ
Recommended external capacitor for RC oscillation	Cosc	OSC RC oscillator operating mode		1000		pF
Guaranteed range of RC oscillation	fosc	OSC RC oscillator operating mode	19	38	76	kHz
External clock operating frequency	f_{CK}	OSC External clock operating mode [Figure 3]	19	38	76	kHz
External clock duty cycle	D_{CK}	OSC External clock operating mode [Figure 3]	30	50	70	%
Data setup time	tds	CL, DI [Figure 1], [Figure 2]	160			ns
Data hold time	tdh	CL, DI [Figure 1], [Figure 2]	160			ns
CE wait time	tcp	CE, CL [Figure 1], [Figure 2]	160			ns
CE setup time	tcs	CE, CL [Figure 1], [Figure 2]	160			ns
CE hold time	tch	CE, CL [Figure 1], [Figure 2]	160			ns
High-level clock pulse width	tϕH	CL [Figure 1], [Figure 2]	160			ns
Low-level clock pulse width	tϕL	CL [Figure 1], [Figure 2]	160			ns
Rise time	tr	CE, CL, DI [Figure 1], [Figure 2]		160		ns
Fall time	tf	CE, CL, DI [Figure 1], [Figure 2]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure 4], [Figure 5], [Figure 6]	10			μs

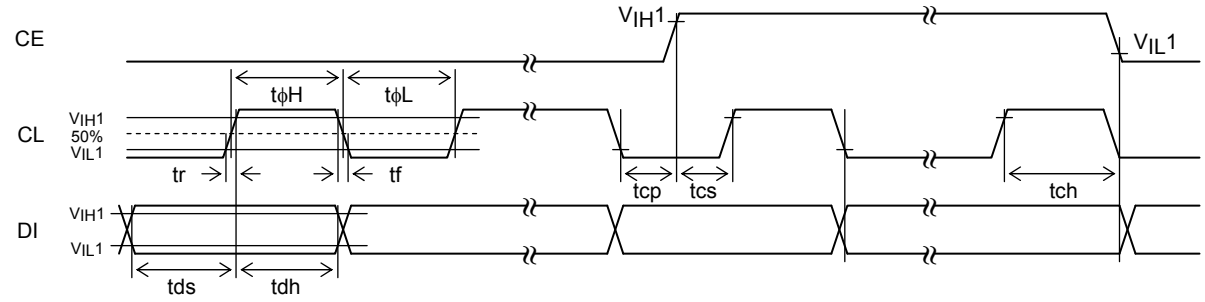
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.03V_{DD}$		V
Input high-level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 6.0 V			5.0	μA
	$I_{IH}2$	OSC	$V_I = V_{DD}$ External clock operating mode			5.0	
Input low-level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0 V	−5.0			μA
	$I_{IL}2$	OSC	V_I = 0 V External clock operating mode	−5.0			
Output high-level voltage	$V_{OH}1$	S1 to S27	I_O = −20 μA	V_{DD}−0.9			V
	$V_{OH}2$	COM1, COM2	I_O = −100 μA	V_{DD}−0.9			
	$V_{OH}3$	P1 to P4	I_O = −1 mA	V_{DD}−0.9			
Output low-level voltage	$V_{OL}1$	S1 to S27	I_O = 20 μA			0.9	V
	$V_{OL}2$	COM1, COM2	I_O = 100 μA			0.9	
	$V_{OL}3$	P1 to P4	I_O = 1 mA			0.9	
Output middle-level voltage	V_{MID}	COM1, COM2	1/2 bias I_O = ±100 μA	$1/2V_{DD}$ −0.9		$1/2V_{DD}$ +0.9	V
Oscillator frequency	fosc	OSC	RC oscillator operating mode, Rosc = 39 kΩ, Cosc = 1000 pF	30.4	38	45.6	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			15	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 6.0 V, Output open, RC oscillator operating mode, fosc = 38 kHz, Static		350	700	
	$I_{DD}3$	V_{DD}	V_{DD} = 6.0 V, Output open, RC oscillator operating mode, fosc = 38 kHz, 1/2 duty		1500	3000	
	$I_{DD}4$	V_{DD}	V_{DD} = 6.0 V, Output open, External clock operating mode, f_{CK} = 38 kHz, $V_{IH}2 = 0.5V_{DD}$, $V_{IL}2 = 0.1V_{DD}$, Static		450	900	
	$I_{DD}5$	V_{DD}	V_{DD} = 6.0 V, Output open, External clock operating mode, f_{CK} = 38 kHz, $V_{IH}2 = 0.5V_{DD}$, $V_{IL}2 = 0.1V_{DD}$, 1/2 duty		1600	3200	

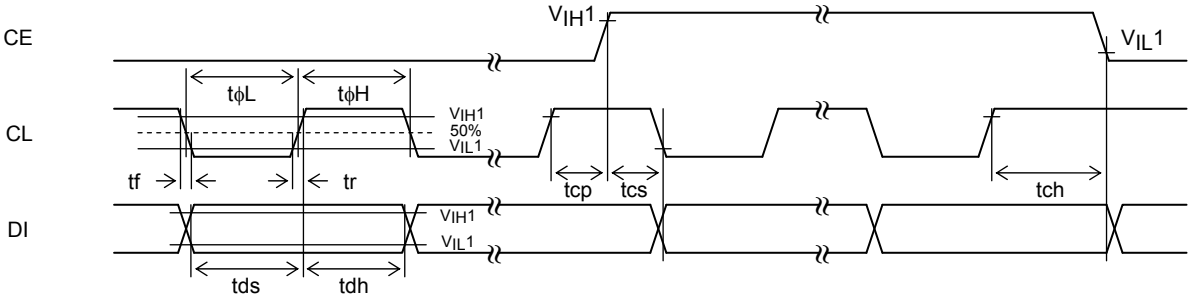
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When CL is stopped at the low level



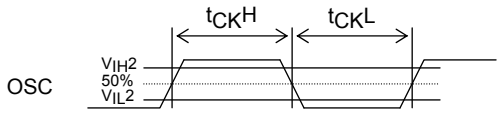
[Figure 1]

2. When CL is stopped at the high level



[Figure 2]

3. OSC pin clock timing in external clock operating mode



$$f_{CK}=\frac{1}{t_{CKH}+t_{CKL}}\ [kHz]$$

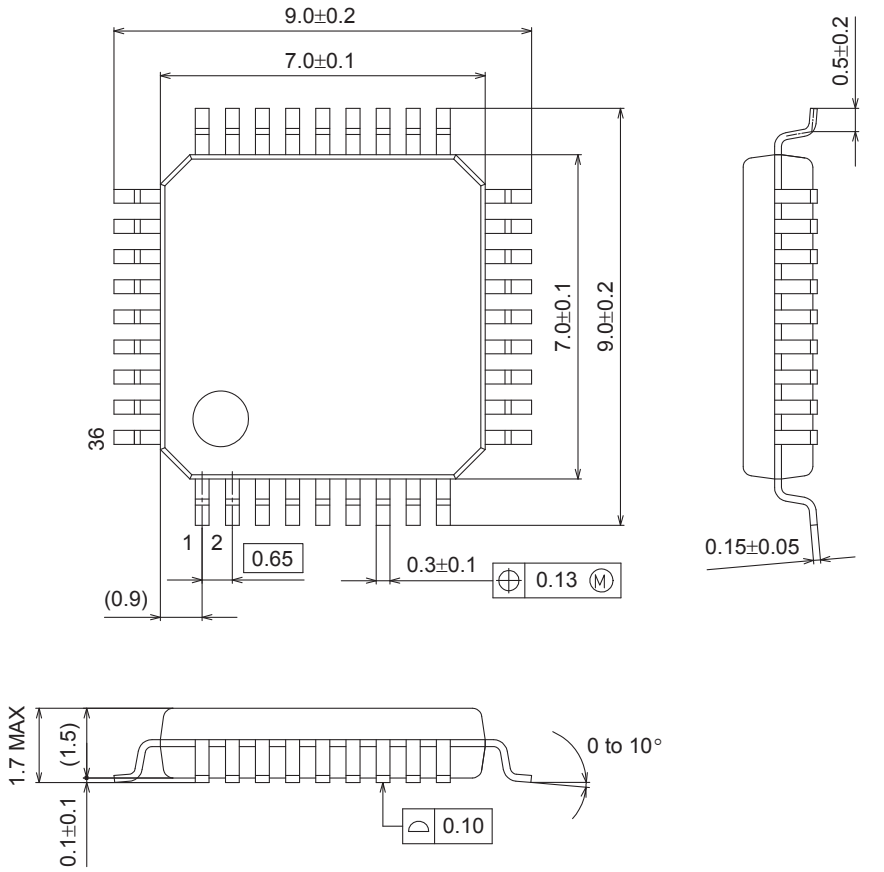
$$D_{CK}=\frac{t_{CKH}}{t_{CKH}+t_{CKL}}\times 100[\%]$$

[Figure 3]

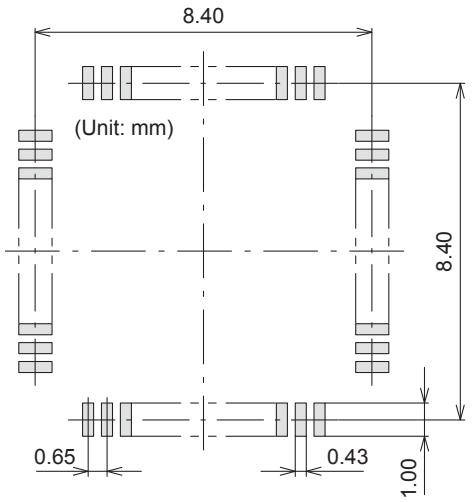
Package Dimensions

unit : mm

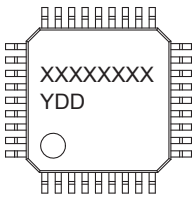
LQFP36 7x7 / QFP36
CASE 561AV
ISSUE A



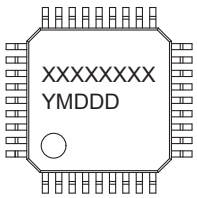
SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data



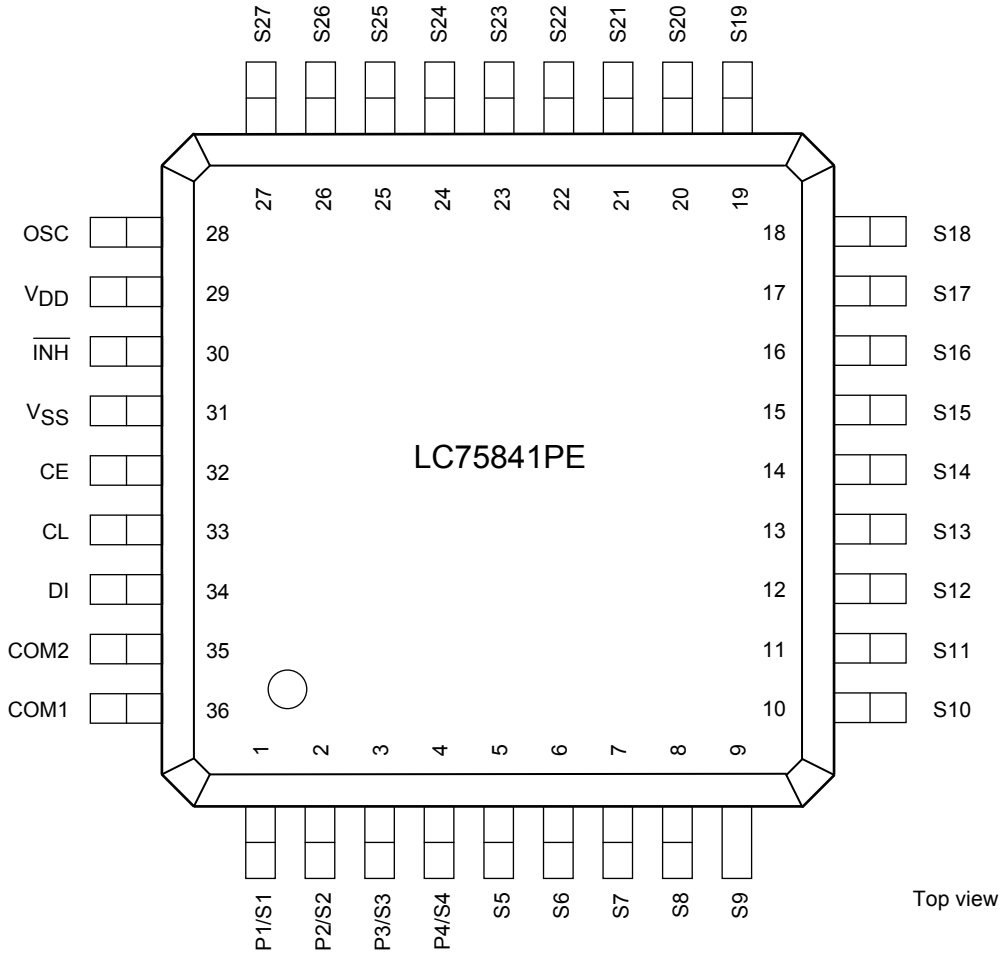
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

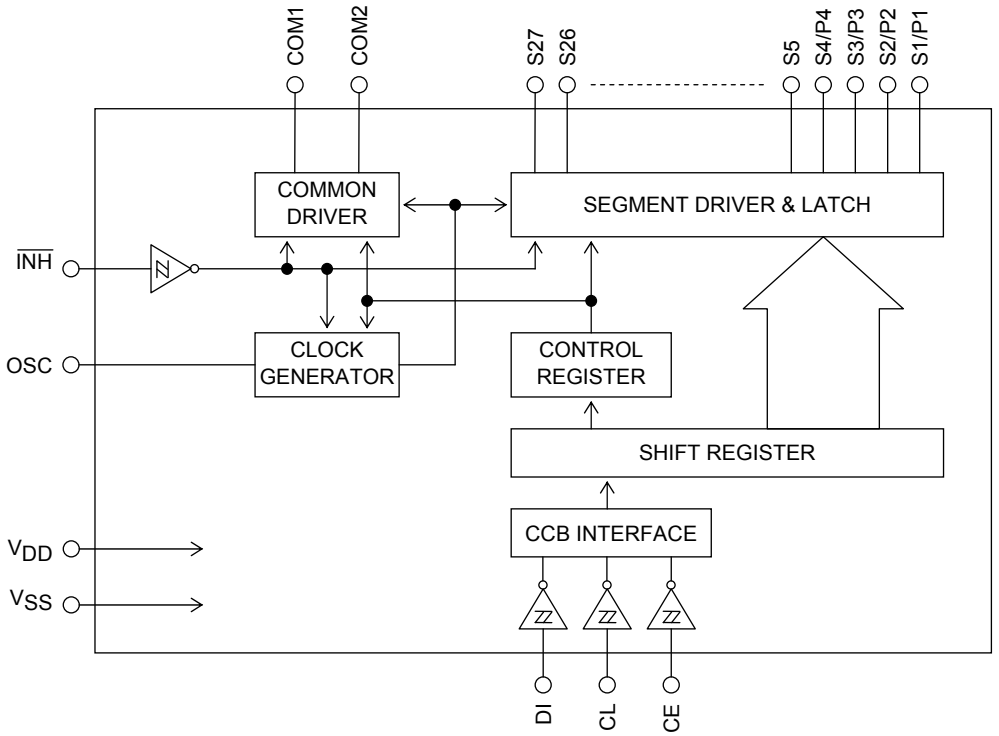
NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment



Block Diagram



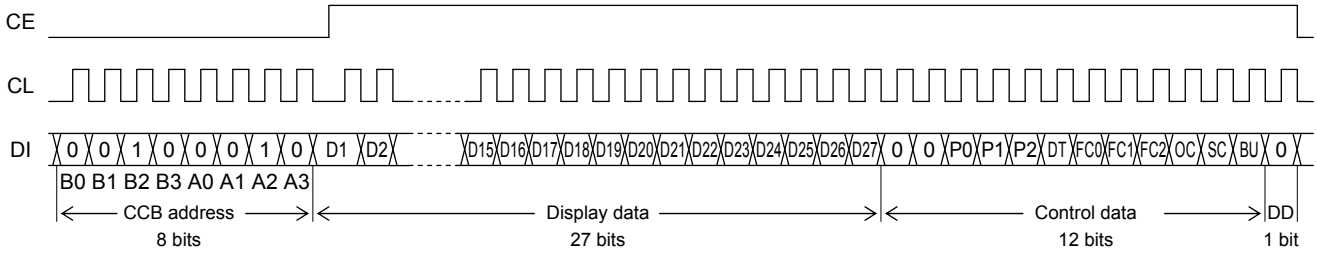
Pin Functions

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S4/P4 S5 to S27	1 to 4 5 to 27	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports when so set up by the control data.	-	O	OPEN
COM1 COM2	36 35	Common driver outputs. The frame frequency is fo [Hz].	-	O	OPEN
OSC	28	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can be used as the external clock input pin if external clock operating mode is selected with the control data.	-	I/O	V_{DD}
CE CL DI	32 33 34	Serial data transfer inputs. Must be connected to the controller. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ -	I I I	GND
$\overline{INH}$	30	Display off control input • $\overline{INH}$ = low (V_{SS}) ...Display forced off S1/P1 to S4/P4 = low (V_{SS}) (These pins are forcibly set to the segment output port function and held at the V_{SS} level.) S5 to S27 = low (V_{SS}) COM1, COM2 = low (V_{SS}) OSC = Z (high impedance) RC oscillation stopped Inhibits external clock input. • $\overline{INH}$ = high (V_{DD})...Display on RC oscillation enabled (RC oscillator operating mode) Enables external clock input (external clock operating mode) However, serial data transfer is possible when the display is forced off.	L	I	GND
V_{DD}	29	Power supply. Provide a voltage in the range 4.0 to 6.0 V.	-	-	-
V_{SS}	31	Ground pin. Must be connected to ground.	-	-	-

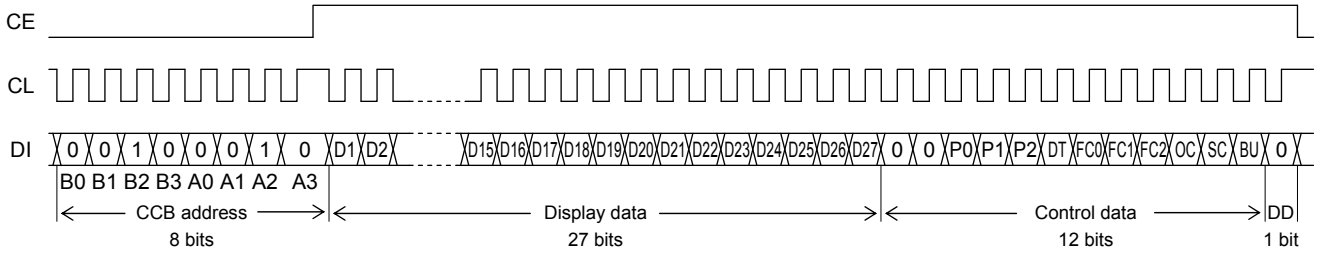
Serial Data Transfer Formats

(1) Static drive mode

1. When CL is stopped at the low level



2. When CL is stopped at the high level

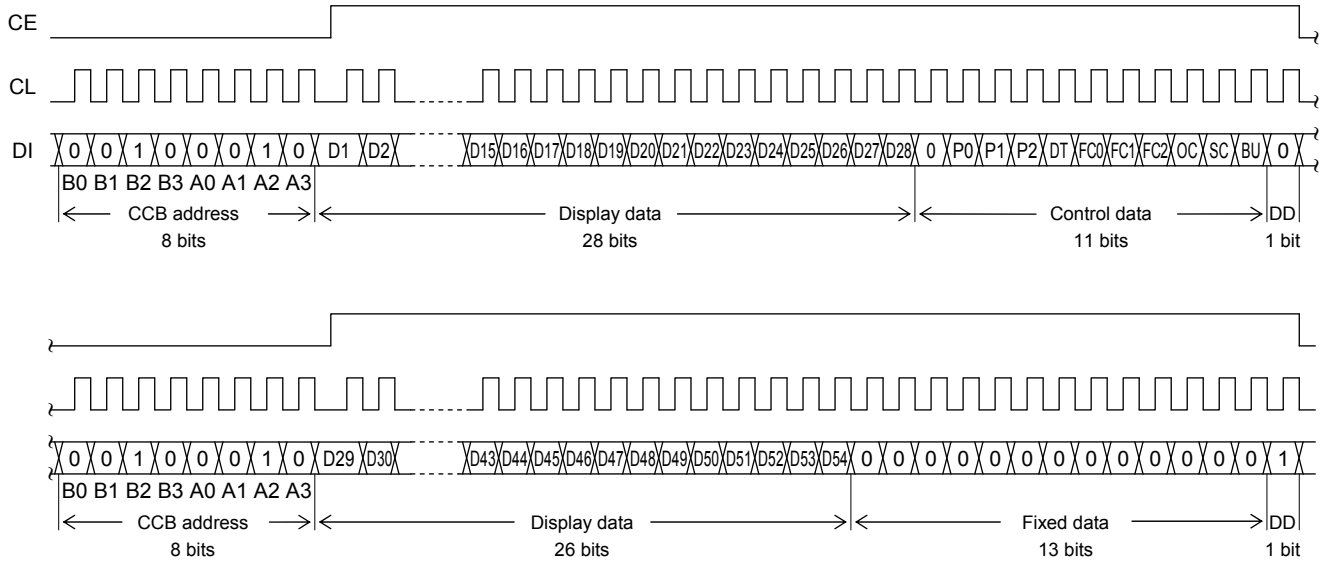


Note: DD is the direction data.

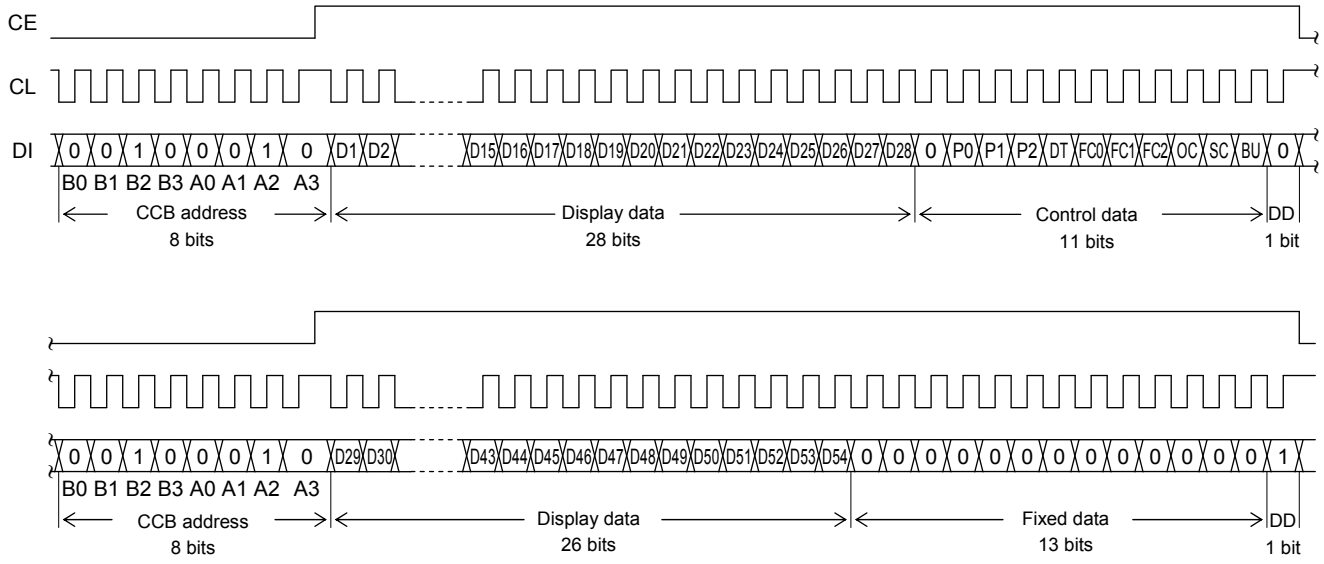
- CCB address ..... "44H"
- D1 to D27 ..... Display data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- DT ..... Static drive or 1/2 duty drive switching control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency control data
- OC ..... RC oscillator operating mode/external clock operating mode switching control data
- SC ..... Segments on/off control data
- BU ..... Normal mode/power-saving mode control data

(2) 1/2 duty drive mode

1. When CL is stopped at the low level



2. When CL is stopped at the high level



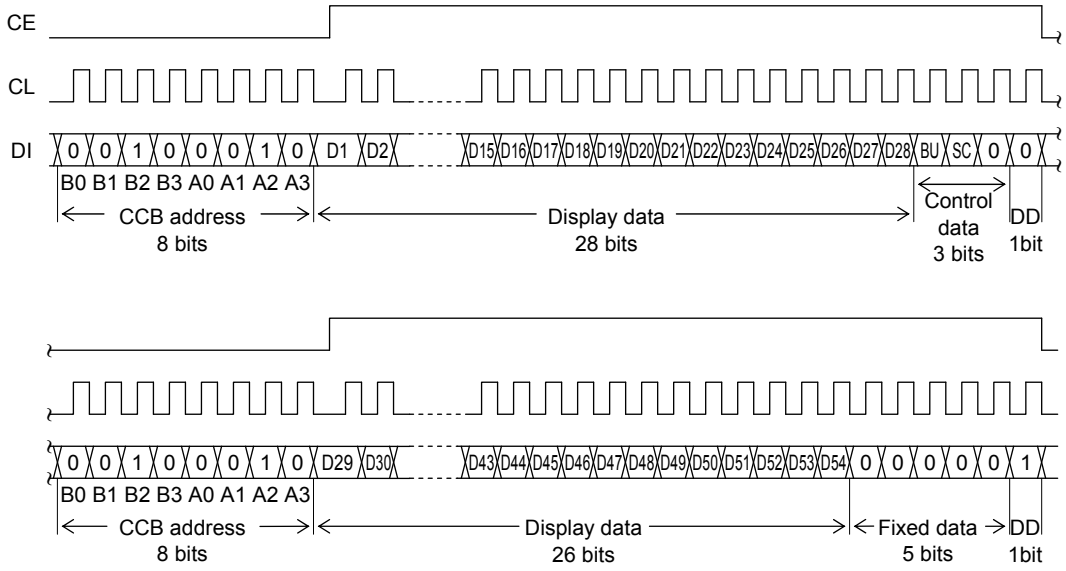
Note: DD is the direction data.

- CCB address ..... "44H"
- D1 to D54 ..... Display data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- DT ..... Static drive or 1/2 duty drive switching control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency control data
- OC ..... RC oscillator operating mode/external clock operating mode switching control data
- SC ..... Segments on/off control data
- BU ..... Normal mode/power-saving mode control data

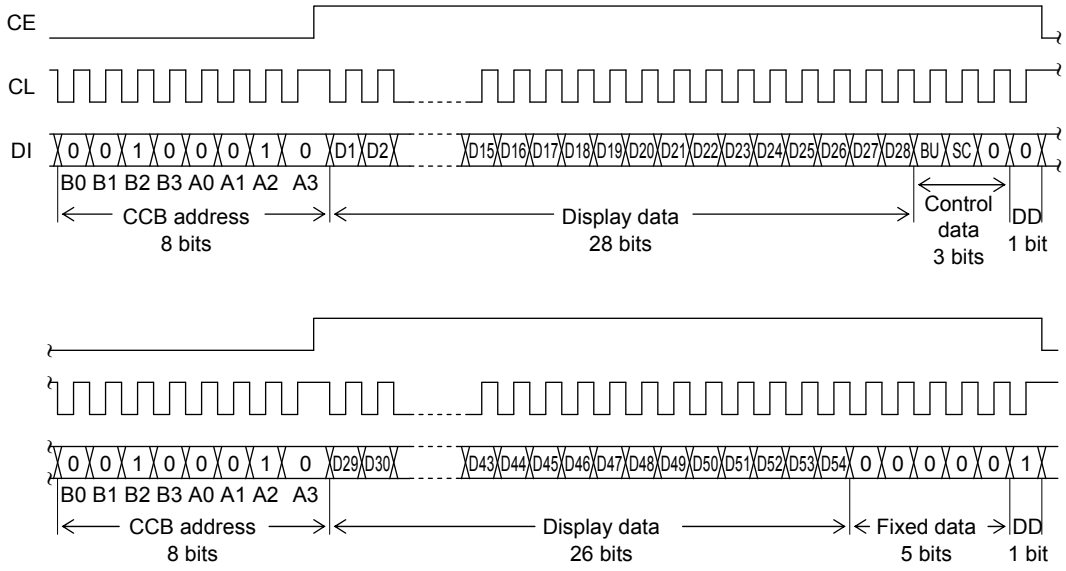
Serial Data Transfer Formats (When in 842 mode data transfer)

(1) 1/2 duty drive mode (When in 842 mode data transfer)

1. When CL is stopped at the low level



2. When CL is stopped at the high level



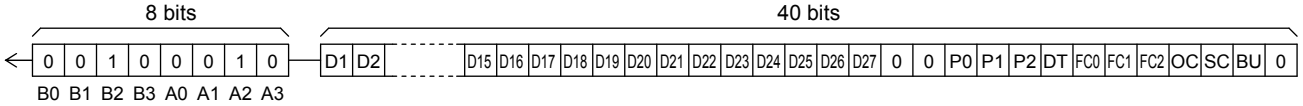
Note: DD is the direction data.

- CCB address ..... "44H"
- D1 to D54 ..... Display data
- BU ..... Normal mode/power-saving mode control data
- SC ..... Segments on/off control data

Serial Data Transfer Examples

(1) Static drive mode

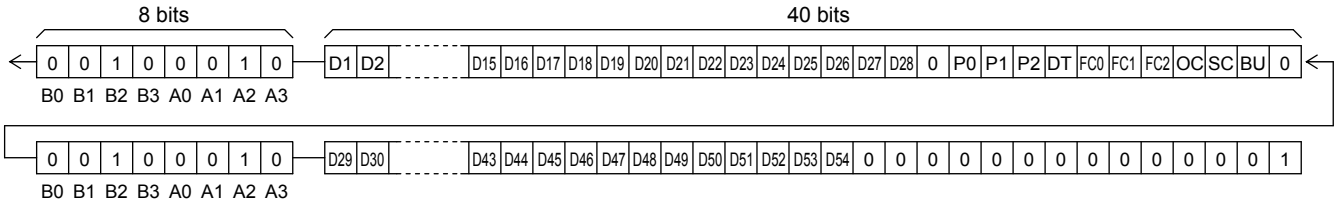
The serial data shown in the figure below must be sent.



(2) 1/2 duty drive mode

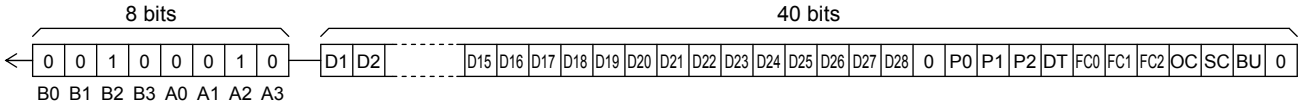
• When 29 or more segments are used

96 bits of serial data (including CCB address bits) must be sent.



• When fewer than 29 segments are used

The serial data shown below (the D1 to D28 display data and the control data) must always be sent.

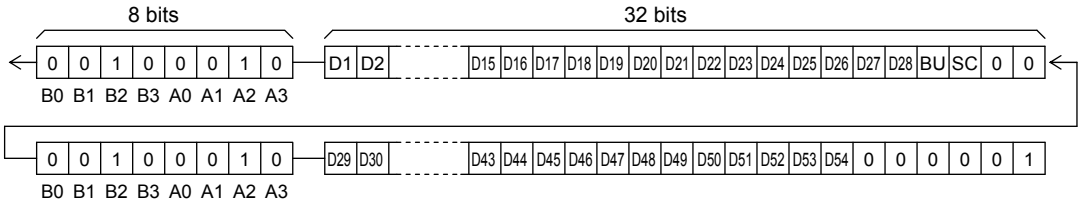


Serial Data Transfer Examples (When in 842 mode data transfer)

(1) 1/2 duty drive mode (When in 842 mode data transfer)

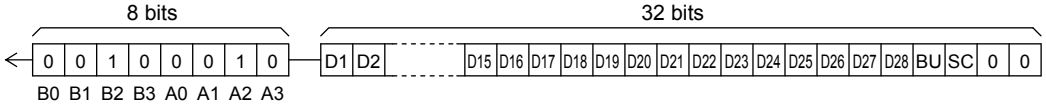
• When 29 or more segments are used

80 bits of serial data (including CCB address bits) must be sent.



• When fewer than 29 segments are used

The serial data shown in the figure below (the D1 to D28 display data, and the control data) must be sent.



Control Data Functions

1. P0 to P2: Segment output port/general-purpose output port switching control data
   These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S4/P4 output pins.
   However, segment output port is forcibly selected when in 842 mode data transfer.

Control data			Output pin state			
P0	P1	P2	S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4

Note: Sn (n = 1 to 4): Segment output ports
Pn (n = 1 to 4): General-purpose output ports

Note that when the general-purpose output port function is selected, the correspondence between the output pins and the display data will be that shown in the table.

Output pin	Corresponding display data	
	Static drive mode	1/2 duty drive mode
S1/P1	D1	D1
S2/P2	D2	D3
S3/P3	D3	D5
S4/P4	D4	D7

For example, if the general-purpose output port function is selected for the S4/P4 output pin in 1/2 duty drive mode, it will output a high level (V_{DD}) when display data D7 is 1, and a low level (V_{SS}) when D7 is 0.

2. DT: Static drive mode or 1/2 duty drive mode switching control data
   This control data bit selects either static drive mode or 1/2 duty drive mode.
   However, 1/2 duty drive mode is forcibly selected when in 842 mode data transfer.

DT	Duty drive mode	Output pin state (COM2)
0	Static drive mode	V_{SS} level
1	1/2 duty drive mode	COM2

Note: COM2…Common output

3. FC0 to FC2: Common/segment output waveform frame frequency control data
   These control data bits set the frame frequency of the common and segment output waveforms.
   However, fo=fosc/384 is forcibly selected when in 842 mode data transfer.

Control data			Frame frequency fo [Hz]
FC0	FC1	FC2	
1	1	0	fosc/768, f_{CK}/768
1	1	1	fosc/576, f_{CK}/576
0	0	0	fosc/384, f_{CK}/384
0	0	1	fosc/288, f_{CK}/288
0	1	0	fosc/192, f_{CK}/192

4. OC: RC oscillator operating mode/external clock operating mode switching control data
   This control data bit switches the OSC pin function
   (either RC oscillator operating mode or external clock operating mode).
   However RC oscillator operating mode is forcibly selected when in 842 mode data transfer.

OC	OSC pin function
0	RC oscillator operating mode
1	External clock operating mode

Note: An external resistor, Rosc, and an external capacitor, Cosc, must be connected to the OSC pin if RC oscillator operating mode is selected.

5. SC: Segment on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

6. BU: Normal mode/power-saving mode control data
   This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power-saving mode. In RC oscillator operating mode (OC = 0), the OSC pin oscillator is stopped, and in external clock operating mode (OC = 1), acceptance of the external clock is stopped. In this mode the common and segment output pins go to the V_{SS} levels. However, S1/P1 to S4/P4 output pins that are set to be general-purpose output ports by the control data P0 to P2 can be used as general-purpose output ports.

Display Data and Output Pin Correspondence

(1) Static drive mode

Output pin	COM1
S1/P1	D1
S2/P2	D2
S3/P3	D3
S4/P4	D4
S5	D5
S6	D6
S7	D7
S8	D8
S9	D9
S10	D10

Output pin	COM1
S11	D11
S12	D12
S13	D13
S14	D14
S15	D15
S16	D16
S17	D17
S18	D18
S19	D19
S20	D20

Output pin	COM1
S21	D21
S22	D22
S23	D23
S24	D24
S25	D25
S26	D26
S27	D27

Notes: This applies to the case where the S1/P1 to S4/P4 output pins are set to be segment output ports.
The static drive mode cannot be selected when in 842 mode data transfer.

For example, the table below lists the output states for the S11 output pin.

Display data	Output pin (S11) state
D11	
0	The LCD segment corresponding to COM1 is off
1	The LCD segment corresponding to COM1 is on

(2) 1/2 duty drive mode

Output pin	COM1	COM2
S1/P1	D1	D2
S2/P2	D3	D4
S3/P3	D5	D6
S4/P4	D7	D8
S5	D9	D10
S6	D11	D12
S7	D13	D14
S8	D15	D16
S9	D17	D18
S10	D19	D20

Output pin	COM1	COM2
S11	D21	D22
S12	D23	D24
S13	D25	D26
S14	D27	D28
S15	D29	D30
S16	D31	D32
S17	D33	D34
S18	D35	D36
S19	D37	D38
S20	D39	D40

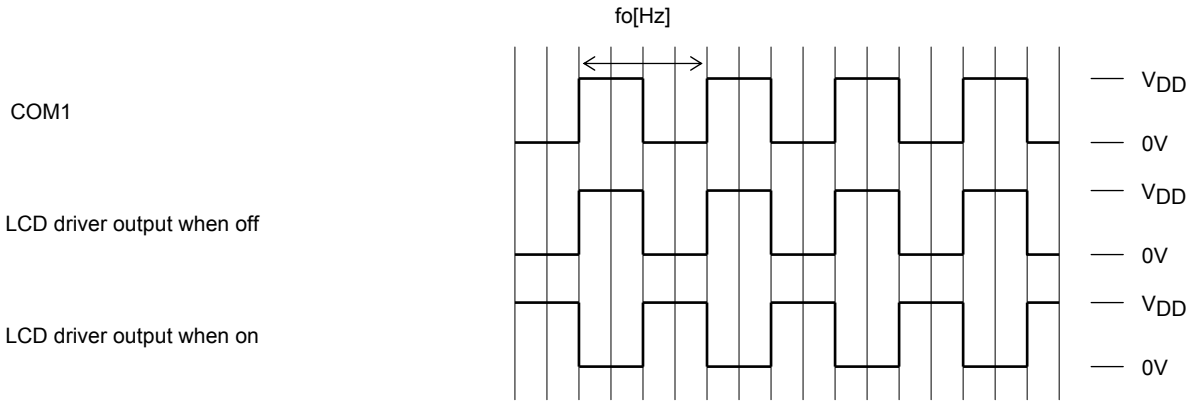
Output pin	COM1	COM2
S21	D41	D42
S22	D43	D44
S23	D45	D46
S24	D47	D48
S25	D49	D50
S26	D51	D52
S27	D53	D54

Note: This applies to the case where the S1/P1 to S4/P4 output pins are set to be segment output ports.

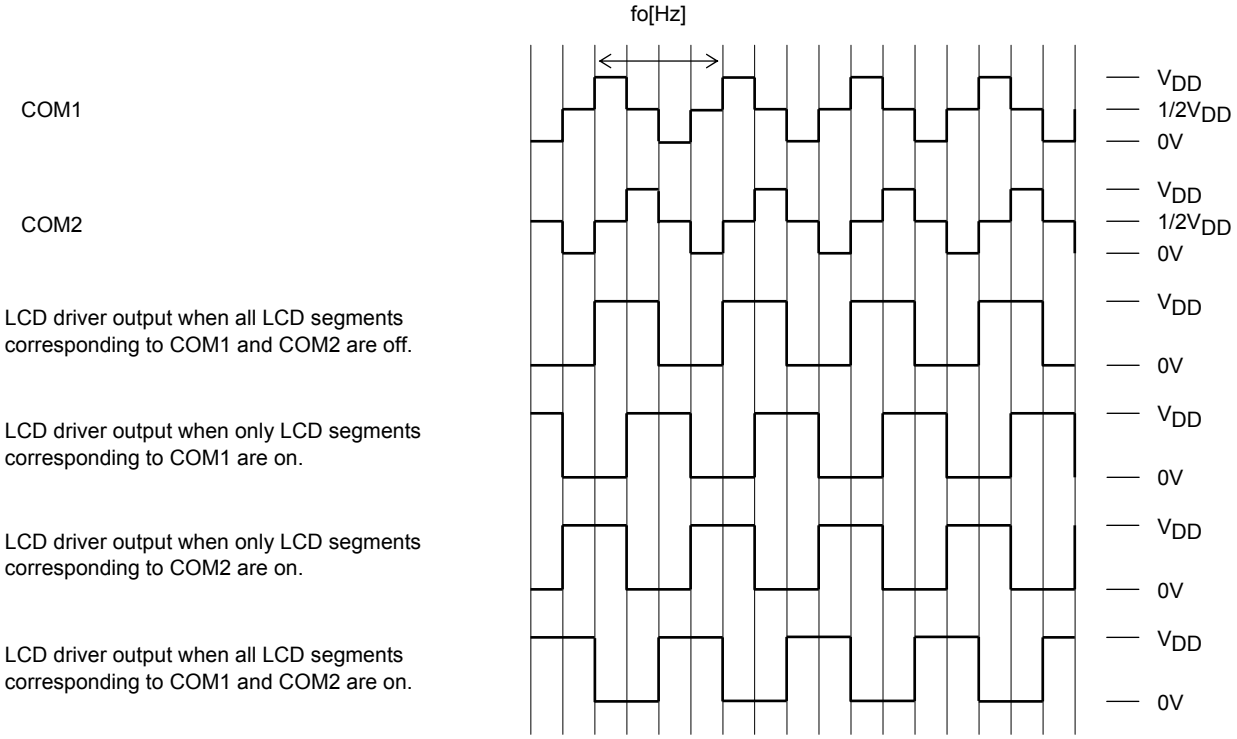
For example, the table below lists the output states for the S11 output pin.

Display data		Output pin (S11) state
D21	D22	
0	0	The LCD segments corresponding to COM1 and COM2 are off.
0	1	The LCD segment corresponding to COM2 is on.
1	0	The LCD segment corresponding to COM1 is on.
1	1	The LCD segments corresponding to COM1 and COM2 are on.

Output Waveforms (Static drive mode)



Output Waveforms (1/2 duty, 1/2 bias drive mode)

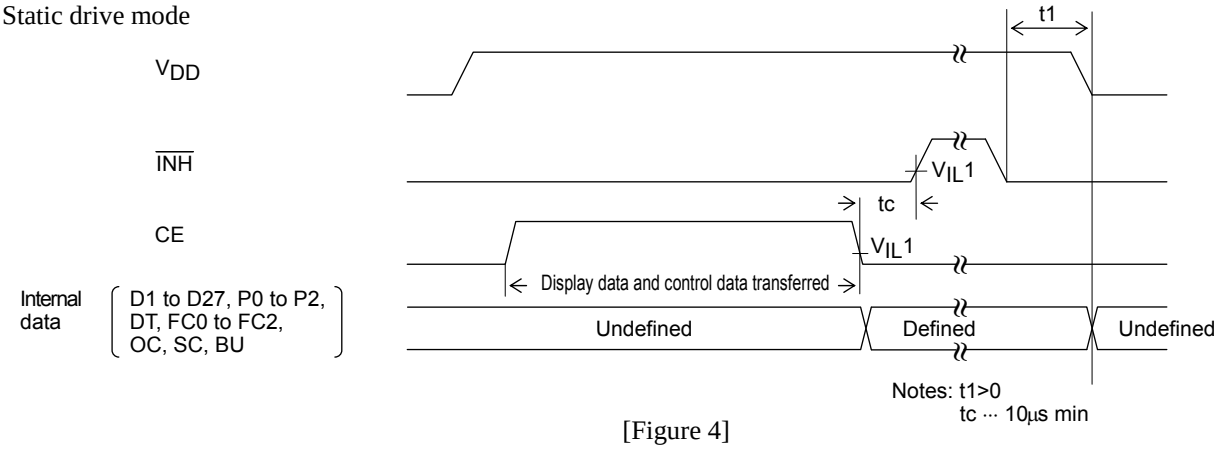


Control data			Frame frequency fo [Hz]
FC0	FC1	FC2	
1	1	0	fosc/768, f_{CK}/768
1	1	1	fosc/576, f_{CK}/576
0	0	0	fosc/384, f_{CK}/384
0	0	1	fosc/288, f_{CK}/288
0	1	0	fosc/192, f_{CK}/192

Display Control and the $\overline{INH}$ Pin

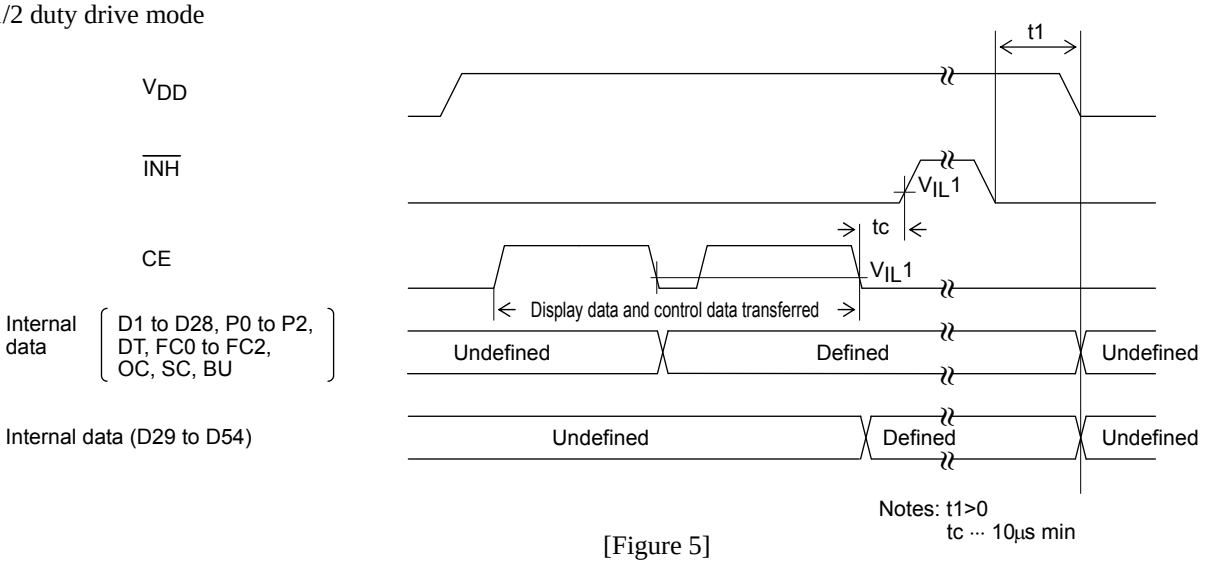
Since the IC's internal data (the display data D1 to D27 and the control data when in static drive mode, and the display data D1 to D54 and the control data when in 1/2 duty drive mode) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (setting S1/P1 to S4/P4 and S5 to S27, COM1, and COM2 to the V_{SS} level) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents unnecessary display at power on. (See figure 4, figure 5 and figure 6)

• Static drive mode



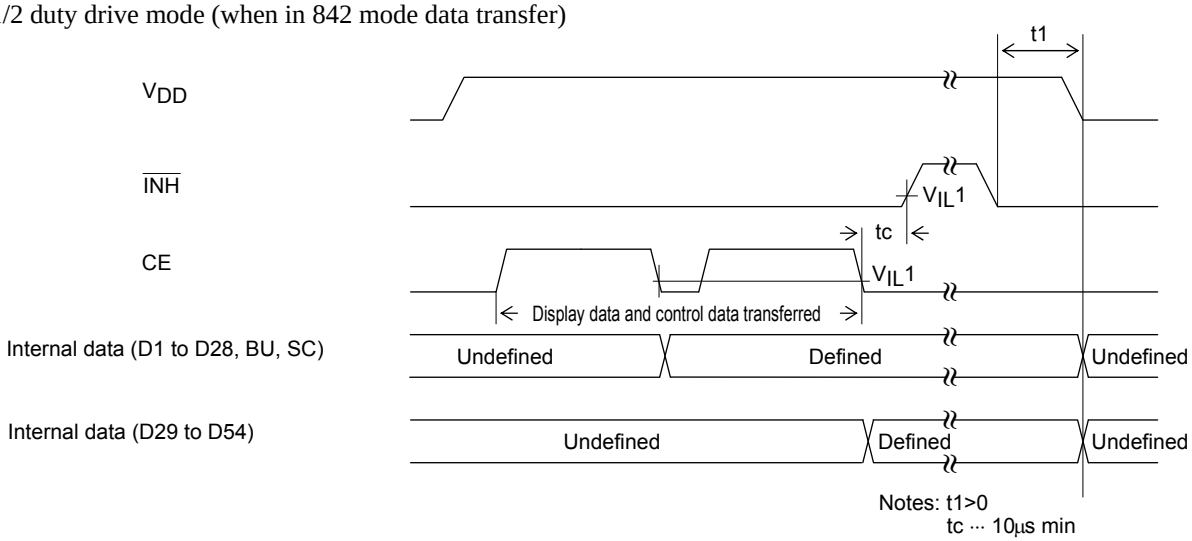
[Figure 4]

• 1/2 duty drive mode



[Figure 5]

• 1/2 duty drive mode (when in 842 mode data transfer)



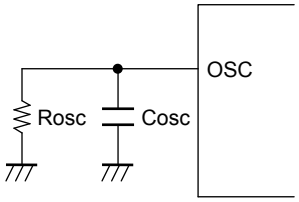
[Figure 6]

Notes on Controller Transfer of Display Data

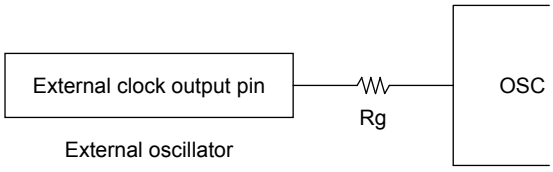
Since the LC75841PE transfer the display data (D1 to D54) in two separate transfer operations in 1/2 duty drive mode, we recommend that applications make a point of completing all of the display data transfer within a period of less than 30 ms to prevent observable degradation of display quality.

OSC Pin Peripheral Circuit

(1) RC oscillator operating mode (control data OC = 0)
An external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and GND if RC oscillator operating mode is selected.



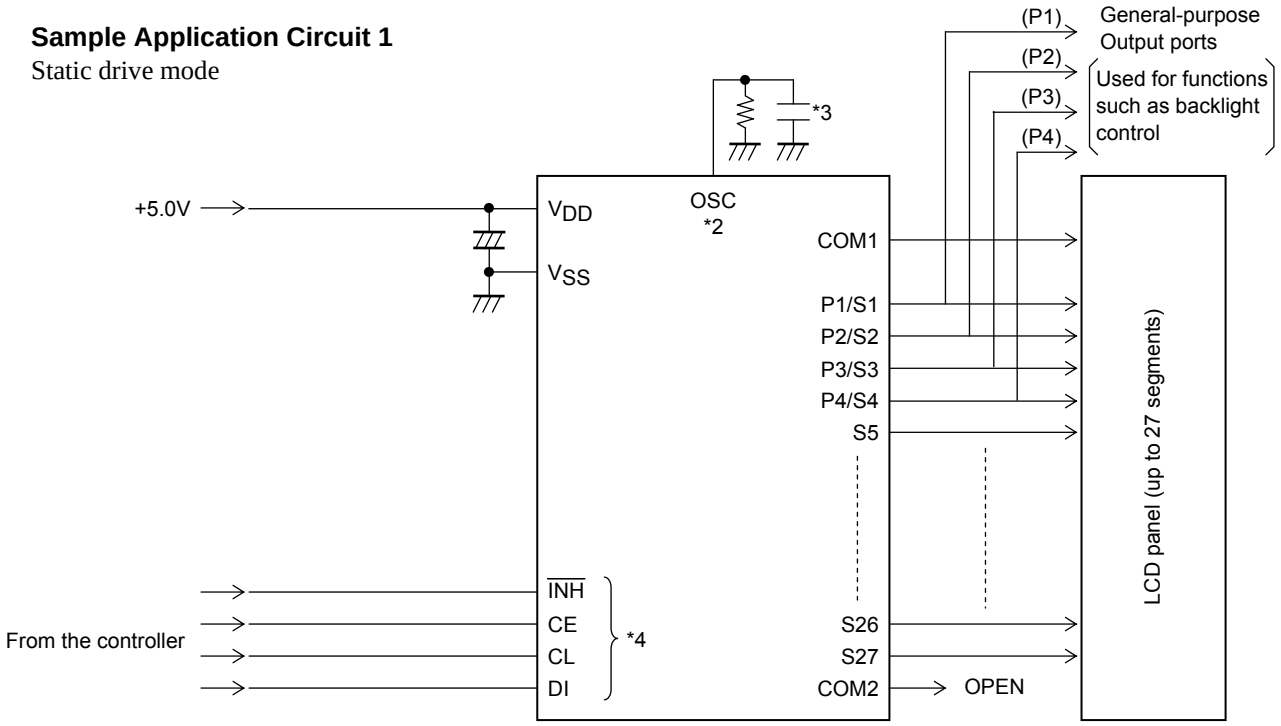
(2) External clock operating mode (control data OC = 1)
When the external clock operating mode is selected, insert a current protection resistor Rg (4.7 to 47 kΩ) between the OSC pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.



Note: Allowable current value at external clock output pin > $\frac{V_{DD}}{Rg}$

Sample Application Circuit 1

Static drive mode



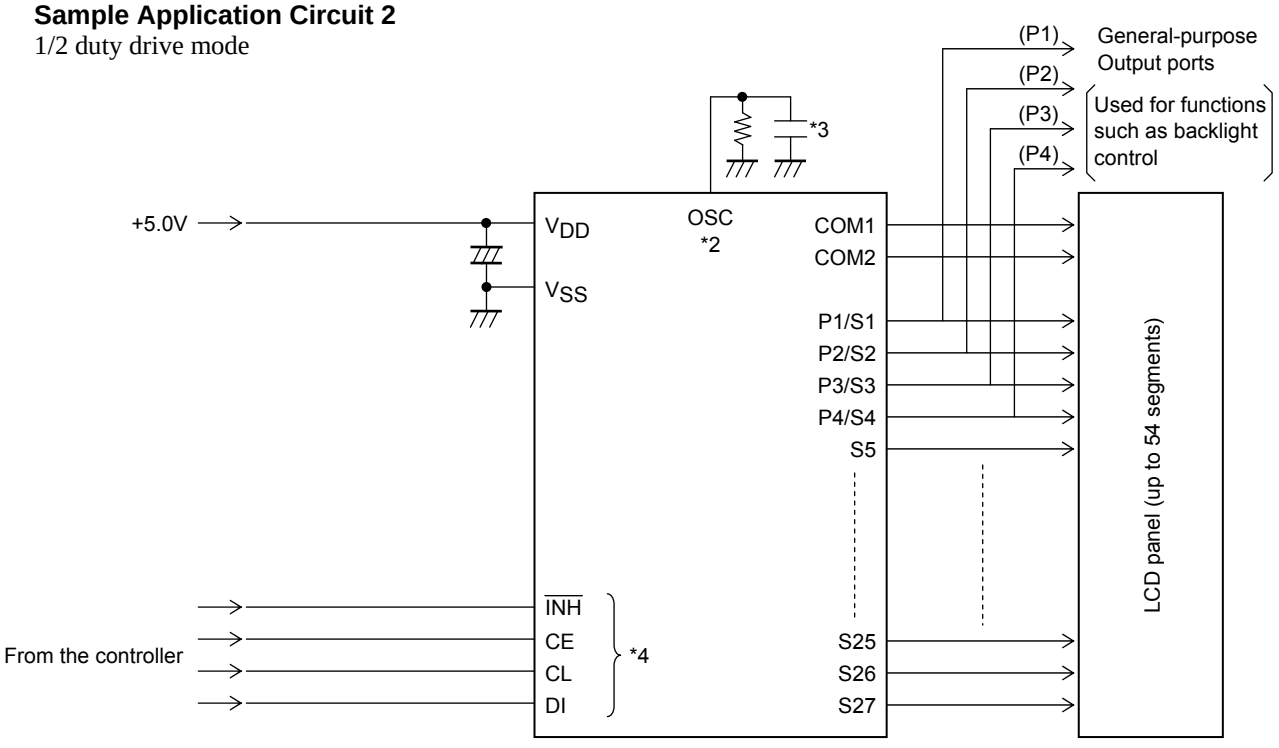
*2: In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. If external clock operating mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ), must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the "OSC Pin Peripheral Circuit" section.)

*3: When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected to the OSC pin, it should be in the range 220 to 2200 pF.

*4: The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3 V or 5.0 V.

Sample Application Circuit 2

1/2 duty drive mode



*2: In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. If external clock operating mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ), must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the "OSC Pin Peripheral Circuit" section.)

*3: When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected to the OSC pin, it should be in the range 220 to 2200 pF.

*4: The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3 V or 5.0 V.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75841PE-H	LQFP36 7x7 / QFP36 (Pb-Free / Halogen Free)	1250 / Tray JEDEC
LC75841PES-H	LQFP36 7x7 / QFP36 (Pb-Free / Halogen Free)	1250 / Tray JEDEC